**MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)**

(UGC Autonomous Institution, Affiliated to JNTUH, Accredited 2nd time by NAAC with 'A' Grade & NBA and Recipient of World Bank Assistance under TEQIP--II S.C. 1.1)

Maisammaguda (H), Medchal-Malkajgiri District, Telangana State – 500100

**Department of Electronics and Communication Engineering**

# CIRCULAR

Date:10.01.2022

All the students are hereby informed that value added courses on **VLSI Design and Verification** from 17/01/2022 to 21/01/2022 is being organized by the Department of Electronics and Communication Engineering. The resource person for this course is V. Kiran Kumar, Associate Professor, Department of ECE, MRCET, Hyderabad. Students are advised to register their names to the programme coordinator on or before 27/10/2021 and utilize this opportunity to enhance their skills by attending the programme.

The detailed program will be displayed in notice board

Copy to

1) Circulation in students classroom
2) All HOD's
3) Notice board
4) PA to principal for filing

HOD,ECE

Head, Dept. of ECE
Malla Reddy Engg. College
Maisammaguda, Dhullapally,
Secunderbad-500100

PRINCIPAL

Principal
Malla Reddy Engineering College
Maisammaguda, Dhulapally,
(Post Via Kompally), Sec'bad-500100.

## About the Institution

**Malla Reddy Engineering College (Autonomous)** is one of the reputed engineering colleges in Hyderabad, Telangana established in 2002. **MREC (A)** is part of Malla Reddy Group of Institutions (MRGI), founded by Sri. Ch. Malla Reddy Gaaru, currently Hon'ble Minister of Labor & Employment, Factories, Govt. of Telangana State. The college is situated in a serene, lushgreen environment in Maisammaguda, Gundlapochampally, Medchal (M), Medcha l- Malkajgiri District Telangana–500100.

MREC (A) is skillfully and smartly guided by **Dr. A. Ramaswami Reddy, Principal**, **MREC (A)** which is affiliated to JNTUH and an autonomous institution approved by UGC &JNTU Hyderabad first in Telangana state in 2014 for a period of 6 years from 2014-2020. The college is re-accredited by NAAC with 'A' Grade (II Cycle).Our eligible UG and PG programs received NBA accreditation twice. The college caters to wide ranging aspirations and goals of student communities by offering regular programs in various streams of Engineering and Management.

It provides world-class infrastructure facilities like RnD, Incubation Centre, EDC, IIIC, IPR, Start ups, Centre of Excellence, Innovation Council, many clubs for Faculty & Students and well-equipped laboratories in all departments

MREC (A) has more than 100 doctorates with good Research work.

## Advisory Committee:

**Chief Patrons**: **Sri. Ch. Malla Reddy, Minister-Telangana State-India.**
Founder Chairman,
**Malla Reddy Group of Institutions.**

**Patrons:** **Sri.Ch. Mahender Reddy.**
Secretary, MRGI.
**Dr.Ch.Bhadra Reddy,**
President, MRGI.

**Co-Patrons:** **Dr. A. Ramaswami Reddy**
Principal, MREC (A).

**Convener:** **M. Jagdeesh Chandra Prasad**
**HOD ECE.**

**Co-ordinator: Dr. S. K. Fairoz,**
**Assoc. Professor, ECE.**

## Organizing Committee:

Dr.G.S.K.Gayathri Devi, Assoc. Prof., ECE.
Mr G Prasanna Kumar Assoc . Prof., ECE.
Dr. M.Nithin Varma Asst.Prof.,ECE
Mrs.C.Silpa, Assoc. Prof., ECE.
Dr A Pradeep Kumar,, Assc. Prof., ECE
Dr T Srinivas Reddy, Assoc. Prof., ECE.
Mr. J. Sunil Kumar,Asst.Prof.,ECE
Mr.Vutkuri Srinivas, Asst.Prof.,ECE
Mr. M.Kranthi Kumar, Asst.Prof.,ECE
Mrs. G.Jyothi,Asst.Prof.,ECE

**5-days Value Added Course**

**on**

**" VLSI Design and Verification "**

**From 17th to 21th January 2022**

*Organized by*

**Department of**

**Electronics and Communication Engineering**

**MALLA REDDY ENGINEERING COLLEGE**

**(AUTONOMOUS) MAIN CAMPUS**

**An UGC Autonomous Institution, Approved by AICTE & Affiliated to JNTUH-Hyderabad**
**Reaccredited by NAAC with 'A' Grade (II Cycle)**
**Maisammaguda(H), Gundlapochampally (V), Medchal (M), Medchal - Malkajgiri District Telangana - 500100, India.**

## About the Department:

The Department of Electronics and Communication Engineering at MREC has been producing high quality technical manpower needed by industry, R&D organizations, and academic institutions since 2002 with an Intake of 60. The intake has been increased to 120 in the year 2004-05 and 180 in the year 2013-14.The Department also offering PG Program **VLSI and Embedded Systems.** The department UG Program was accredited by NBA in 2008 and Re-accredited in 2014 and 2018.

Electronics and Communication Engineering department is now headed by **Dr. M. Jagdeesh Chandra Prasad** Department maintaining 1:15 student faculty ratio with enough faculty retention. Total 30% of doctorates available in the department. Faculty Publications are 150, Patents-5, sanctioned UGC Minor Project, AICTE (AQIS) sponsored MODROB & FDP and Consultancy projects-4.Applied projects for research grants under AQIS, CRG.

Many of our students are placed in reputed companies like INFOSYS, IBM, AMAZON, Tech-Mahindra, TCS, COGNIZANT and many more. Apart from teaching department also provides technical guidelines for the benefits of students by organizing short-term courses, certificate oriented training, seminars, Guest lectures, workshops, national and international conferences.

## About Workshop

**PROGRAMME OBJECTIVE** The aim of this workshop is to provide an overview on EDA tools for VLSI design to the participants. The workshop will comprise of live demonstration of tools and lectures delivered by design engineers on platforms like Cadence, Mentor Graphics, Xilinx, and Synopsys Sentaurus TCAD. This workshop is a generous attempt of qualified VLSI domain researchers to help and encourage the research scholars, undergraduate, postgraduate, and entrepreneurs to meet their research goals. The participants will have exposure to the state-of-the-art semiconductor devices to circuit modeling and integrated applications. After finishing this workshop, the participants will be able to execute the various analysis needed to characterize devices and circuits individually.

## PROGRAMME CONTENTS

- Introduction to MOS transistor and 3D TCAD tool
- Design flow using Synopsis tool
- Full custom design using trainer EDA and Mentor tool
- Xilinx FPGA design flow
- PYNQ platform with Vivado

## *Registration Form*

**5-days Value Added Course**

**on**

**" VLSI Design and Verification "**

**From 17th to 21th January 2022**

**Name:**_____

**Roll Number**_____

**Department:**_____

**Organization:**_____

**Address:**_____

_____

_____

**Mobile No:**_____

**E-mail ID:**_____

**Signature of the Candidate:**_____

**OR**

Interested students are can register using below link

**https://forms.gle/M91WTujRUdPknyPq5**

**Note: Certificate will be provided for the participants on feedback submission, 80% attendance.**

**Registration Fee :**

**1000** Rs registration fee will be charged for attending this programme.

**MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)**
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Maisammaguda (H), Medchal-Malkajgiri District, Telangana State – 500100

**DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING**

Value Added Course
on
"VLSI Design and Verification"

17th -21th Jan 2022
**Programme Schedule**

| Date | Time | Topic | Resource Person |
|---|---|---|---|
| 17.01.2022 | 9:30 – 4.00 pm | Introduction to MOS transistor and 3D TCAD tool | Mr. N Ravi Shankar |
| 18.01.2022 | 9:30 – 4.00 pm | Design flow using Synopsis tool | Mr. N Ravi Shankar |
| 19.01.2022 | 9:30 – 4.00 pm | Full custom design using trainer EDA and Mentor tool | Mr. N Ravi Shankar |
| 20.01.2022 | 9:30 – 4.00 pm | Xilinx FPGA design flow | Mr. N Ravi Shankar |
| 21.01.2022 | 9:30 – 4.00 pm | PYNQ platform with Vivado | Mr. N Ravi Shankar |

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Maisammaguda (H), Medchal-Malkajgiri District, Telangana State – 500100

## DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Value Added Course on "**VLSI Design and Verification**"

17th -21th Jan 2022

# Syllabus

## Day 1

- Introduction to Non-Classical MOS Transistor
- Live demonstration of device simulation and analysis using Synopsys Sentaurus 3D TCAD tool

## Day 2

- Physical Insights into the nature of Gate-induced Drain Leakage in Emerging Nano-scale FETs
- ASIC and full-custom design flow using Synopsys tool

## Day 3

- BACK-END design flow, generation of GDS-II, and use of Fin-FET library in Cadence
- Static timing analysis using Tempus and clock tree synthesis concept in Cadence
- Demonstration of full-custom design using Tanner EDA and Mentor tool

## Day 4

- Xilinx FPGA design flow
- Demonstration on system generator flow with Matlab

## Day 5

- Demonstration on PYNQ platform with Vivado
- Introduction to HDL Verification and UVM
- Learn to build UVM testbench from scratch

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|---|---|---|

Department of Electronics and Communication Engineering

Academic Year 2021-2022

Name of the Value Added Course: VLSI Design and Verification

## List of Students enrolled for value added course

| Sl. No. | Roll No. | Name | Year/Semester |
|---|---|---|---|
| 1 | 21J41D6801 | UJJELLI RAKESH REDDY | M. Tech I/I |
| 2 | 21J41D6802 | PONNA SNEHA | M. Tech I/I |
| 3 | 21J41D6803 | TAGORE SANJANA | M. Tech I/I |
| 4 | 21J41D6804 | M. INDRANI SOWMYA | M. Tech I/I |
| 5 | 21J41D6805 | PAMPARI SRAVANTHI | M. Tech I/I |
| 6 | 21J41D6806 | NAGAM SHRAVYA | M. Tech I/I |
| 7 | 21J41D6807 | JANGILI SAIKIRAN | M. Tech I/I |
| 8 | 21J41D6808 | BALERAO CHOUDARY MANISH | M. Tech I/I |
| 9 | 21J41D6809 | KONATHAM MOUNIKA | M. Tech I/I |
| 10 | 20J41D6801 | AARADHANA | M. Tech II/I |
| 11 | 20J41D6803 | BOLLIBATULLA SHIVA TEJA | M. Tech II/I |
| 12 | 20J41D6807 | HARI BABU J | M. Tech II/I |
| 13 | 20J41D6808 | KALAPALLI ABILASH | M. Tech II/I |

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Maisammaguda (H), Medchal-Malkajgiri District, Telangana State – 500100

# DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Value Added Course: VLSI Design and Verification

Date: 21/01/ 2022

## Objective Questions

1. VLSI technology uses _____ to form integrated circuit.
a) transistors
b) switches
c) diodes
d) buffers

2. Medium scale integration has _____
a) ten logic gates
b) fifty logic gates
c) hundred logic gates
d) thousands logic gates

3. The difficulty in achieving high doping concentration leads to _____
a) error in concentration
b) error in variation
c) error in doping
d) distribution error

4. _____ is used to deal with effect of variation.
a) chip level technique
b) logic level technique
c) switch level technique
d) system level technique

5. As die size shrinks, the complexity of making the photomasks _____
a) increases
b) decreases
c) remains the same
d) cannot be determined

6. _____ architecture is used to design VLSI.
a) system on a device
b) single open circuit
c) system on a chip
d) system on a circuit

7. What is the design flow of VLSI system?
i. architecture design
ii. market requirement
iii. logic design
iv. HDL coding
a) ii-i-iii-iv
b) iv-i-iii-ii
c) iii-ii-i-iv
d) i-ii-iii-iv

8. _____ is used in logic design of VLSI.
a) LIFO
b) FIFO
c) FILO
d) LILO

9. Which provides higher integration density?
a) switch transistor logic
b) transistor buffer logic
c) transistor transistor logic
d) circuit level logic

10. Physical and electrical specification is given in _____
a) architectural design
b) logic design
c) system design
d) functional design

11. Which is the high level representation of VLSI design?
a) problem statement
b) logic design
c) HDL program
d) functional design

12. Gate minimization technique is used to simplify the logic.
a) true
b) false

13. Depletion mode MESFET operates as
a) reverse biased

b) forward biased
c) both reverse and forward biased
d) none of the mentioned

14. Pinch-off voltage is equal to
a) built-in potential
b) applied voltage
c) sum of built-in potential and applied voltage
d) difference of built-in potential and applied voltage

15. Pinch-off voltage is a function of
a) channel depth
b) channel thickness
c) channel length
d) channel density

16. The threshold voltage is sensitive to
a) channel length
b) channel depth
c) doping density
d) doping of the channel layer

17. The dynamic switching energy must exceed the capacitive load.
a) true
b) false

18. To keep dynamic switching energy small
a) logic voltage swing must be large
b) logic current swing must be large
c) logic voltage swing must be small
d) logic current swing must be small

19. Standard deviation of threshold voltage should be _____ of logic voltage swing.
a) less than 5%
b) more than 5%
c) less than 10%
d) more than 10%

20. In D-MESFET, voltage swing is less than 1V.
a) true
b) false

21. Threshold voltage is _____ on implant depth.
a) proportionally dependent
b) inversely proportionally dependent
c) exponentially dependent

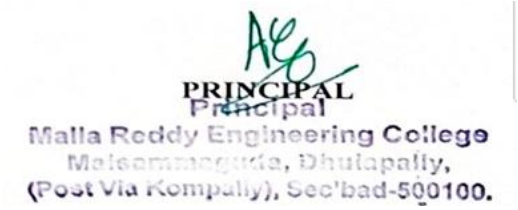
d) logarithmically dependent

22. The drain current is independent of
a) Vgs
b) Vds
c) Vt
d) Vs

23. Impurity concentration should be
a) greater than 20%
b) lesser than 20%
c) greater than 10%
d) lesser than 10%

24. Threshold voltage is independent of pinch-off voltage.
a) true
b) false

25. Pinch-off voltage is _____ to channel concentration density.
a) directly related
b) inversely related
c) exponentially related
d) is not related

| | | |
|---|---|---|
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Department of Electronics and Communication Engineering

Academic Year 2021-2022

Name of the Value Added Course: **VLSI Design and Verification**

## List of Students completed course

| Sl. No. | Roll No. | Name | Course Completion (Yes/No) |
|---|---|---|---|
| 1 | 21J41D6801 | UJJELLI RAKESH REDDY | Yes |
| 2 | 21J41D6802 | PONNA SNEHA | Yes |
| 3 | 21J41D6803 | TAGORE SANJANA | No |
| 4 | 21J41D6804 | M. INDRANI SOWMYA | Yes |
| 5 | 21J41D6805 | PAMPARI SRAVANTHI | Yes |
| 6 | 21J41D6806 | NAGAM SHRAVYA | Yes |
| 7 | 21J41D6807 | JANGILI SAIKIRAN | Yes |
| 8 | 21J41D6808 | BALERAO CHOUDARY MANISH | Yes |
| 9 | 21J41D6809 | KONATHAM MOUNIKA | Yes |
| 10 | 20J41D6801 | AARADHANA | Yes |
| 11 | 20J41D6803 | BOLLIBATULLA SHIVA TEJA | Yes |
| 12 | 20J41D6807 | HARI BABU J | Yes |
| 13 | 20J41D6808 | KALAPALLI ABILASH | Yes |

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Maisammaguda (H), Medchal-Malkajgiri District, Telangana State – 500100

**Department of Electronics and Communication Engineering**

Date: 21.01.2022

# Report for value added course on

# VLSI Design and Verification

A Five days VLSI Design and Verification programme was organized by the Department of Communication Engineering, and the event was coordinated by Dr. S. K. Fairoz, Associate Professor, ECE Department from 22 Jan. 2022 to 21 Jan. 2022 and 13 students were attended from M.Tech VLSI. The resource person for this course is V. Kiran Kumar. The quality of life for the students are enhanced by introspect and learn techniques that imbibe ethics and moral to help the students for active and successful participation in a modern society, producing individuals of high character, probity, and honor.

After the training programme, the students learned the following:

- Fundamental knowledge on VLSI Design
- Design flow using Xilinx and FPGA
- Acquired the knowledge on Vivado and system generator flow with Matlab

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**Department of Electronics and Communication Engineering**

# *Certificate of Completion*

This is to certify that Mr./Ms. **BALERAO CHOUDARY MANISH** bearing roll no. **21J41D6808** has successfully completed Value Added Course in "VLSI Design and Verification" organized by Department of Electronics and Communication Engineering from 17/01/2022 to 21/01/2021.

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Maisammaguda, Dhullapally,

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**Principal MREC**

# MALLA REDDY ENGINEERING COLLEGE

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Maisammaguda (H), Medchal-Malkajgiri District, Secunderabad, Telangana – 500100.

**Department of Electronics and Communication Engineering**

# *Certificate of Completion*

This is to certify that Mr./Ms. **BOLLIBATULLA SHIVA TEJA** bearing roll no. **20J41D6803** has successfully completed Value Added Course in "VLSI Design and Verification" organized by Department of Electronics and Communication Engineering from 17/01/2022 to 21/01/2021.

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Maisammaguda (H), Medchal-Malkajgiri District, Telangana State – 500100

**Department of Electronics and Communication Engineering**

Title of the Session: VLSI Design and Verification.

Department: ECE

Date of the Session: 17.1.2022 to 21.01.2022

| Sl No. | | Excellent | Very Good | Good | Average |
|---|---|---|---|---|---|
| 1 | The session objectives were stated clearly and met | | | ✓ | |
| 2 | The Workshop was well organized | | | ✓ | |
| 3 | The information and/or skills presented were relevant and useful for career | | | ✓ | |
| 4 | The presenter responded to questions effectively? | | | | ✓ |
| 5 | The overall assessment of the Session | | | | ✓ |
| 6 | The session content met your expectation | | | ✓ | |

Excellent:4 Very Good:3 Good:2 Average:1

Suggestions if any:

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Maisammaguda (H), Medchal-Malkajgiri District, Telangana State – 500100

**Department of Electronics and Communication Engineering**

Title of the Session: VLSI Design and Verification.

Department: Electronics & communicat Engg.

Date of the Session: 17.01.2022 to 21.01.2022.

| Sl No. | | Excellent | Very Good | Good | Average |
|---|---|---|---|---|---|
| 1 | The session objectives were stated clearly and met | | ✓ | | |
| 2 | The Workshop was well organized | | ✓ | | |
| 3 | The information and/or skills presented were relevant and useful for career | ✓ | | | |
| 4 | The presenter responded to questions effectively? | ✓ | | | |
| 5 | The overall assessment of the Session | ✓ | | | |
| 6 | The session content met your expectation | | | ✓ | |

Excellent:4 Very Good:3 Good:2 Average:1

Suggestions if any: