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An Adjustable DC Link Voltage Based Control of Multifunctional Grid Interfaced Solar Enegry PV System

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***Abstract*— This paper presents a grid supported solar energy conversion system with an adjustable DC link voltage for CPI (Common Point of Interconnection) voltage variations. A two stage circuit topology is proposed wherein; the first stage is a boost converter which serves for MPP (Maximum Power Point) tracking and the second stage is a grid tied VSC (Voltage Source Converter), which not only feeds extracted solar photovoltaic energy into the three phase distribution system but also serves for harmonics mitigation, reactive power compensation and grid currents balancing. An interweaved DFSOGI (Double Frequency Second Order Generalized Integrator) based control algorithm is proposed for control of this multifunctional VSC which possesses the feature of good steady state performance along with fast dynamic response even under sudden load changes at CPI. Moreover, a feed-forward term for the solar PV contribution is used to enhance the dynamic response for climatic changes and CPI voltage variation. An adjustable DC link voltage structure is used to accommodate CPI voltage variation which helps in reduction of losses in the power circuit. To implement adjustable DC link voltage structure, the reference DC link voltage is adjusted with variation in CPI voltage in real time. A PI (Proportional-Integral) controller is used to regulate DC link voltage to set reference value. A wide range of experimental results are shown to demonstrate the features of proposed system. The THD (Total Harmonics Distortion) of grid current has been found well under IEEE-519 standard even under nonlinear loads at CPI.**

***Index Terms*— Solar PV; Adjustable DC link; DFSOGI; Power Quality, Under voltage; Over voltage**

I. INTRODUCTION

The rapidly vanishing conventional energy sources (fossil fuels) have put an alarming energy crisis situation in front of the world. Moreover, the deteriorating environmental conditions have moved world's attention towards nonconventional green energy sources. The solar energy has provided a new cost feasible alternative. The grid parity for solar energy conversion systems have been shown in [1]-[2].

Solar PV (Photovoltaic) energy generation systems can be broadly classified into two main categories which are standalone and grid interfaced. Several standalone systems for PV power generation systems considering rural electrification, three port converters for PV application, PV based battery charging station and battery energy management are shown in [3]-[6]. The batteries are integral part of standalone PV based system. However, they require frequent maintenance and timely replacement. Therefore, battery-less grid interfaced PV generation systems are more preferred where the grid is available.

The initial investment to setup a PV plant is high because of high cost of PV panels. Hence the aim is to extract maximum power from available capacity once a PV plant is installed. Several MPPTs (Maximum Power Point Techniques) are proposed in the literature [7]-[9]. The classification and basic concept of MPPT algorithms used in PV applications are shown in [7]. A power plane analysis of V-I characteristics is shown in [8]. The incremental conductance based algorithm is simple and easy to implement. A variable step incremental conductance (InC) MPPT technique is shown in [9]. In this paper, a combination of InC and fractional open circuit voltage (V_{OC}) MPPT algorithm is used which is named composite InC algorithm.

The power electronic converters based nonlinear loads are increasing in the distribution system. The nonsinusoidal current by these loads causes problems such as voltage distortion, increased distribution loss, derating of distribution equipment etc. In order to solve these power quality problems, several retrofit solutions are proposed by researchers such as passive filter, active filters, DSTATCOM (Distribution Static Compensator) etc [10]-[17].

The SRF (Synchronous Reference Frame) based control algorithm for active power filters have been proposed in [12]-[14]. The SRF based control algorithm provides an advantage that all three phase load currents are processed simultaneously. The DC component of direct axis current corresponds to uniformly distributed average power consuming component of load current. Therefore, only one low pass filter is required to estimate DC component of direct axis current. However, in case of unbalanced operation, the second harmonic is the dominant component in the direct axis current. In order to achieve good steady state response under unbalanced operation, the cut off frequency for low pass filter is to be set very low. However, the low cutoff frequency causes poor dynamic response. Therefore, there is a tradeoff between steady state and dynamic performances in SRF based control approach.

Various advanced control approaches for DSTATCOM have been proposed to solve this tradeoff under unbalanced operation [15]-[17]. A learning based antihebbian based control approach is shown in [15]. A neural network based conductance estimation based control approach is shown in [16]. A back propagation based control approach is shown in

[17] .In all these control approaches, the load respect to CPI voltage variation. The adjustable DC link voltage not only helps in reduction of switching losses in all the power devices (the VSC and the boost converter) but also processed through an advanced filtering scheme for estimation of average power consuming component of load current. Since all three phase load currents are processed separately in the VSC control approach, three such filters are required (one for each phase). However, in this paper an interweaved DFSOGI (Double Frequency Second Order Generalized Filter) based control approach is proposed which solves the tradeoff between steady state and dynamic performances, while processing all three load currents together.

The shunt grid tied VSCs (Voltage Source Converters) are used in many applications. For proper control of output currents of the VSC, the DC link voltage of the VSC is kept constant (higher than peak of maximum allowable line voltage) [10]-[17]. Most of these researchers have shown operation of the grid tied system for constant CPI (Common Point of Interconnection) voltage. However, in case of weak distribution system, a wide voltage variation is observed. During peak loading condition, a sustained voltage dip or under voltage is observed commonly and in night time when the loading of the distribution system is low, the over voltages are observed. The practical range of voltage variation is about ±15 % of nominal voltage. In this paper, the operation of the complete system is shown for practical range of voltage variation and the control approach is appropriately modified for improved performance under this range of voltage variation.

The use of two stage generation system for solar photovoltaic systems has been proposed by several researchers [18]-[20]. Conventionally, a DC-DC converter is used as first stage which serves the purpose of MPPT. The second stage is a grid tied VSC which feeds the power into the distribution system. A single phase two stage grid tied PV generation system with constant DC link voltage is shown in [18]. Moreover, the three phase grid tied PV generation system with constant DC link voltage control is also shown in [19]-[20]. The DC link voltage of VSC is kept constant (higher than peak of maximum allowable line voltage) using a PI controller [19]-[20].

In this paper, a two stage multifunctional solar energy conversion system is proposed which not only feeds the solar energy into the distribution system but also serves the purpose of harmonics mitigation, reactive power compensation and grid currents balancing at the same time. The utilization factor of the grid tied VSC is better as it also serves for power quality improvement in night time. An interweaved DFSOGI based control algorithm is proposed to serve all aforementioned purposes. The interweaved DFSOGI algorithm is a combination of SRF [12]-[14] and SOGI (SOGI Second Order Generalized Filter) [21] based algorithm. A wide variety of results are shown to demonstrate the performance of interweaved DFSOGI based control in. algorithm.

Moreover, unlike previous work with constant DC link voltage, an adjustable DC link voltage based control approach is proposed here. The DC link voltage of VSC is adjusted with The concept of loss reduction by adjusting DC link voltage for VSC in hybrid filters is shown in [22]-[23] wherein, reactive power requirement of the filter is satisfied by adjusting the DC link voltage. A three-phase PV inverter with adjustable DC link voltage is shown in [24]. A single-phase solar based system with adjustable DC link voltage is demonstrated in

[25]. However, all these systems are different from point of view of circuit topology. Therefore, there is a wide difference in work presented in [22]-[25] and the proposed work. The main contributions of this work can be listed as,

1. The use of interweaved DFSOGI with d-q reference based control approach to overcome the drawbacks of SRF, which enables fast dynamic response along with better steady state accuracy.
2. Formulation of an approximate linear model of DC link voltage control structure considering the effect of feed-forward terms for load contribution and PV array contribution and an assessment of DC bus control structure demonstrating the need and requirements for the feed-forward compensation.
3. An implementation of an adaptive DC link voltage based control structure for multitasking solar energy conversion system which helps in reduction of switching losses and high frequency ohmic losses (verified experimentally). Moreover, it also reduces high frequency ripple content in grid currents.

Moreover, it should be noted that the stress on the power circuit (power semiconductor devices, DC link capacitor etc) remains same in both proposed and conventional systems, considering the fact that these ratings are decided assuming worst case scenario, which is same in both the cases. Hence, while using the same hardware resources, an increased energy output is observed with the system using proposed DC link voltage control approach.

II. System Configuration

The system configuration for proposed two stage circuit topology is shown in Fig. 1. The proposed system consists of a solar photovoltaic array, a boost converter, a three phase VSC, interfacing inductors, ripple filter, a three-phase distribution system and some local loads. The three-phase distribution system, local loads and VSC are connected at one CPI. The PV array is connected at the input of the boost converter. The output of boost converter is connected to the DC link of the VSC. The boost converter serves the purpose of extraction of maximum power from the PV array and it feeds the extracted energy to the DC link of the VSC. The three phase VSC is tied to the distribution system via interfacing inductors. A small ripple filter is also connected at CPI to absorb the switching

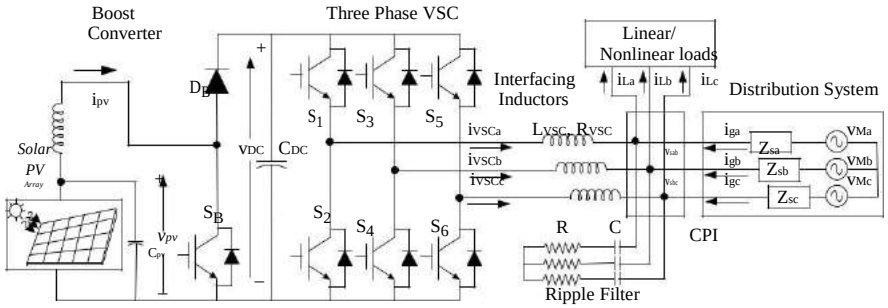


Fig. 1 System Configuration

III. Control Approach

Fig. 2 shows the detailed block diagram of proposed control approach. There are two main power circuits in the proposed circuit topology. The duty ratio for boost converter is decided on the basis of MPPT control algorithm. The input voltage of boost converter is continuously adjusted such that the PV array operates at MPP. The output of boost converter is connected to the DC link of the VSC. The DC link voltage of the VSC is adjusted in real time considering the CPI voltage. Therefore, with the proposed control approach, both input and output voltages of boost converter are adjusted in real time. Moreover, the VSC is controlled such that the grid deals with only real power exchanges even when local load demands reactive power or harmonics. The proposed control algorithm also presents a solution for balancing grid currents. Hence, the currents injected by the VSC are controlled such that the grid currents are always balanced sinusoids at unity power factor. The detailed explanation for control algorithm of the two main power circuit is given below.

A. Maximum Power Point Tracking

A composite InC based MPPT algorithm is used. A range of voltage for peak power is known with the knowledge from fractional Voc MPPT which is $0.7V_{ocmax}$ to $0.9V_{ocmax}$, where Voc is open circuit voltage and V_{ocmax} is maximum open circuit voltage. The voltage for peak power is always searched in this range for fast search of V_{mpp}. The InC algorithm works in order to minimize the difference between the incremental conductance and the conductance offered by the PV array. At first, the reference PV array voltage is estimated based on the InC principle then that reference voltage is used to estimate the duty ratio of boost converter. For calculation of incremental conductance ΔI_{PV} and ΔV_{PV} are estimated as,

$$\Delta I_{PV} = I_{PV}(k) - I_{PV}(k-1) \quad (1a)$$

$$\Delta V_{PV} = V_{PV}(k) - V_{PV}(k-1) \quad (1b)$$

where I_{PV} (k) and V_{PV} (k) are the instantaneous sampled current and voltage of the solar array.

The governing equations for InC based MPPT algorithm is as,

$$\frac{\Delta I_{PV}}{\Delta V_{PV}} = \frac{-I_{PV}}{V_{PV}}, \text{at MPP} \quad (2a)$$

$$\frac{\Delta I_{PV}}{\Delta V_{PV}} > \frac{-I_{PV}}{V_{PV}}, \text{Left of MPP on } P_{PV} \text{ v/s } V_{PV} \text{ curve} \quad (2b)$$

$$\frac{\Delta I_{PV}}{\Delta V_{PV}} < \frac{-I_{PV}}{V_{PV}}, \text{Right of MPP on } P_{PV} \text{ v/s } V_{PV} \text{ curve} \quad (2c)$$

The reference PV voltage and sensed DC link voltage are then used to estimate the duty ratio for the boost converter. The governing equation for estimating duty ratio is,

$$D_{ref}(k) = 1 - \frac{V_{PVref}(k)}{V_{DC}(k)} \quad (3)$$

This reference duty ratio is used to generate switching logic for boost converter.

B. Control Approach for Three-Phase VSC

The three phase VSC is controlled to achieve the objective of reactive power compensation, harmonics mitigation, grid currents balancing and regulation of DC link voltage to desired adjustable reference value. A total of nine quantities are sensed to control the SECS, which are line voltages (v_{sab} and v_{sbc}), DC link voltage (v_{DC}) and grid currents (i_{ga} and i_{gb}), load currents (i_{La} and i_{Lb}), PV array voltage (v_{PV}) and PV array current (i_{PV}). The phase voltages are estimated from the sensed line voltages and then the synchronization signals are estimated from the phase voltages. To estimate the synchronization signals at first amplitude of phase voltages is estimated. The amplitude of phase voltages is estimated as,

$$V_z = \sqrt{\frac{2(v_{sa}^2 + v_{sbsc}^2)}{3}} \quad (4)$$

This amplitude is used to determine the synchronization signals of CPI voltage which contains the phasor information of all phase voltages. The synchronization signals are estimated as,

$$z_a = \frac{v_{sa}}{V_z}, z_b = \frac{v_{sb}}{V_z}, z_c = \frac{v_{sc}}{V_z} \quad (5)$$

The control objective for the VSC is to maintain the grid currents balanced sinusoids at unity power factor. To achieve the aforementioned objective, the peak of grid currents is estimated, which is common for all three phases. The grid current consists of three main parts, which are average power consuming component of load current, PV array contribution and losses of the SECS. The average power consuming component of load current is estimated using interweaved DFSOGI based control algorithm. At first the direct axis component (i_d) of three phase load currents is estimated. T

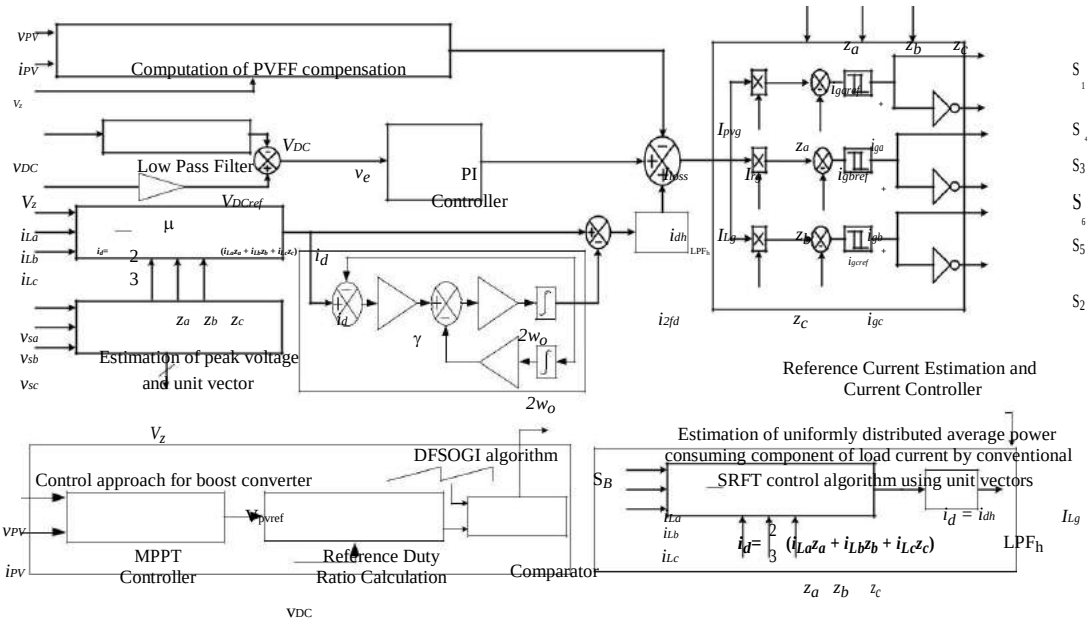


Fig. 2 Block diagram for control approach.

The average value of direct axis component (I_{Lg}) represents the average power consuming component of load current distributed uniformly in all three phases. In order to estimate the I_{Lg} conventionally i_d is passed though a low pass filter as shown in Fig. 2.

The cut off frequency of low pass filter depends on several aspects related to nature of the load. In case the load currents are balanced sinusoidal, the i_d is a DC value which can directly be used without used as I_{Lg} and without using a low pass filter. However, in case the load currents are balanced and nonsinusoidal (representing balanced nonlinear load), the i_d consists of a DC with superimposed ripple component corresponding to load current harmonics, then in order to estimate I_{Lg} the i_d is passed though a low pass filter. The cut off frequency of low pass filter is decided by lowest order ripple frequency in i_d. In case of three-wire balanced nonlinear load the 5^{th} and 7^{th} harmonic are the lowest order harmonics in the load currents. The lowest order ripple frequency is 6^{th} as the 5^{th} harmonics is positive sequence and 7^{th} harmonic is negative sequence. A low pass filter tuned to line frequency can be used to suppress this ripple.

In case of unbalanced load currents, the second harmonic component is the dominant part of i_d. In order to suppress the dominant second harmonic component, conventionally a low pass filter with a low cut off frequency is used. However, the dynamic response for estimation of I_{Lg} is adversely affected by reduction of cut off frequency. Hence, there is a compromise between the steady state and the dynamic performances of conventional SRFT in case of unbalanced loads at CPI.

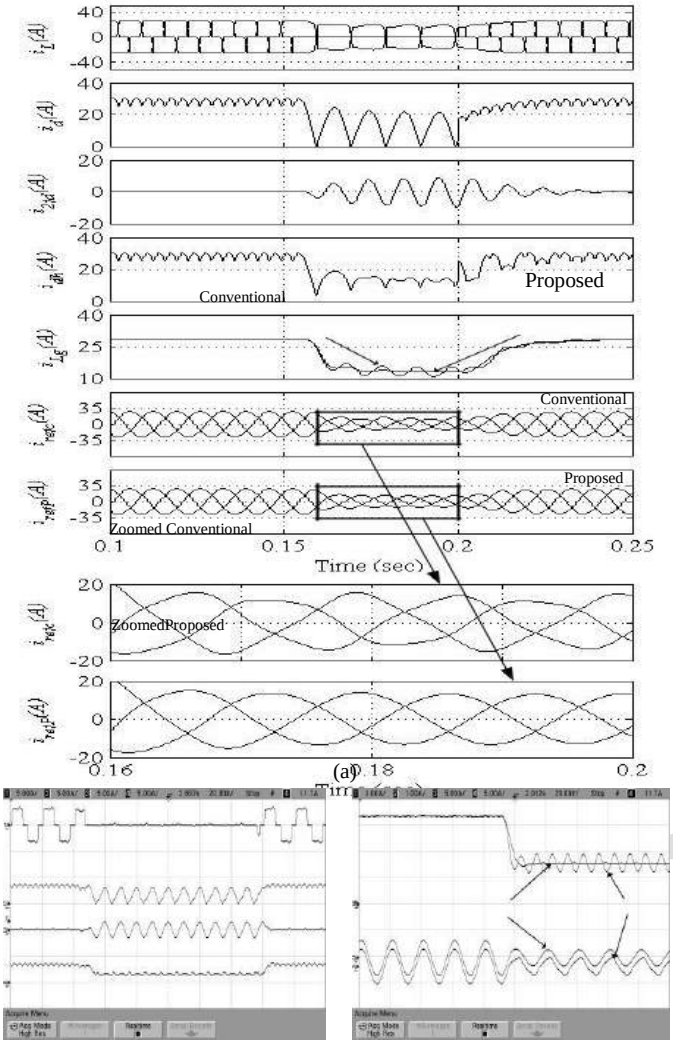
The proposed interweaved DFSOGI based control algorithm provides a solution to tradeoff between steady state and dynamic performances. DFSOGI based control algorithm is interwoven with direct axis current control based algorithm such that the double frequency component of i_d quashed separately. The estimation of double frequency component with DFSOGI is given as,

$$\frac{I_{2fd}(s)}{I_d(s)} = \frac{2\gamma\omega_0 s}{s^2 + 2\gamma\omega_0 s + \omega_0^2} \quad (6)$$

where ω_o is the nominal line frequency and γ is the convergence factor. The second harmonic component present in the i_d is subtracted in real time. The resultant value is designated as i_{dh}, which is then passed though a low pass filter to suppress ripple component corresponding to harmonics in load current. However, the cutoff frequency for low pass filter can be kept comparatively higher, as the dominant second harmonic component is already quashed by interweaved DFSOGI algorithm.

Fig. 3 shows the comparison of the proposed interweaved DFSOGI based algorithm with conventional SRF algorithm. Fig. 3 (a) shows simulated steady state and dynamics performances. In Fig. 3 (a), it can be observed that before time t = 0.15 s, the loads are balanced and nonlinear hence i_d contains only high frequency ripples corresponding to load current harmonics. However at t = 0.15 s, when one of the load line is opened, the load currents are unbalanced. The i_d for unbalanced load contains large second harmonic component along with average DC value. The DFSOGI is used to detect and quash double harmonic component separately. The I_{Lg} represents the uniformly distributed average power consuming component of load current. It can be easily observed that the I_{Lg} estimated by DFSOGI based algorithm is quite smooth as compared to that of conventional SRF algorithm. The effects of oscillations in the I_{Lg} on the corresponding component of

(b) shows experimentally captured internal signals. The experimental results are consistent with simulation results.



i_{Lc} 5 A/div

i_d 5 A/div Hall

i_{2fd} 5 A/div

i_{dh} 5 A/div

$$I_{PVg} = \frac{(2V_{PV} I_{PV})}{(3V_z)} \quad (7)$$

voltage is kept fixed at set reference value, the proposed algorithm adjusts reference DC link voltage according to sensed CPI voltage. The performance improvement by keeping the adjustable reference for DC link voltage has been verified experimentally and is discussed in section V. The reference DC link voltage is estimated as,

$$v_{DCref} = \mu\sqrt{3V_Z}, \text{ where } \mu>1 \quad (8)$$

For proper current control the DC link voltage must be higher than the amplitude of CPI line voltage. Therefore, reference DC link voltage is kept around 10 % higher than the peak of CPI line voltage, considering the drop across switches, interfacing inductor, resistance of interfacing inductor and proper current control under DC link voltage dynamics. Hence, the selected value of μ in the proposed work is 1.1.

The sensed DC link voltage is passed through a low pass filter to suppress the switching noise. The output of low pass filter is designated as V_{DC}. A PI controller is used to regulate the DC link voltage to the desired reference value. The governing equation for PI controller is as,

$$( ) \quad ( ) \quad \{ ( ) \quad ( )\} \quad ( ) \quad (9)$$

The grid currents are assumed coming out from equivalent voltage source, hence considering the direction of grid currents, the load power and the losses are drawn from the grid whereas the PV contribution is fed into the grid. Therefore, net amplitude of grid current is estimated as,

$$I_{rg} = I_{Lg} + I_{loss} - I_{PVg} \quad (10)$$

The reference grid currents are estimated using synchronizing unit vectors and the estimated peak of reference grid currents. The mathematical expression for estimation of the reference grid currents are as,

$$i_{garef} = I_{rg} z_a, i_{gbref} = I_{rg} z_b, i_{gcref} = I_{rg} z_c \quad (11)$$

An indirect current control is used in the proposed control approach wherein the estimated reference grid currents are compared with sensed grid currents and based on polarity of error in each sampling time, the switching logic for VSC is decided.

IV. Results and Discussion

Test results are shown in Figs. 4-12. A total of nine quantities are sensed which are v_{pv}, i_{pv}, v_{DC}, v_{sab}, v_{sbc}, i_{ga},i_{gb}, i_{La}, i_{Lb}. The Effect voltag (LV-25) and current sensors (LA-55p) are used to sense voltages and currents. The sensed signals are conditioned and given to ADC (Analog to Digital Converter) of processor (DSP-dSPACE-1103). The outputs from processor are the switching logics for all controlled switches. These results are captured using power analyzer (Fluke 43B) and a four channel digital storage oscilloscope (DSO6010A). Test results are categorized in three sections which are steady state results, dynamics and performance improvement with adjustable DC link control approach. The salient system parameters for implementation purpose are given bel

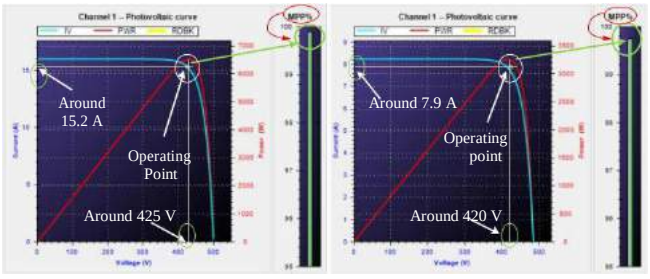
balanced three-phase 1.31 kW. ripple filter R = 5 Ω, C = 5μF, K_p= 0.4, K_i =0.1, DFSOGI parameters: ω_0 = 314, γ = 0.2, cut off frequency for LPF_h of DFSOGI and SRF = 50 Hz, Cut off frequency of DC link LPF = 500 Hz, PV array maximum open circuit voltage: 500 V, PV array maximum short circuit current: 16 A, PV array peak power: approximately 6 kW.

A. Steady State Performance

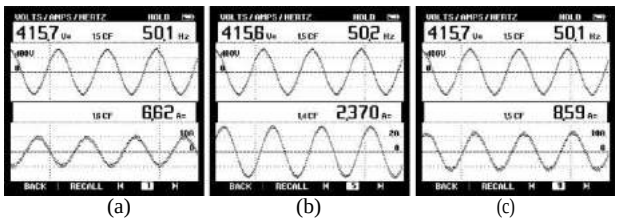
The steady state performance for MPPT is shown in Fig. 4, which is recorded from PV array simulator. The MPP efficiency is around 99.7% for both the insolation levels (1000 W/m^2 and 500 W/m^2).

The steady state performance for reactive power compensation for balanced linear load is shown in Fig. 5. Figs. 5 (a)-(c) show the CPI voltage (v_{sab}) with grid, load and VSC currents. As under balanced loading condition, the three phase currents for all the phases are equal hence only one phase quantities are shown. The reactive power compensation can be observed form Figs. 5 (d)-(f). Fig. 5 (d) shows the power taken from the grid. Fig. 5 (e) shows the load power which is at pf of 0.8 lag. It can be observed that sign for power absorbed from the grid is negative and the DPF (Displacement Power Factor) is -1 which shows that power is being supplied to the grid at unity power factor. Fig 5 (f) shows the power supplied by the VSC. The power supplied by the VSC is divided between load and grid.

Fig. 6 shows the performance of the SECS under unbalanced nonlinear load at CPI. Figs. 6 (a)-(c), Figs. 6 (d)-(f), Figs. 6 (g)-(i) show v_{sab} with three phase grid, load, VSC currents respectively. It can be observed that load currents for phase "a" and "b" are nonsinusoidal and for that of phase "c" is zero, which shows that the load is nonlinear and unbalanced. However, the grid currents (as shown in Figs. 6 (a)-(c)) are balanced (can be observed from magnitude) and sinusoidal. The VSC currents are so adjusted that the grid currents are balanced and sinusoidal. Figs. 6 (j)-(l) show the harmonics spectra of grid load and VSC currents. The THD of load current is 21.8 % however that of grid current is of order of 2%. The THD of VSC current is higher as compared to grid current as it consists of load current harmonics. The power supplied by the grid and power absorbed by the load are given in Figs. 6 (m)-(n). The power supplied by the grid is negative which shows power is being supplied into the grid.

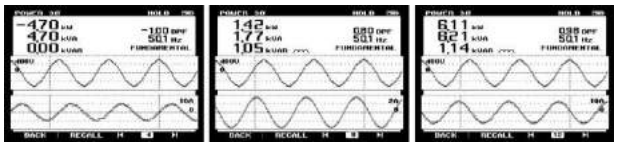


(a) (b)



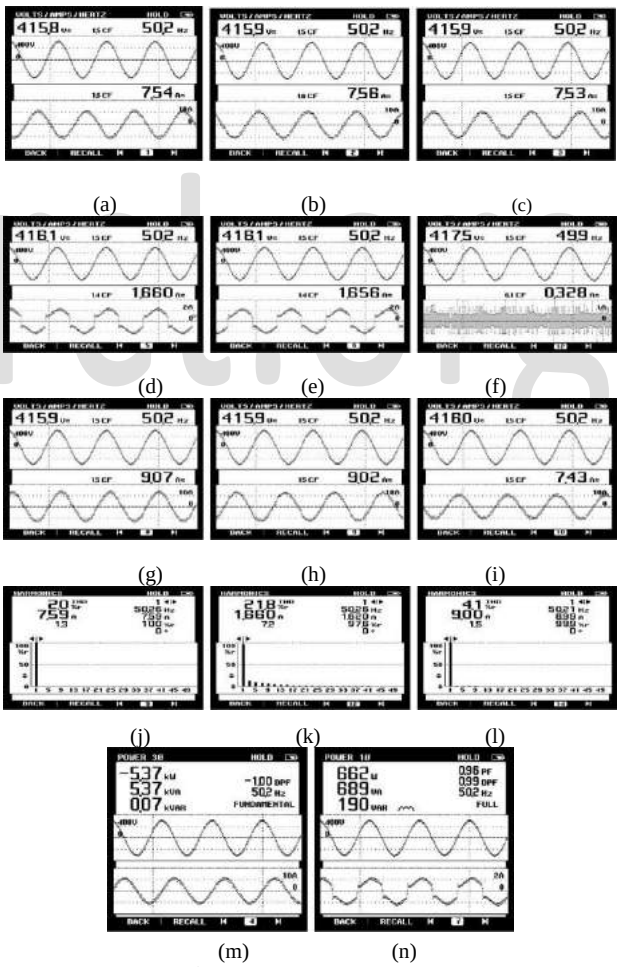
(a) (b) (c)

Fig. 4 Steady state recorded performance for MPPT (a) at 1000 W/m^2, (b) at 500 W/m^2.



(d) (e) (f)

Fig. 5 Steady state performance under balanced linear loads, (a)-(c) v_{sab} with i_{ga}, i_{La}, i_{VSCa} respectively, (d) power drawn from grid (P_g), (e) power drawn by load (P_L), (f) power supplied by VSC P_{VSC}.



(a) (b) (c)

(d) (e) (f)

(g) (h) (i)

(j) (k) (l)

(m) (n)

Fig. 6 Steady state performance under unbalanced nonlinear loads (a)-(c) v_{sab} with i_{ga}, i_{gb}, i_{gc} (d)-(f) v_{sab} with i_{La}, i_{Lb}, i_{Lc}, (g)-(i) v_{sab} with i_{VSCa}, i_{VSCb}, i_{VSCc}, (j)-(l) harmonics spectrum of various currents i_{ga}, i_{La}, i_{VSCa}, (m)power drawn from grid (P_g), (n) power drawn by load (P_L).

B. Dynamics Performance

The dynamic performances of the system for change in insolation, load removal and voltage variation are discussed is

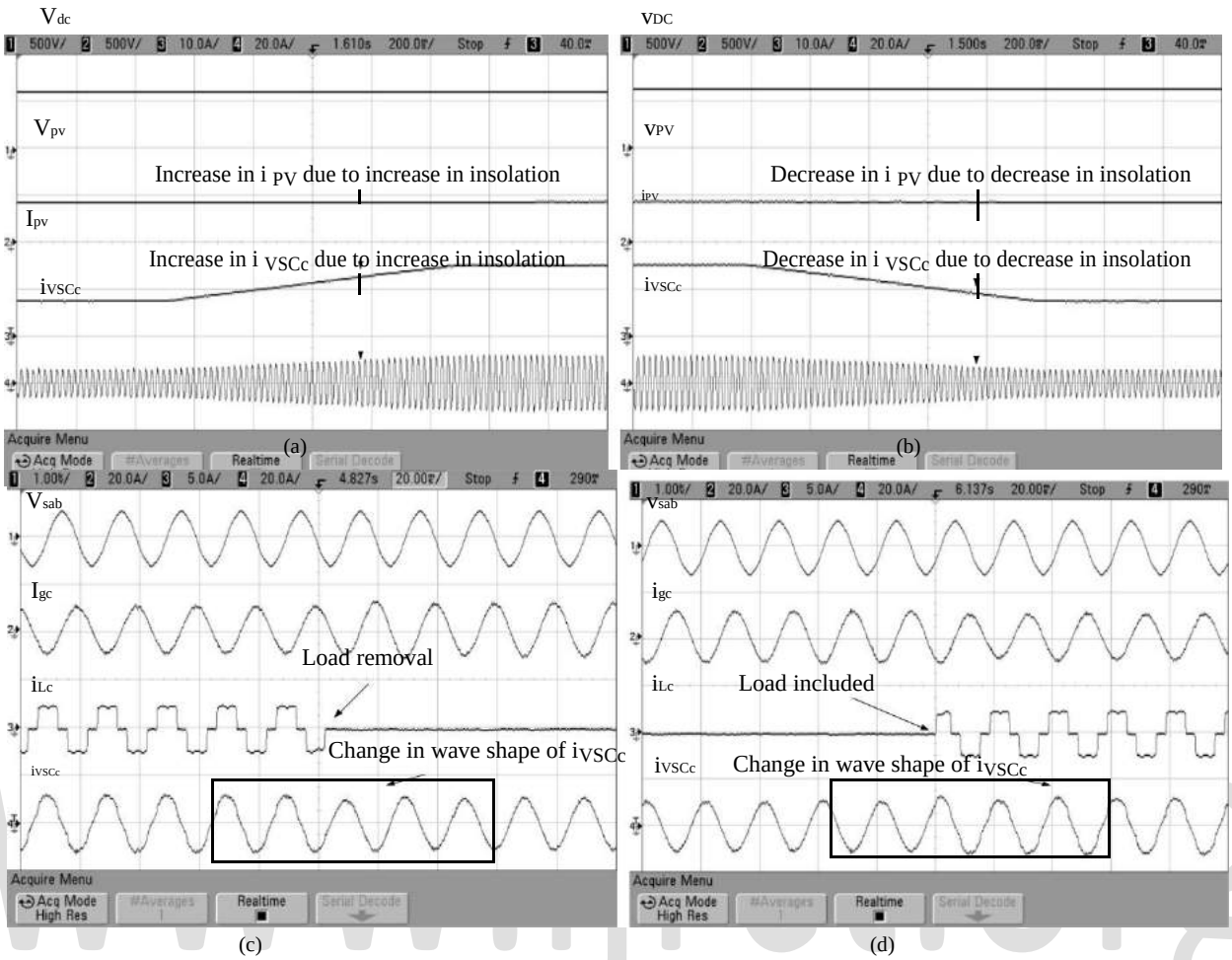


Fig. 7 Dynamic performance under (a) increase in insolation, (b) decrease in insolation, (c) sudden load removal, (d) sudden load inclusion.

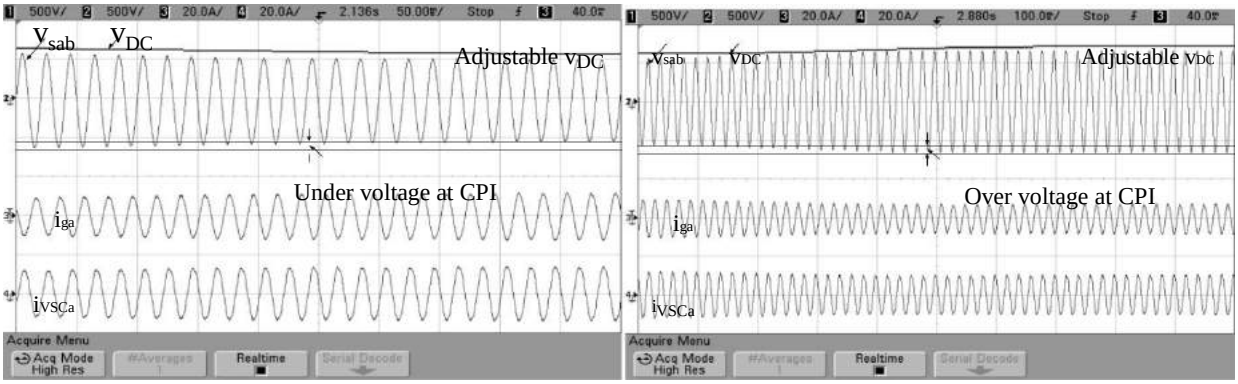
this section. Figs. 7 (a)-(b) show the performance of the system for increase and decrease in insolation level respectively. The solar insolation is changed from 500 W/ m^2 to 1000 W/m^2 and vice versa. Fig. 7 (a) shows that with the increase in insolation, the PV array current increases and the power delivered from PV array also increases. The increase in power fed can be observed from increase in VSC current. The vice versa inferences can be drawn from Fig. 7 (b).

Figs. 7 (c)-(d) show performance of SECS for load disturbances at CPI. The load disturbance is emulated by opening one of the load lines (phase "c"), which not only causes reduction in effective load and also emulates unbalanced load at CPI. The grid current increases after load removal as the net power fed to grid increases. Moreover, a change in wave-shape of phase c current of VSC can be observed in which the VSC currents become sinusoidal after load removal as VSC has not to feed any harmonics current in phase c after load removal. The vice versa explanation of Fig. 7 (c) can be used to explain the performance depicted in Fig. 7 performance for under voltage in CPI voltage. The voltage of the CPI is changed from 415 V to 350 V. The adjustable
(d) wherein load inclusion is demonstrated.

nature of DC link voltage (decreasing with decrease in CPI voltage) can be observed in Fig. 8 (a). The PV array parameters are kept same during this operation. Hence, the grid currents and VSC currents are increased in order to feed same power at lower voltage. Fig. 8 (b) shows the performance for over voltage at CPI. The DC link voltage increases with an increase in CPI voltage. The grid and VSC currents are decreased to feed same real power but at increased voltage.

C. Comparison of Proposed Control Approach with Fixed v_{DC} Based Control Approach

Conventionally in a two stage system, the first stage is a DC-DC converter which serves for MPPT and the output of first stage is cascaded to second stage, which is a grid tied VSC. The DC link voltage of VSC is kept fixed corresponding to maximum value of CPI voltage. For proper control of VSC currents under full range of CPI voltage variation, the DC link voltage should be greater than the peak of maximum allowed grid voltage. The DC link voltage is kept around 10% higher than the peak of maximum allowed grid voltage, considering the drop across the inductor, switches and proper control under dynamics. However, while considering a weak AC grid (far radial end) the over and under voltages are quite common.



(a) (b)

Fig. 8 Dynamic performance for CPI voltage variation (a) decrease in voltage from 415 V to 350 V, (b) increase in voltage from 415 V to 480 V.

Considering the range of voltage variation of ±15 %, the AC mains voltage may vary between 352 V to 477 V approximately for a nominal voltage of 415 V. The fixed DC link voltage for operation under such a voltage range is estimated as,

$$V_{DC} = 1.414 * V_{g\,max} * 1.1 = 1.414 * 477 * 1.1 = 742.40\,V \cong 740V \quad (12)$$

In the proposed system an adjustable DC link voltage structure is proposed to reduce the power loss in the system. The switching losses and the high frequency ohmic losses in the interfacing inductor are dependent on DC link voltage. The ripple content in the interfacing inductor can be reduced by adjusting the DC link voltage. The principle for power loss reduction and its effects on the performance of the over all system are demonstrated experimentally follows.

Fig. 9 shows basic principle for switching power loss in a two-level VSC considering linear transients. The switching logic for the two switches of same leg is always complementary. Therefore, before switching on S_2, the switch S_1 is on, making the voltage across S_2 same as DC link voltage. When S_2 is turned on the voltage across S_2 fall to zero and current from S_1 is shifted to S_2 with a switching transient. It can be easily observed that switching power losses are dependent on DC link voltage of the VSC and the relation for total energy loss per switching in one leg is expressed as,

$$E = \int_0^{t_{on}} p_{switchon}\,dt + \int_0^{t_{off}} p_{switchoff}\,dt = \frac{1}{6} V_{DC}\, I_{VSC}\,(t_{on} + t_{off}) \quad (13)$$

where E is the total energy loss in one switching cycle, $p_{switchon}$ is instantaneous power loss during switch on duration, $p_{switchon}$ is instantaneous power loss during switch off duration, t_{on} is switch on time and t_{off} is switch off duration.

It should be noted that the switching power losses in all 8 power switches (S_1 to S_6 for VSC and S_B and D_B for boost converter) are dependent on DC link voltage. Therefore, the switching power losses are reduced by keeping adjustable DC link voltage based control algorithm, wherein the DC link voltage is kept just sufficient for current control.

The adjustable DC link voltage based control also helps in reduction of high frequency ripple current in the interfacing inductor, which in turn reduces the high frequency ohmic losses. Fig. 10 shows the basic principle for reduction in ripple current by adjustable DC link voltage. The ripple in the interfacing inductor depends on instantaneous voltage difference between the line voltage and the DC link voltage.

$$\Delta I \propto (V_s - V_{DC}) \quad (14)$$

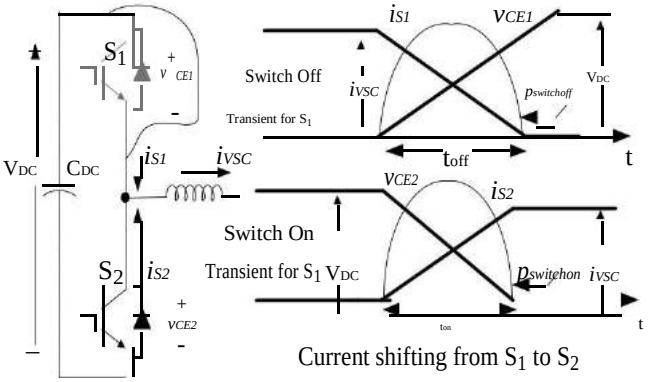


Fig. 9 Switching transient for shunt grid interfaced VSC.

where ΔI is current ripple, V_s is instantaneous CPI volage, and V_{DC} is DC link voltage. From (13) it is clear that the current ripple with fixed DC link voltage corresponding to worst case CPI voltage is higher under all other voltage condition. The increased ripple in the inductor current causes increased ripple in the grid current. Therefore, high frequency ripple current is higher in conventional system.

Fixed DC link Voltage	Adjustable DC link Voltage
Vs2	Vs2

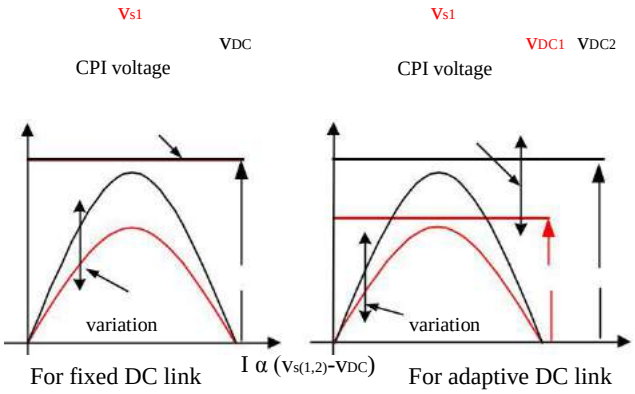


Fig. 10 Basic principle for reduction in ripple current by keeping DC link voltage near to amplitude of grid voltage.

Fig. 11 shows the experimental currents waveforms for grid current with proposed and conventional DC link voltage structure. The lower ripple content with proposed DC line voltage control can be confirmed. The high frequency ripple current is also responsible high frequency ohmic losses. An overall experimental comparison of losses between the two systems is shown in Fig. 12.

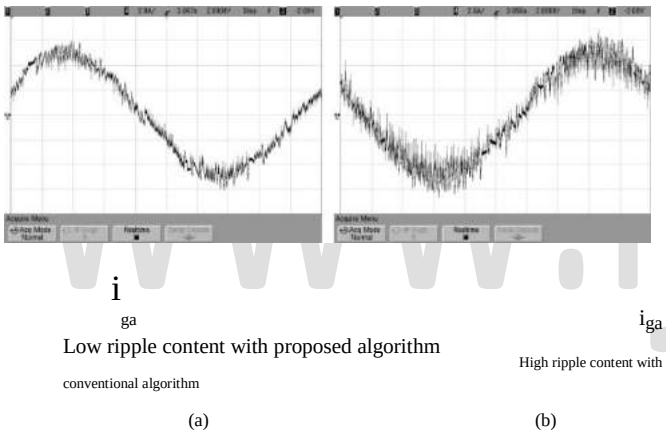


Fig. 11 Grid currents for phase a with (a) proposed DC link voltage structure, (b) conventional DC link voltage structure.

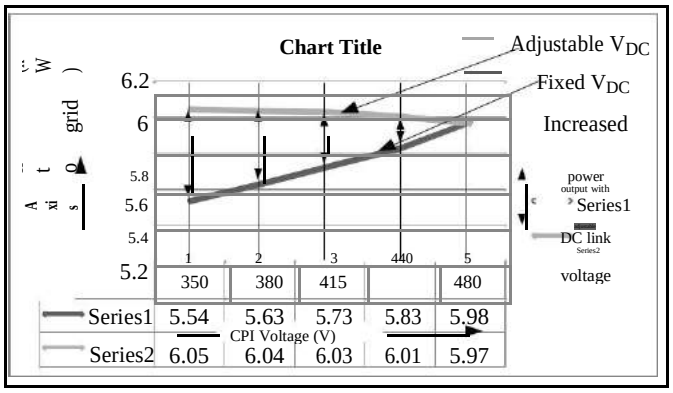


Fig. 12 Comparison of power fed into grid at different CPI voltage by fixed and adjustable DC link based system.

In order to demonstrate the effectiveness of proposed control algorithm, the experiments are conducted for both conventional (fixed DC link voltage) and proposed (adjustable DC link voltage) method keeping the same power from solar array emulator. Fig. 12 shows the experimental comparisons of system with fixed and adjustable DC link voltages. The fixed DC link voltage is kept at 740 V. It can be observed that the power fed into the grid remains almost constant with proposed control approach, however with conventional approach the power fed into the grid is lower at all operating voltage except the worst case highest CPI voltage. It should be noted that even under nominal voltage condition (415 V) the system with adjustable DC link voltage feeds more power into the grid.

V. Conclusion

A two-stage grid tied multifunctional solar energy conversion system has been proposed. The proposed system not only feeds the available solar energy into the grid but also helps in power quality improvement at CPI. The physical significance of all salient internal signals of control algorithms has been presented to make the proposed algorithm intuitive and simple to understand. A PVFF term has improved the dynamic response for changes in PV array power and CPI voltage variation. An interweaved DFSOGI based control algorithm has been proposed and its comparison with conventional SRF theory has been shown to demonstrate its effectiveness

Moreover, an adjustable DC link voltage structure for CPI voltage variation is included in the proposed control algorithm. A comparison of proposed adjustable DC link voltage structure algorithm with fixed DC link based algorithm has been shown which demonstrates direct benefits in terms of increased energy output. The proposed system not only helps in improving the voltage power quality but also helps in reduction of distribution losses. The proposed system yields increased energy output using the same hardware resources just by virtue of difference in DC link voltage control structure. The THDs of the grid currents are found less than 5% (within IEEE-519 standard [26]) even under nonlinear loads at CPI. Test results have shown the feasibility of proposed system.

REFERENCES

[1] M. Kolhe, "Techno-Economic Optimum Sizing of a Stand-Alone Solar Photovoltaic System," *IEEE Transactions on Energy Conversion*, vol.24, no.2, pp.511-519, 2009.

[2] M.A.G. de Brito, L. Galotto, L.P. Sampaio, G. de Azevedo e Melo and C.A. Canesin, "Evaluation of the Main MPPT Techniques for Photovoltaic Applications," *IEEE Transactions on Industrial Electronics*, vol.60, no.3, pp.1156-1167, 2013.

[3] J.S.C.M. Raj and A.E. Jeyakumar, "A Novel Maximum Power Point Tracking Technique for Photovoltaic Module Based on Power Plane Analysis of I–V Characteristics," *IEEE Trans. on Ind. Electron.*, vol. 61, no. 9, pp.4734-4745, 2014.

[4] Fangrui Liu, Shanxu Duan, Fei Liu, Bangyin Liu and Yong Kang, "A Variable Step Size INC MPPT Method for PV Systems," *IEEE Trans. Ind. Electron.*, vol.55, no.7, pp.2622-2628, 2008.

[5] S. Singh and B. Singh, "Optimized Passive Filter Design Using Modified Particle Swarm Optimization Algorithm for a 12-Pulse Converter-Fed LCI–Synchronous Motor Drive," *IEEE Transactions on Industry Applications*, vol.50, no.4, pp.2681-2689, 2014.

[6] H. Akagi, "Active Harmonic Filters," *Proceedings of the IEEE*, vol.93, no.12, pp. 2128-2141, Dec. 2005.

[7] S.AO. da Silva and R.A. Modesto, "A comparative analysis of SRF-based controllers applied to active power line conditioners," *34th Annual Conf. of IEEE on Industrial Electronics (IECON)*, 2008. pp. 405-410.

[8] M. Kesler and E. Ozdemir, "Synchronous-Reference-Frame-Based Control Method for UPQC Under Unbalanced and Distorted Load Conditions," *IEEE Trans. Ind. Electron.*, vol. 58, no. 9, pp. 3967-3975, 2011.

[9] Arun Kumar Verma, Bhim Singh and D.T Sahani "Grid Interfaced Solar Photovoltaic Power Generating System with Power Quality