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APPLIED RESEARCH

Analysis of Novel Core-Shell Junctionless Nanosheet FET for CMOS Logic Applications

VAKKALAKULA BHARATH SREENIVASULU[1], (Member, IEEE), M. PRASAD[2], (Member, IEEE), EPURI DEEPTHI[3], ARURU SAI KUMAR[4], (Member, IEEE), AND S. SUDHEER MANGALAMPALLI[5], (Member, IEEE)

[1]Department of Electronics and Communication Engineering, Manipal Institute of Technology Bengaluru, Manipal Academy of Higher Education, Manipal, Karnataka 576104, India
[2]Department of Electronics and Communication Engineering, Nitte Meenakshi Institute of Technology, Bengaluru, Karnataka 560064, India
[3]Department of Electronics and Communication Engineering, Malla Reddy Engineering College, Hyderabad, Telangana 500100, India
[4]Department of Electronics and Communication Engineering, VNR Vignana Jyothi Institute of Engineering and Technology, Hyderabad 500090, India
[5]Department of Computer Science and Engineering, Manipal Institute of Technology Bengaluru, Manipal Academy of Higher Education, Manipal 576104, India

Corresponding author: Vakkalakula Bharath Sreenivasulu (vb.sreenivasulu@manipal.edu)

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ABSTRACT A Rectangular core-shell (RCS) is analyzed on vertically stacked gate oxide junctionless nanosheet along with doping and gate/dielectric engineering. This paper also proposes an N-type three fins vertically stacked with gate oxide stack junctionless nanosheet with opposite core doping in the channel known as RCS. The simulation results show that gate oxide stack with RCS junctionless nanosheet exhibit reduced I_{OFF} is 6.913E-21, increased I_{ON} is 2.408E-07, I_{ON}/I_{OFF} ratio is 0.418 $\times$ 10^6, DIBL is 6.9mV and SS of 60.65 mV/dec respectively. The core shell width variations with various gate oxide dielectric towards better I_{ON}, I_{OFF} and I_{ON}/I_{OFF} are analyzed. Interestingly, it is noted that for smaller shell thickness, the thickness of core should be equivalent to shell thickness and for larger shell thickness, thicker core is required. The device robustness towards analog and RF metrics are also evaluated with varied gate dielectrics. It has been observed that RCS architecture with opposite doping with HfO_2 as gate oxide material has given outstanding outcomes compared to other gate oxide materials and without RCS method. Further, simulated the P-type of three fins vertically stacked with gate oxide stack junctionless nanosheet and combined both N-type and P-type three fins vertically stacked with gate oxide stack junctionless nanosheet to construct the CMOS inverter circuit. The voltage transfer characteristics (VTC) characteristics of junctionless nanosheet with RCS having HfO_2 as gate-oxide based inverter has been notably improved as compared to the SiO_2, Al_2O_3 and conventional three fins vertically stacked with gate oxide stack junctionless nanosheet inverter.

INDEX TERMS Junctionless, stacked quad gate, gate oxide stack, RCS architecture, inverters.

I. INTRODUCTION

The shrinking of MOSFET came to an end for advanced nodes due to power, area and performance aspects. Thus, the advent of double gate, triple gate and gate all around FETs emerged for future nodes. The double gate junctionless FET with a variation of core thickness and gate misalignment on RCS shows better performance than the conventional double gate junctionless FET [1]. The double gate junctionless FET with RCS architecture performance is enhanced by employing doping engineering [2]. The gate oxide stack junctionless three fins vertically stacked FET compared to a single quad gate with stacked gate oxide junctionless FET, the nanosheet performance outperforms better [3]. The nanowire transistors without junctions feature lower supply side resistance (SS), very low leakage currents, and less degradation in mobility with temperature and gate voltage than conventional transistors [4]. The junctionless nanowire transistor appears to be a viable contender for future CMOS scaling. Because it provides an improvement in I_{ON}/I_{OFF} ratio and current drive consistent with IRDS requirements [5]. When compared to single gate transistors, double lateral gate transistors are superior choices in terms of performance [6]. The dual material gate with double

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gate junctionless transistor exhibits superior subthreshold swing, DIBL, transconductance, I_{ON}/I_{OFF} ratio and intrinsic delay [7]. The effect of BTBT on the OFF-state behaviors of SOI-JLT and BPJLT was investigated. Because of the strong doping in the channel, the BTBT current is seen to be substantial in SOI-JLT [8]. Due to quantum confinement, junctionless transistors become less sensitive to channel thickness when the thickness is decreased to less than 4nm [9]. The vertical stacked nanowire FET with high doping in inversion mode results in smaller tunnelling width than in the junctionless mode [10]. The shell doping profile for junctionless FET offers to avoid the large series resistance and quantum confinement [11]. The inclusion of a high-k dielectric as a spacer improves the OFF current (I_{OFF}) while also increasing the scalability of the device [12]. The rectangular core-shell junction-less FET with the use of gate dielectric engineering enhances the performance of the conventional junctionless FET [13]. In a double gate junctionless transistor, using a hetero gate dielectric minimizes band to band tunnelling effects in the sub- threshold domain [14]. Because it is easier to fabricate, has less instability, and has superior electrical characteristics to standard inversion mode devices, the junctionless multi-gate transistor has enormous potential for the future [15]. The junctionless transistors are scale down from 30nm to 20nm and compared the results. The result reveals that based upon the requirement of parameter, the device can be selected accordingly [16]. The junctionless Si nanowire provides better electrical features than conventional inversion mode nanowire transistors [17]. The inclusion of a high-k oxide decreases leakage current while preserving the driving current high [18]. The authors have discussed the limitation and challenges in scale down, the threshold voltage of double-gate MOSFET [19]. The four-layer vertically stacked horizontal gate-all-around Si nano sheets device structure are optimized and better results in Electrical characteristics are obtained [22].

The term ''nanosheet'' implies the future form of field-strip FETs, which enable current to flow across numerous silicon stacks entirely encircled by a transistor gate. With fewer paths for current to leak through and more current available to the device, the design improves performance and mitigates power consumption. The gate is surrounded by rectangular silicon fins and a stack of thin silicon sheets known as nanosheets, which widens the channel in a smaller transistor while effectively controlling leakage current. The objective of this work is to improve the performance of a quad gate oxide stack junctionless nanosheet (QGOSJLNS) with three fins stacked vertically by using gate/dielectric engineering, doping engineering, and RCS architecture, in that order. To design three final structures of both N-type and P-type devices, which are then utilized in inverter circuits, three fins are finally vertically stacked with various gate oxide stack junctionless Nanosheets with RCS. Furthermore, a comparison was performed between the three inverter circuits.

Fabrication of stacked nanosheet with most semiconductor production techniques cutting straight down from the top of the silicon or filling straight up from the exposed surface, this could seem like a challenging task. The substance between layers of other materials must be removed from nanosheets, and the voids must be filled with both metal and dielectric. After the silicon nanosheet channel areas have been constructed, the remaining spaces must be filled up by enclosing the channel with metal to produce the gate stack after first enclosing it with dielectric. The technique known as atomic layer deposition is used to complete each of these procedures.

A gaseous chemical is absorbed by exposed surfaces in this process, including the bottom of the nanosheet, to produce a single layer. The required substance, such as the dielectric hafnium dioxide, is next introduced, and it reacts with the first chemical to leave an atomic-scale layer. It is possible to regulate the deposited material's thickness down to the level of an individual atom thanks to the technique's extreme precision. By stacking more Nano-sheets, we might increase performance by a factor of ten or more. (Researchers at HRL Laboratories in Malibu, California are working on the stacking tens of Nano-sheets).

The full forms of acronyms: RCS- Rectangular Core-Shell, HfO_2-Hafnium oxide, SiO_2-Silicon dioxide, Al_2O_3-aluminium oxide, FET- Field-effect transistor, BTBT-Band to Band tunnelling, SOI-JLT-Silicon-on-insulator junctionless transistor, DIBL-Drain induced barrier lowering, CMOS- complementary metal-oxide-semiconductor, IRDS [5]- International roadmap for devices and systems, I_{ON}-ON current, I_{OFF}-OFF current, V_{th}-Threshold voltage, SS-Sub-threshold voltage, QGOSJLNS-Quad gate Oxide stack junctionless nanosheet, Lin-Linear, Sat- Saturation.

II. DEVICE STRUCTURE AND SIMULATION

The Visual TCAD platform was used to simulate and construct three fins vertically stacked QGOSJLNS with RCS. Fig 1 shows a 3D modelled view of three fins vertically stacked QGOSJLNS and Fig 2 shows three fins vertically stacked QGOSJLNS simulation setup model. All the structural specifications for both structures are shown in Table 1. Fig 1 represents only one doping concentration i.e., N+ regions through the channel, whereas Fig 3 represents core-shell having the P+ doping that is opposite doping concentration, which is called RCS at the core, which is represented as t_{core} in Fig 3, then tshell having N+ doping concentration and simulation 3D view as shown in Fig 4. The dielectric constants of the low-k and high-k interfacial layers were set to 3.9, 9, and 22 respectively. In Fig 1 oxide 1 is SiO_2 and Oxide 2 is HfO_2, whereas in Fig 3 oxide 1 is SiO_2 and Oxide 2 is varied for different oxides i.e. HfO_2, SiO_2 and Al_2O_3. While the operation voltage V_{DD} was set to 0.1V and 1V in the linear and saturation regions, respectively [20], [21].

The I_{DS} in the nano-scale unit is based on Potential, Electric-Filed, and Carrier Temperature. The Lombardi model is used to measure the current which consists of three parameters: bulk mobility, dispersion-mobility, and mobility on surface charge. According to Matthiessen's law, the combined carrier mobility in the inversion layer is determined by three factors.

$$1/\mu s = 1/\mu b + 1/\mu ac + 1/\mu sr \quad (1)$$

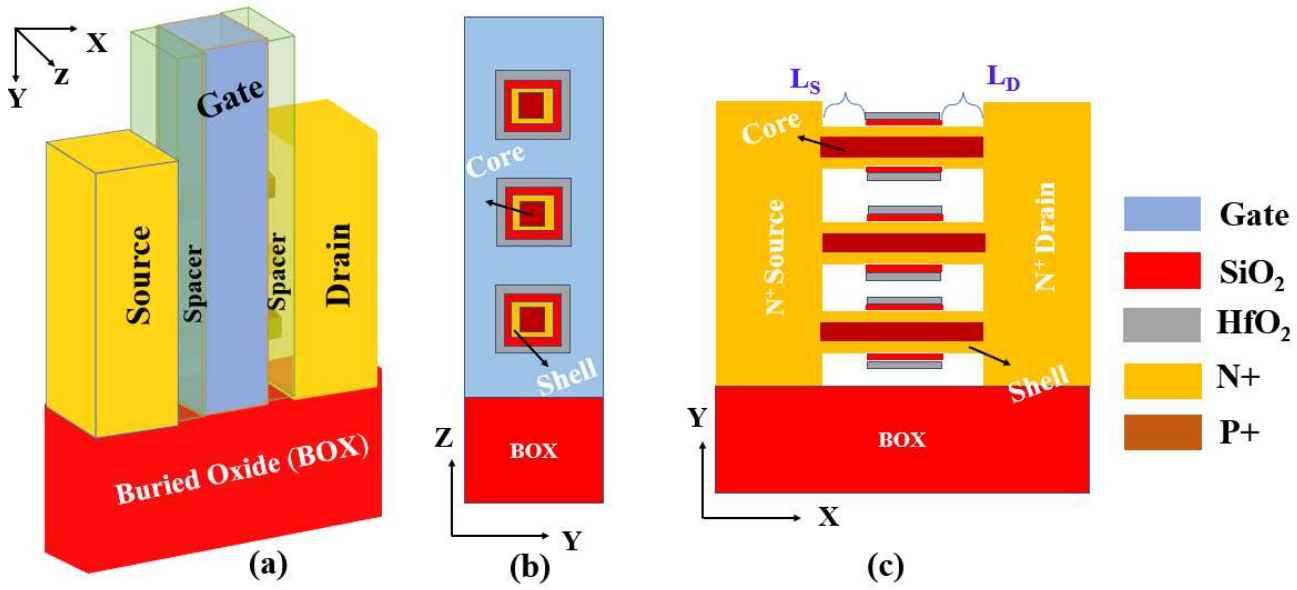

FIGURE 1. The 3D View of three fins vertically stacked QGOSJLNS of simulation model setup.

where μb represents doping dependent bulk mobility, μac represents mobility degradation due to acoustic phonon scattering and μsr represents mobility degradation due to surface roughness.

TABLE 1. Structural specifications for three fins vertically stacked QGOSJLNS.

Parameters	Conventional QGOSJLNS	QGOSJLNS With RCS
Gate Length	30 nm	30 nm
Work Function (W.F) NMOS	5.2 eV	5.2 eV
Shell-Doping (N_D)	1E19	1E19
Core Doping (N_A)	-	1E17 to 1E19
Oxide-thickness (t-oxide 1)	1nm	1nm
Oxide-thickness (t-oxide 2)	1nm	1nm
Core-thickness (t-core)	-	1nm to 4nm
Shell-thickness (t-shell)	10nm	2nm to 4nm
Gate oxide thickness (t-gate)	1nm	1nm
Channel Length (L_g)	30nm	30nm
Channel width (L_w)	10nm	10nm
SiO_2 PMOS HfO_2	W.F	4.27 eV
PMOS Al_2O_3	W.F	4.24 eV
PMOS	W.F	4.25 eV

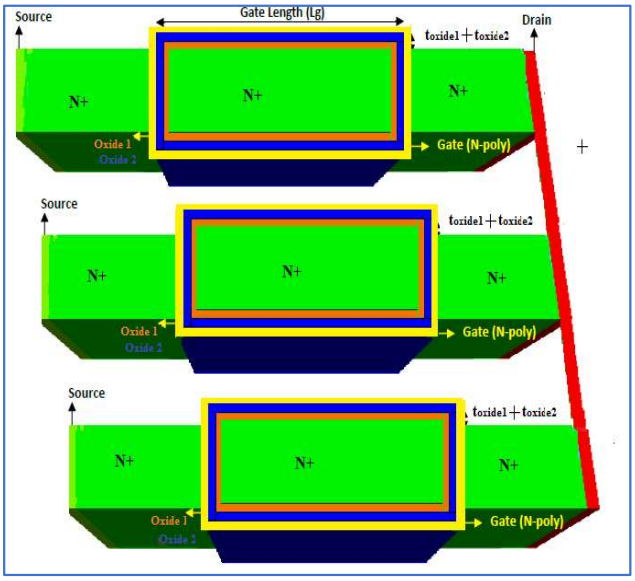

FIGURE 2. 3D View of three fins vertically stacked QGOSJLNS.

III. RESULTS AND DISCUSSION

The Three fins vertically stacked QGOSJLNS reference structure [3] has the design configuration as shown in Table 1. The same structure is built and optimized to match the reference data for the same design parameters as presented in [3]. With a V_{GS} variation from 0 V to 1.2 V and a fixed V_{DS} of 0.1 V, both the reference and simulation structures are simulated. The I_D vs V_{GS} plot in Figure 5 demonstrates that the findings of the reference and simulation architectures are well-matched [21]. Three fins vertically stacked QGOSJLNS and Three fins vertically stacked QGOSJLNS with RCS architecture are also simulated with V_{GS} ranging from 0 to 1.2V and a constant V_{DS} of 0.1V. The results reveal that three fins vertically stacked QGOSJLNS with RCS structure have lower I_{OFF} and higher I_{ON} than three fins vertically stacked QGOSJLNS, as illustrated in Fig 4 for I_{DS} versus V_{GS}.

Table 2 shows the comparative analysis of the three fins vertically stacked QGOSJLNS and three fins vertically stacked QGOSJLNS with RCS architecture. The results show that reduced off current and increased I_{ON}/I_{OFF} ratio which is 1.685 times higher than the three fins vertically stacked QGOSJLNS.

Furthermore, the performance of three fins vertically stacked QGOSJLNS with RCS is simulated using various

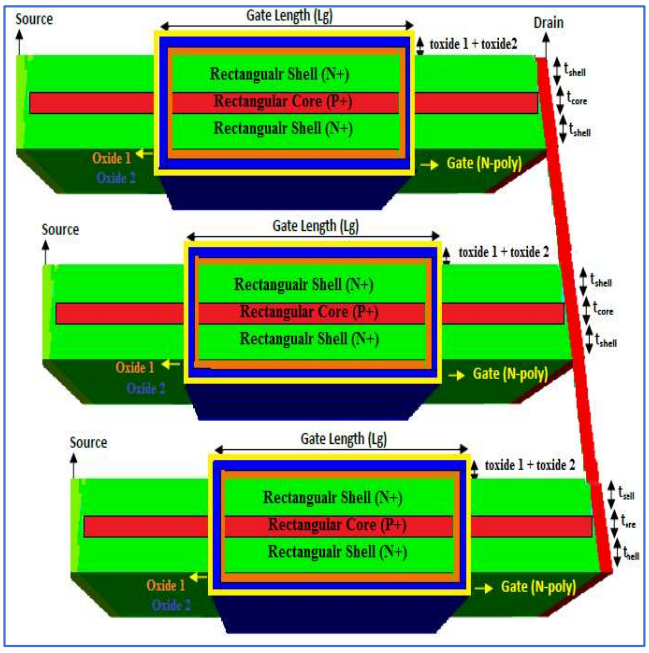

FIGURE 3. 3D View of three fins vertically stacked QGOSJLNS with RCS architecture.

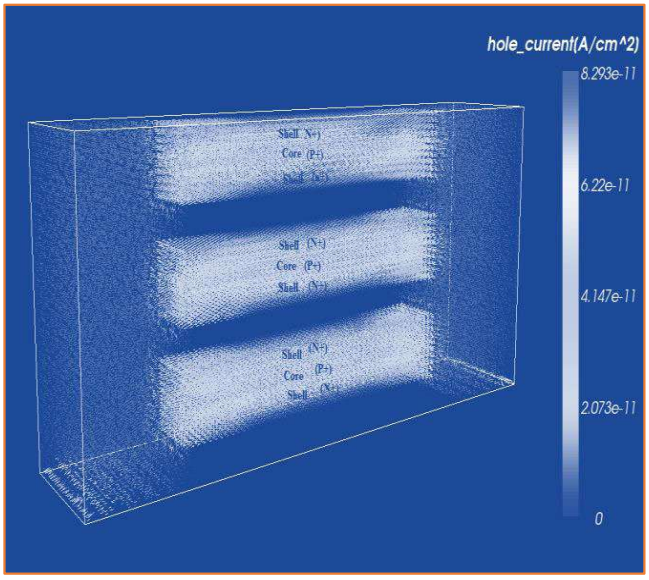

FIGURE 4. 3D View of three fins vertically stacked QGOSJLNS with RCS of simulation model setup.

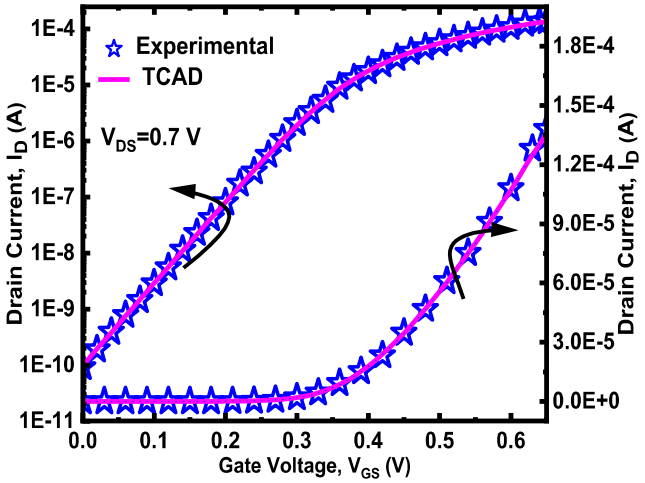

FIGURE 5. The calibration $I_D - V_{GS}$ characteristics of reference and simulation [21].

TABLE 2. Comparative analysis of three fins vertically stacked QGOSJLNS and three fins vertically stacked QGOSJLNS with RCS.

Model	I_{OFF}(A)	I_{ON}(A)
QGOSJLNS	7.61E-20	2.70E-07
QGOSJLNS With RCS	6.91E-21	2.41E-07

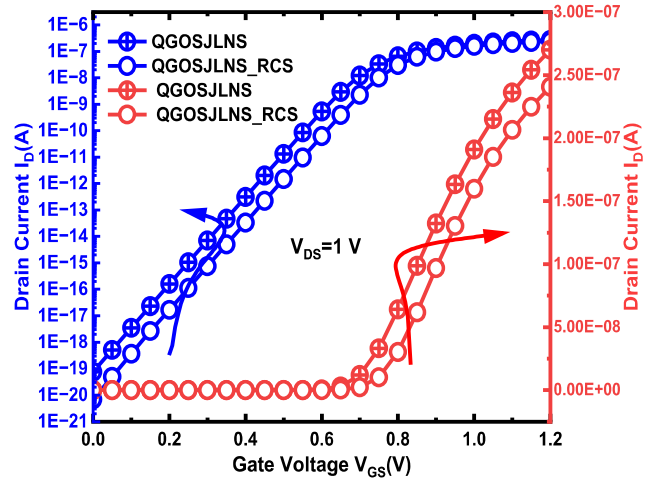

FIGURE 6. The $I_D - V_{GS}$ plot for three fins vertically stacked QGOSJLNS and three fins vertically stacked QGOSJLNS with RCS at $V_{DD} = 0.1$V.

dielectric materials such as SiO_2, Al_2O_3, and HfO_2. After that, all three dielectric material devices are simulated in the linear and saturation regions with V_{DS} is equal to 0.1 V and 1 V respectively and V_{GS} is varied from 0 V to 1.2 V. For the gate stack the oxide thickness is 2 nm because it's stacked gate oxide (1 nm of SiO_2 + 1 nm of SiO_2, 1 nm of SiO_2 + 1nm of HfO_2, 1 nm of SiO_2 + 1nm of Al_2O_3). Due to the high permittivity dielectric's customization in potential profile, there is the increase in carrier velocity and, therefore, carrier transport efficiency. Hence with the use of HfO_2 having a high-k value of 22, shows better performance in increased trans-conductance, early voltage, and intrinsic gain than the other two gate oxide materials. The outcome of the simulation for HfO_2 as gate dielectric with RCS shows increased I_{ON} and reduced I_{OFF} than the SiO_2 and Al_2O_3 as the gate dielectric.

The Table 3 shows the comparison results for different gate dielectric materials for three fins vertically stacked QGOSJLNS with RCS architecture. The results are plotted as shown in Fig 5. In Fig 5 represents two curves, one curve represents in Log scale and another one in the linear scale.

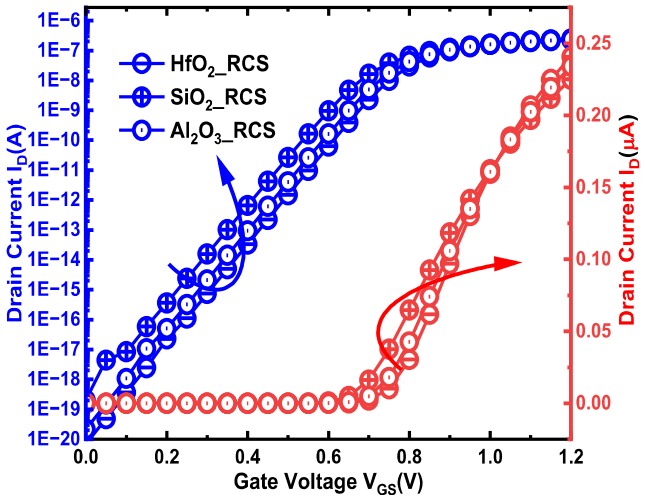

FIGURE 7. The $I_D - V_{GS}$ plot for three fins vertically stacked QGOSJLNS with RCS for different gate dielectric at $V_{DS} = 0.1V$.

TABLE 3. Comparison of RCS for different gate dielectric.

Model	Region	I_{OFF} (A)	I_{ON} (A)	I_{ON}/I_{OFF}
HfO_2-RCS	Lin	6.913E-21	2.408E-07	0.34E14
	Sat	4.512E-19	9.555E-07	2.1E12
SiO_2-RCS	Lin	2.05E-19	2.251E-07	1.07E12
	Sat	7.48E-19	1.010E-06	0.13E13
Al_2O_3-RCS	Lin	2.156E-20	2.341E-07	1.08E13
	Sat	4.872E-19	9.758E-07	2.03E12

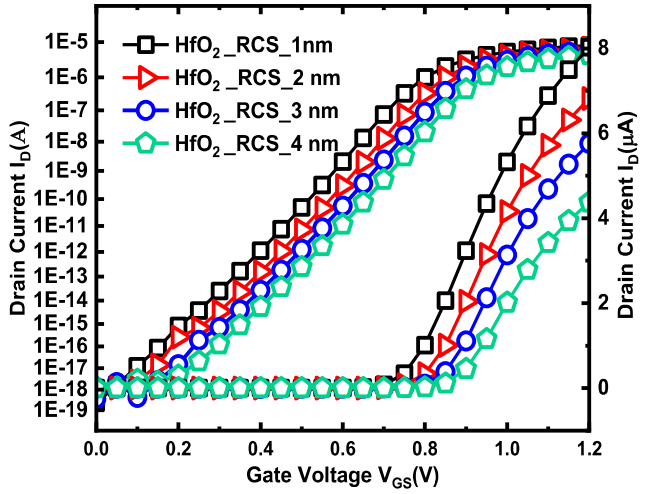

FIGURE 8. The $I_{DS} - V_{GS}$ plot for three fins vertically stacked QGOSJLNS with RCS for different shell width.

Table 4 depicts the performance evaluation in terms of drain-induced barrier lowering (DIBL), threshold voltage, and sub-threshold swing (SS) in the linear and saturation regimes. All the findings are close to perfect, however, when fine-tuning the parameters, three fins vertically stacked QGOSJLNS with RCS for HfO_2 as gate dielectric reveal the SS 60 mV/dec and DIBL is minimal in comparison to others. After calculating the threshold voltage in all instances, it indicates that SS achieves the best value for HfO_2. It is evident

TABLE 4. Comparison of V_{th}, DIBL and SS for all three structures.

Fins (RCS)	V_{th} Lin(V)	V_{th} Sat(V)	DIBL (mV/dec)	SS $_{Lin}$ (mV/dec)	SS $_{Sat}$ (mV/dec)
HfO_2	0.591	0.584	6.9	60.65	60.74
SiO_2	0.514	0.504	10.8	61.47	61.24
Al_2O_3	0.564	0.557	8.2	60.96	60.75

TABLE 5. Core shell width variation for quad gate oxide vertically stacked junctionless Nanosheet with RCS architecture.

Shell-Core-Shell(nm)	I_{OFF}(A)	I_{ON}(A)	I_{ON}/I_{OFF}
4.5-1-4.5	6.913E-21	2.408E-07	0.34E14
4-2-4	2.718E-20	2.406E-07	0.88E13
3.5-3-3.5	1.058E-20	1.728E-07	1.63E13
3-4-3	3.97E-20	1.312E-07	0.33E13

that HfO_2 as a gate dielectric material presents lowered DIBL and SS value of near-ideal value when the threshold voltage is determined using a constant current approach. The mathematical formulas for SS [2] and DIBL [2] are calculated as:

$$SS = \frac{\partial \mathbf{VGS}}{\partial \mathbf{log(IDS)}}. \tag{2}$$

$$DIBL = \frac{(Vth\ Lin - Vth\ sat)}{(Vsat - VLin)} \tag{3}$$

where, V_{thLin} is the threshold voltage measured at a very low drain voltage i.e. 0.1V and V_{thSat} is the threshold voltage measured at a high drain voltage i.e. 1V. The V_{sat} is the supply voltage (the high drain voltage) and V_{Lin} is the low drain voltage.

In addition, three fins vertically stacked QGOSJLNS with RCS for HfO_2 as gate dielectric material are simulated with different core-shell width variations from 1nm to 4nm, which are simulated in the linear region at 0.1V of V_{DD} and V_{GS} is varied from 0V to 1.2 V with W.F of 5.2. The outcome of simulation at core-shell of 1nm shows the notable improvement in reduced I_{OFF} with a higher I_{ON}/I_{OFF} ratio than the 2nm, 3nm, and 4nm core-shell width. The result analysis is plotted as shown in Fig 6.

The channel's layer volume depletion of carriers is indicated by a decrease in the OFF current (I_{OFF}) and an increase in core thickness. The oppositely doped core (P+) in RCS generates two PN junctions, which lead to depletion zones in the device, which is how the rectangular core functions in the device. The core and a portion of the top and bottom shells are included in the depletion area. Thinner core thereby aids in the depletion of carriers in the shell areas that are not depleted by the gate when the shell is maintained at 4 nm and 4.5 nm. However, when the carriers within the core fail to exhaust themselves, the device's performance begins to deteriorate

as the thickness of the core increases. Table 5 tabulates the results of the modifications in core width. Compared to the other width configurations, the results show a lower I_{OFF} current for the 4.5-1-4.5 width.

Further, the triple-fin quad gate vertically staked junctionless nanosheet with 4.5-1-4.5 RCS architecture is simulated for different doping level acceptors at 1E17 cm^{-3}, 1E18 cm^{-3}, and 1E19 cm^{-3} respectively. The core is made of P+ as shown in Fig 4. The opposite doping at core means having P+, whereas the shell doping is varied from lower doping to higher doping. The result of all three models is represented in I_D-V_{GS} plot. The simulated results for all doping are plotted and shown in Fig 7.

In table 6 shows the performance evaluation of three fins vertically stacked QGOSJLNS with RCS architecture for core doping variation. The results for 1E19 cm^{-3} show reduced I_{OFF} and increased I_{ON} than other doping levels. In terms of various parameters such as I_{OFF}, I_{ON}, I_{ON}/I_{OFF} ratio, reduced DIBL, the near-ideal value of SS, and so on, it has been observed that RCS architecture with opposite doping with HfO_2 as gate oxide material has given outstanding outcomes and exhibits the best performance compared to other gate oxide materials and without RCS method.

A. POTENTIAL DISTRIBUTION

Due to high permittivity dielectric affects the potential profile, it causes an enhancement in carrier velocity and, consequently, an increase in carrier transport efficiency. Hence with the use of HfO_2 having a high-k value of 22, shows better performance in increased trans-conductance, early voltage, and intrinsic gain than the other two gate oxide materials. The 3D view of surface and core potential distribution for three fins vertically stacked QGOSJLNS with RCS architecture for HfO_2 gate dielectric with electron density is shown in Fig 8 and electric current in Fig 9 and potential distribution in Fig 10. The electron density is maximum in the channel area in shell area which increases performance. The variation of electric current is shown in Fig 11. The channel's potential distribution is uniform throughout and has a negative value because of the vacuum. Typically, a 2D Poisson equation that does not fully capture its variance determines the potential distribution inside the channel. Its output properties are largely determined by geometry because of the 3D structure. It is necessary to accurately analyze the internal channel potential to determine the channel current. The device's thickness, width, and oxide material sheets were evaluated for surface potential.

TABLE 6. Doping variation for three fins vertically stacked QGOSJLNS with RCS architecture.

Doping (cm^{-3})	I_{OFF}(A)	I_{ON}(A)	I_{ON}/I_{OFF}
1E17	1.545E-20	2.878E-07	3.4E12
1E18	8.758E-21	2.676E-07	0.29E14
1E19	6.913E-21	2.408E-07	0.34E14

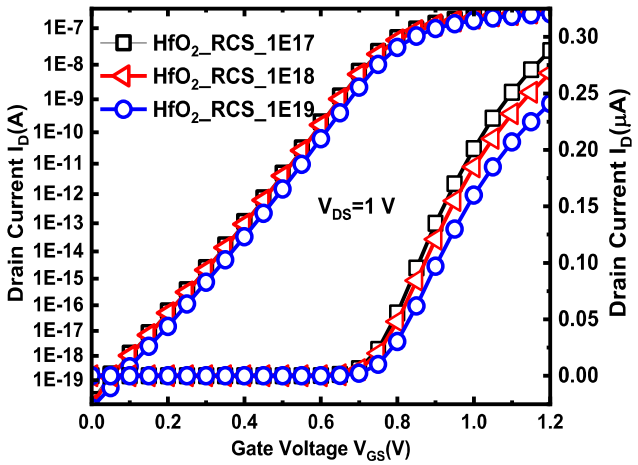

FIGURE 9. The $I_D - V_{GS}$ plot for three fins vertically stacked QGOSJLNS with RCS for different doping levels.

In combination with the hole and electron continuity equations, the drift diffusion model must solve a specific set of partial differential equations, which includes Poisson's equation:

$$\Delta\varepsilon\Delta\psi = -q(p - n + N_D^+ - N_A^-) \tag{4}$$

where ψ is the vacuum level's electrostatic potential. The N+ and N- are the concentrations of ionized impurities, whereas n and p represent the concentrations of electrons and holes, respectively. The electron's charge is expressed as q.

$$Ev = Ec - Eg + \Delta Ev \tag{5}$$

Here, x is the electron affinity. The Eg is the band gap of semiconductor. The ΔEc and ΔEv are the band gap shift caused by heavy doping or mechanical strain. Further-more, the relationship of vacuum level ψ and intrinsic Fermi potential ψ intrinsic is:

$$\psi = \psi intrinsic - \frac{X}{q} - \frac{Eg}{2q} - \frac{KbT}{2q} ln \frac{Nc}{Nv} \tag{6}$$

The reference 0 eV of energy is set to intrinsic Fermi level of equilibrium state.

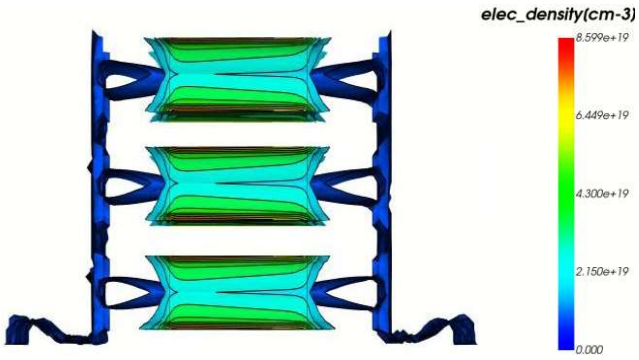

FIGURE 10. The electron density of three fins vertically stacked QGOSJLNS with RCS for HfO2 as gate dielectric.

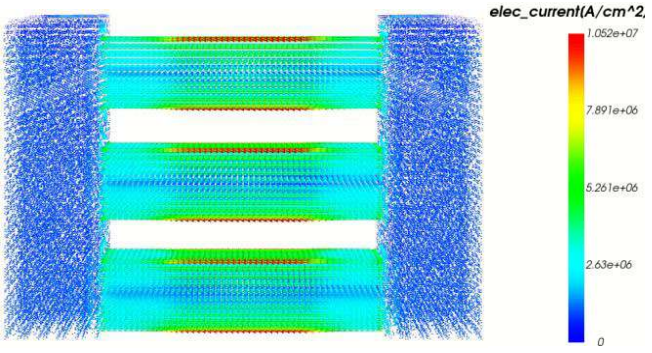

FIGURE 11. The electric current of three fins vertically stacked QGOSJLNS with RCS for HfO_2 as gate dielectric.

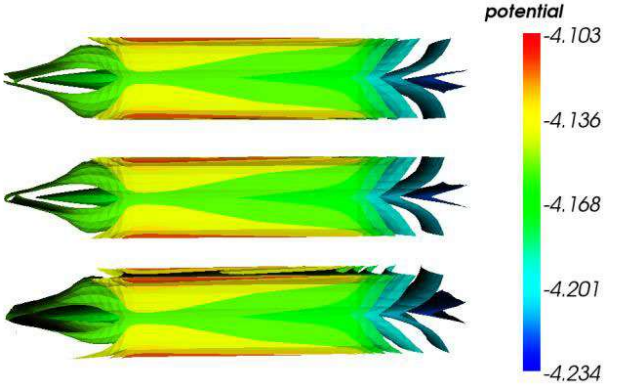

FIGURE 12. The potential distribution over core and surface for three fins vertically stacked QGOSJLNS with RCS for HfO2 as gate dielectric.

B. TRANSCONDUCTANCE (g_m)

The transconductance (g_m) measures the ability of a device under consideration, in converting the applied input voltage into an output current. It is evaluated as the ratio of change in I_{DS} to change in V_{GS} at a constant V_{DD}. It is expressed as, the relationship of conduct band Ec, valence band Ev and vacuum level ψ is:

$$Ec = -q\psi - \mathrm{X} - \Delta\mathrm{Ec} \tag{7}$$

$$gm = \frac{\delta \mathrm{Id}}{\delta \mathrm{Vgs}} \tag{8}$$

Fig 11 shows the transconductance plot for three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2, and Al_2O_3 gate dielectric. With RCS-HfO_2 shows high g_m value than the other two gate dielectric.

C. OUTPUT CONDUCTANCE (g_d)

The output conductance (g_d) [2] is the ratio of I_{DS} upon V_{DS} with a constant V_{GS}. It is expressed as,

$$gd = \frac{\delta \mathrm{ID}}{\delta \mathrm{VGS}} \tag{9}$$

Fig 12 shows the output conductance plot for three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2, and Al_2O_3 gate dielectric. With RCS-HfO_2 shows a better g_d value than the other two gate dielectric.

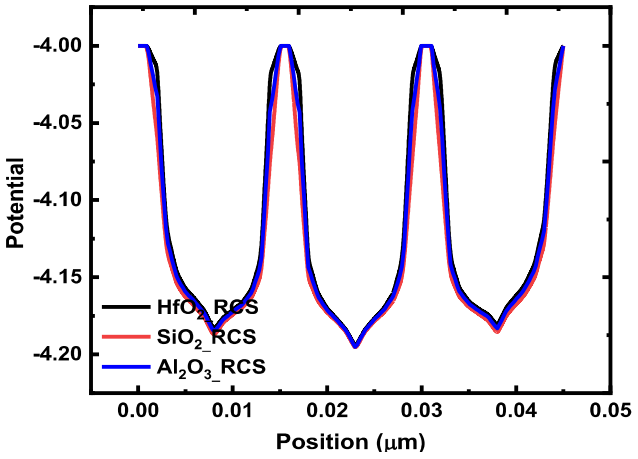

FIGURE 13. Potential distribution cutline for three fins vertically stacked QGOSJLNS with RCS for HfO2, SiO2 and Al2O3 as gate dielectric.

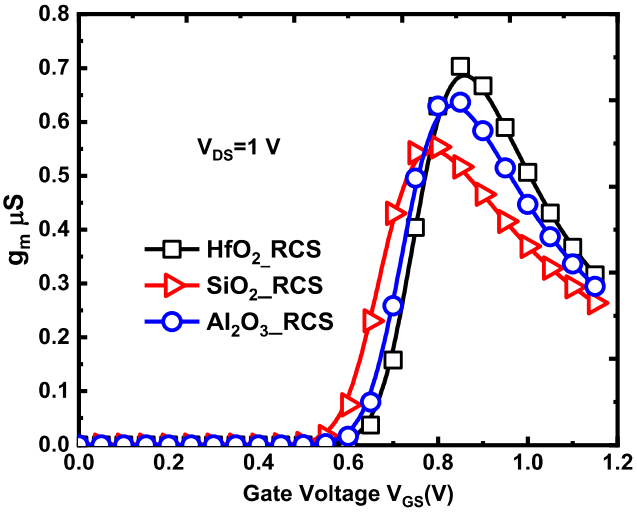

FIGURE 14. The transconductance plot of three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2 and Al_2O_3 gate dielectric.

D. INTRINSIC GAIN (A_v)

The intrinsic gain (A_v) [2] is the ratio of g_m upon gd. Fig 10 shows the variation of A_v with respect to V_{GS} keeping V_D fixed at saturation of 1V.

$$Av = \frac{\mathrm{gm}}{\mathrm{gd}} \tag{10}$$

Fig 13 shows the Intrinsic Gain (A_v) plot of three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2, and Al_2O_3 gate dielectric. With RCS-HfO_2 shows high A_v value than the other two gate dielectric.

E. EARLY VOLTAGE (V_{EA})

The early voltage is a parameter describing the variation of the drain current in the active or saturation region of operation with V_{DS}. The early effect (V_{EA}) is related to the dependence of the width of the space charge layer upon the bias across it. And the voltage gain can rate an amplifying ability in terms of an output/input ratio. The early voltage (V_{EA}) [2] is the ratio

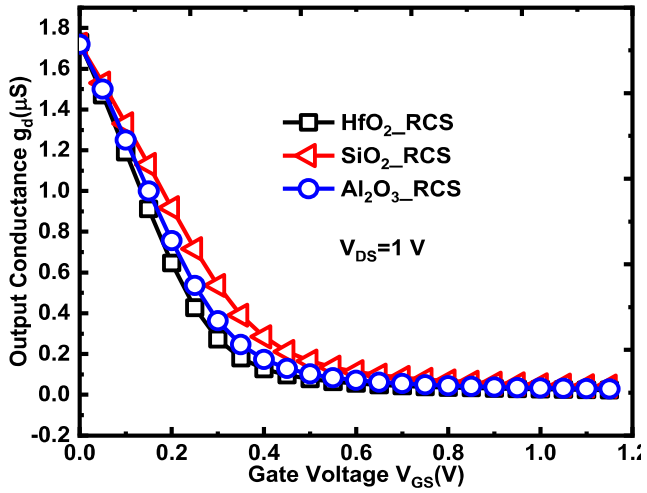

FIGURE 15. Output Conductance plot of three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2 and Al_2O_3 gate dielectric.

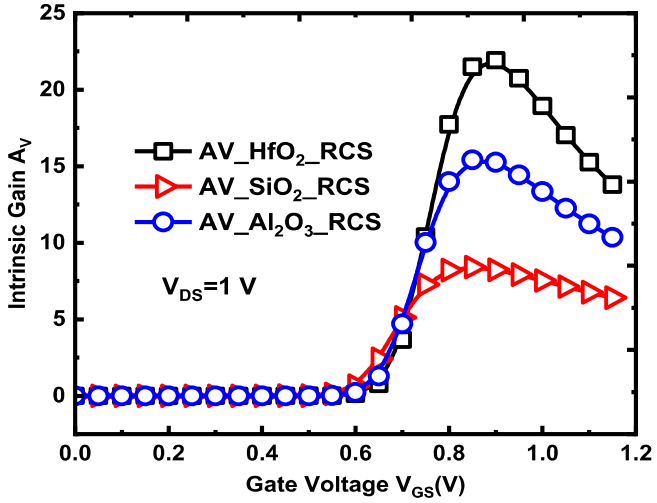

FIGURE 16. Intrinsic Gain (*Av*) plot of three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2 and Al_2O_3 gate dielectric.

of I_{DS} upon g_d is given by

$$VEA = \frac{\mathrm{ID}}{\mathrm{gD}} \tag{11}$$

Fig 14 shows the early voltage plot for three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2, and Al_2O_3 gate dielectric. With RCS-HfO_2 shows high V_{EA} value than the other two gate dielectrics.

F. CMOS CIRCUIT APPLICATION

To evaluate the viability of our model into circuit applications. Both the N-type and P-type of three fins vertically stacked QGOSJLNS with RCS are simulated for HfO_2, SiO_2, and Al_2O_3 as the gate dielectric. Then, for each of the three dielectric material devices, the linear and saturation region at 0.1V and 1V constant V_{DS} are simulated, with V_{GS} varied from 0V to 1.2V. The results show that all three structures are matched for I_{DS} versus V_{GS} with the same origin and nodes of both devices, the results are plotted in Fig 15 and Fig 16.

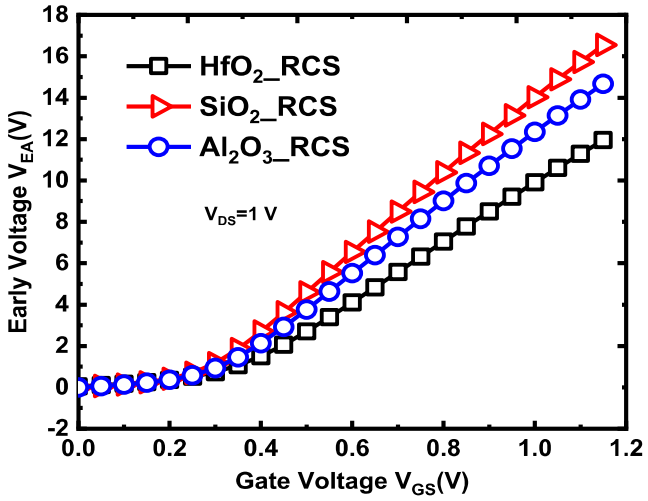

FIGURE 17. The early Voltage (V_{EA}) plot of three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2 and Al_2O_3 gate dielectric.

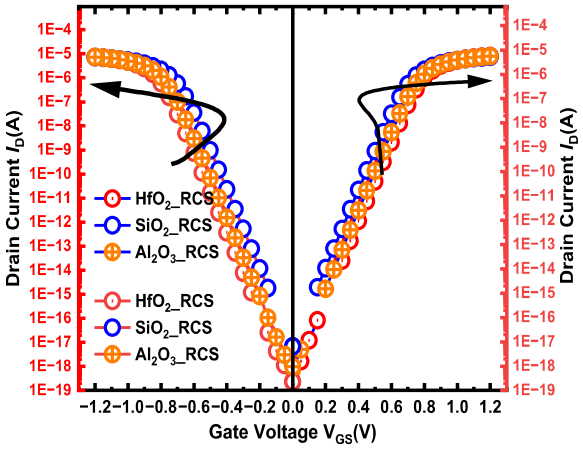

FIGURE 18. The IDS-VGS plot for N-type and P-type of three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2 and Al_2O_3 gate dielectric in the linear region.

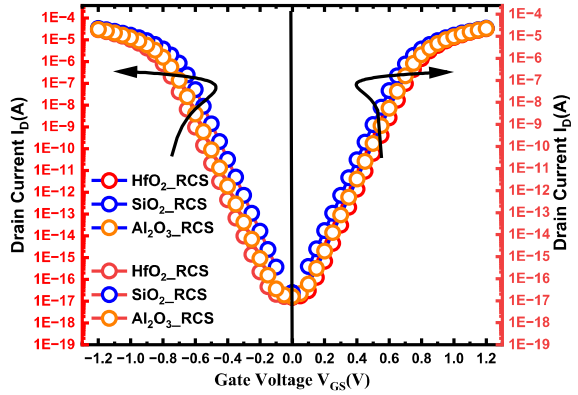

FIGURE 19. The $I_D - V_{GS}$ plot for N-type and P-type of three fins vertically stacked QGOSJLNS with RCS for HfO_2, SiO_2 and Al_2O_3 gate dielectric in Saturation region.

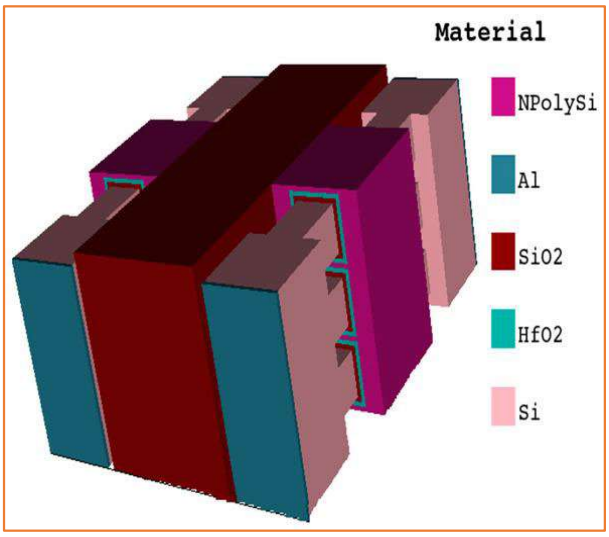

FIGURE 20. Three-dimensional view of three fins vertically stacked QGOSJLNS with RCS Inverter.

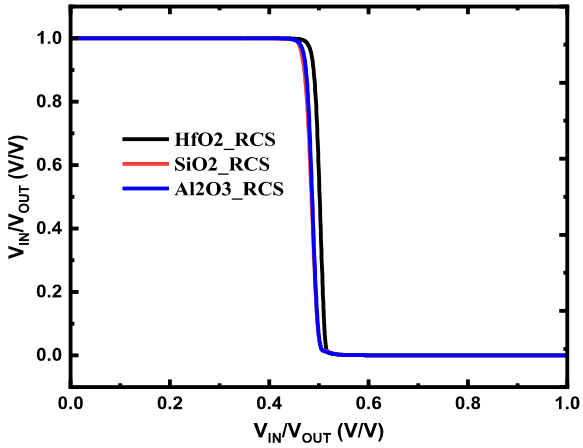

FIGURE 21. The CMOS inverters DC characteristics at V_{DD} = 1V.

TABLE 7. Comparison Table with exiting FETs.

Device	I_{OFF}(A)	I_{ON}(A)	I_{ON}/I_{OFF} (10^{14})	Circuit
Double Gate FET [23]	2.7E-21	1.37E-05	0.045	-
Nanowire [24]	4.3E-19	4.176E-6	0.0965	-
QGOSJLNS [proposed]	6.913E-21	2.408E-07	0.418	CMOS

The 3D view of three fins vertically stacked QGOSJLNS with RCS inverter is shown in Fig 17. The voltage transfer Characteristics (VTC) of three fins vertically stacked QGOSJLNS with RCS for HfO_2 as gate dielectric-based inverter has been considerably enhanced as compared to the SiO_2, Al_2O_3 as gate dielectric and conventional three fins vertically stacked QGOSJLNS inverters. The outcome of inverters reveals that a three fin vertically stacked QGOSJLNS with RCS for HfO_2 as gate dielectric-based inverter produces a more accurate DC characteristics curve and SNM plot, as illustrated in Figs 18 and 19.

The table 7 depicts the comparison of the proposed device with existing FETs towards device and circuit perspective.

IV. CONCLUSION

In this paper, we propose a novel structure with an opposing type doping core in the NMOS silicon body in this work. In comparison to a conventional model, the suggested RCS design has a greater I_{ON}/I_{OFF} ratio, lower I_{OFF}, lower threshold voltage, improved DIBL, and near to the optimal value of sub threshold slope for Nano scale size. In addition, we investigated the effect of rectangular core/shell thickness on RCS design and found that for a channel length of 30nm, a thinner core should be selected for better device performance. Therefore, three fins vertically stacked QGOSJLNS with RCS of N-type and P-type with HfO_2 as gate dielectric structure can be promising and an alternative to the conventional Quad gate structure. We also studied three inverters constructed by newly proposed structures of NMOS and PMOS three fins vertically stacked QGOSJLNS with RCS for a different gate dielectric. The simulation results show that three fins vertically stacked QGOSJLNS with RCS for HfO_2 as a gate dielectric exhibits better performance than the other two inverters. Finally, the suggested structure has lower leakage current and improved performance, making it a good contender for future low-power technologies.

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VAKKALAKULA BHARATH SREENIVASULU (Member, IEEE) received the B.Tech. and M.Tech. degrees from JNTU Anantapur, Andhra Pradesh, India, and the Ph.D. degree from NIT Warangal. He completed his Postdoctoral Research with IIT Patna. He is currently an Assistant Professor with the ECE Department, Manipal Institute of Technology Bengaluru, Karnataka, India. Some of his works are recognized as the most popular and top-cited list of articles in IEEE TRANSACTIONS ON ELECTRON DEVICES, IEEE ACCESS, and *Microelectronics Journals*. Towards his profile, he has 36 publications, which are indexed in SCI databases. He has been listed in Stanford/Elsevier's top 2% list of scientists, in 2024.

M. PRASAD (Member, IEEE) received the B.E. degree in electronics and communication engineering and M.Tech. degree in VLSI design and embedded system from VTU, Belgaum, Karnataka, India, in 2009 and 2013, respectively, and the Ph.D. degree from the Department of Electronics and Communication Engineering, VTU, in 2022. His research interests include nanotechnology, semiconductor devices, and low-power VLSI design.

EPURI DEEPTHI received the B.Tech. degree in electronics and communication engineering and M.Tech. degree in VLSI from JNTU Hyderabad, India, in 2012 and 2014, respectively. She is currently pursuing the Ph.D. degree with Anna University, Tamil Nadu. She is an Assistant Professor with the Malla Reddy Engineering College, Hyderabad. Her research interests include cyber security, network on-ship architecture design, nano-scale device modeling, and low-power VLSI design.

ARURU SAI KUMAR (Member, IEEE) received the B.Tech. degree in electronics and communications engineering from JNTU Hyderabad, India, in 2008, and the M.Tech. degree in VLSI design from VIT University, Vellore, India, in 2010, and the Ph.D. degree in VLSI design from the National Institute of Technology, Warangal, in 2022. He is currently an Assistant Professor with the VNR Vignana Jyothi Institute of Engineering and Technology, Hyderabad. His research interests include network-on-chip architecture design, application mapping in 2-D and 3-D environments, low-power VLSI design, and nanoscale device modeling (i.e. FinFET, nanowire FET, and nanosheet FET devices).

S. SUDHEER MANGALAMPALLI (Member, IEEE) is currently an Associate Professor with the Department of Computer Science and Engineering, Manipal Institute of Technology Bengaluru, Manipal Academy of Higher Education. He is a Passionate Researcher. Towards his profile, he has 34 publications, which are indexed in Scopus and SCI databases. His research interests include cloud computing, edge computing, fog computing, and machine learning. He is a reviewer of various SCI-indexed journals.