

Effect of physical parameters on the drain characteristics of Double gate MOSFET incorporating Quantum Mechanical Effects

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Abstract. Scaling of bulk MOSFETs in nanometre regime has several disadvantages. The electrical behaviour of the devices doesn't show the anticipated characteristics if scaling is done beyond certain point. But in order to have smaller devices with higher density on chips, it is necessary to avoid short channel effects (SCE) which lead to unexpected electrical features. One of the methods to avoid SCE is to have multi-gate architecture of MOSFET. This paper investigates the behaviour of double-gate MOSFETs with respect to the variation of their physical dimensions. The analyses have been done taking into notice the quantum mechanical effects due to dimensions in nanometre scale. The results obtained highlight how subthreshold and above threshold regions are impacted due to the various physical quantities that have been varied.

1. Introduction

By reducing the dimensions of MOSFETs, more number of components can be incorporated on a VLSI [1, 2] chip to have diversified applications. Adjusting short-channel effects (SCE) is the major issue during scaling down of conventional MOSFETs. There are several ways through which SCE can be lessened while reducing the dimensions of a device. There are many prominent techniques to overcome these shortcomings. Use of strain as reported in [3-5] alleviates SCE and boosts electrical integrity. Similar advantages have been found through the use of junctionless transistors [6-8]. Use of multiple gates has been reported in [9-12]. The core theme of all these methods is to enable gate electric field to be more dominant in the channel region. Proper lithographic techniques are used to enable these methods.

