Software defined Network on chip scheduler design for Quality of service in multimedia communication

File Number : CRG/2022/004582

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Submission Date : 30-Apr-2022

PROPOSAL DETAILS

(CRG/2022/004582)

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Technical Details :

Scheme : Core Research Grant

Research Area : Electrical Electronics & Computer Engineering (Engineering Sciences)

Duration : 36 Months **Contact No :** +917842288040

Date of Birth : 01-Apr-1974

Nationality : INDIAN **Total Cost (INR) :** 25,74,139

Is PI from National Laboratory/Research Institution ? No

Project Summary :

In context to the developed approaches in recent time, it is observed that software defined Network on chip (SDNoC) is an emerging approach for optimal network performance in upcoming applications. In realizing the SDNoC operation, system on chip (SoC) design was proposed for integration of multiple processors (MPSoC) for faster and accurate router designing. Design methods for traffic interconnection management, latency minimization, and power minimization were developed in recent past. The SDNoC is developed as an integrated of software defined controllers and NoC design in providing optimal traffic flow and high system performance. However, the external interface an issue of network delay and complex computation in monitoring multiple parameters simultaneously. The switching overhead and system dependency are a considerable factor in NoC design. To alleviate the issue an integrated System on chip (SoC) design for SDNoC is focused in this proposed work. The proposed design address the operation of a SDNoC architecture for monitoring of quality of service, routing overhead, switch controlling, and latency minimization using a multi core processor SDNoC design

Objectives :

- Providing high throughput to existing NoC, interfaced in multimedia data exchange.
- Providing standalone controlling to traffic controlling using integrated scheduler in NoC.
- Developing a real time interface in chip level for software defined network on chip (SDNoC).
- Developing a system on chip (SoC) modeling for SDNoC offering traffic control in multimedia communication.
- Integrating video frame compression and interpolation approach in SDNoC for high throughput system.

Keywords :

SDNoC , SoC , Latency , MPSoC , QoS , NoC

Expected Output and Outcome of the proposal :

The proposed approach outcome with a compact SoC design of software defined network on chip (SDNoC). The proposed design provides feasibility on integrating SDNoC for multimedia traffic in remote applications. The software control design and scheduler unit, control the operation with current state monitoring of network condition resulting in higher accuracy and network throughput. The proposing system will be useful in various applications such as providing high resolution presentation of E-Library, lecture Notes and live online presentation in academic applications at stand alone device level.

Suitability of the proposed work in major national initiatives of the Government:

Digital India

Theme of Proposed Work:

Cyber Physical Systems including AI, IOT and Cyber Security

Collaboration Details for last 5 Years :

Planned Collaboration for the proposed work with any foreign scientist/ institution ? **No**

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1	 **A Kumar** pradeepsujeeth@gmail.com ASSOCIATE PROFESSOR(ELECTRONICS AND COMMUNICATION ENGINEERING) **Malla Reddy Engineering College** Maisammaguda, Dhulapally (Post via. Kompally), Secunderabad, Rangareddy Dt, TELANGANA, HYDERABAD D.O.B : 03 Jun, 1982

Other Technical Details

Project Title: Software defined Network on chip scheduler design for Quality of service in multimedia communication

1. Origin of the Proposal:

With rapid increase in the demand of data exchange over wireless network, new designs for faster, accurate and efficient exchange is needed. Network on Chip (NoC) has emerged as a optimal solution in providing a faster and efficient data exchange in recent time. NoC are designed to achieve the desired level of operation and service quality in constraint resources and power supply. In the communication network, there are major concerns been observed using bus system. Various advantages were observed with the incorporation of network on chip (NoC) at chip level integration. Network on chips design are developed to offer scalability and high end performance.

The system on chip (SoC) design developed with a physical design offers a large guarantee in offered service for specific applications. Network on chip are needed to control for its operation via controller unit. Software defined network (SDN) are a major evolution in the area of network management for traffic control operation. This offers a simplified means of control operation and device implementation. SDN integrate the controller in a centralized mean for network operation in a wide distributed network. It can be developed for decision making more optimal with operating information for a better operation performance.

SDN offers a feasibility of integration for different vendor's devices with a simplified control operation. The advantage of SDN and NoC design has brought out the system of software defined network on Chip (SDNoC) which offers a high reliability in traffic management offering flexibility in runtime interface with self adaptive nature. This interface results into a lower hardware complexity in router designing. This SDNoC operates with an external controller interface which observes the offered quality of service (QoS), power utilization, traffic flow and faults in the network.

The rise in the user accessing and large volume of data exchange constraint the network for limited usage. The existing resource control mechanisms were depended on a centralized monitoring in a software driven environment. These methods are dependent on the connectivity and controlling algorithms which in many cases are subjected to disconnection due to high traffic, or interferences. This motivate in developing a standalone monitoring and control interface in a standalone mode avoiding the dependency

of external interfaces. This proposed work focus on developing a System on chip (SoC) design for software defined network on chip (SDNoC) with the operation of resource allocation and interpolation for quality service in multimedia traffic.

2. Review of status of Research and Development in the subject

System on chip design is targeted for a large integration density in the network with large interconnection which is required to control for faster and higher throughput performance. The current designs of network on chip (NoC) were developed based on the multi core chips architecture. The design architecture was developed in a general purposed mode termed chip multi processor or in a heterogeneous manner which are specific to an application using multi processor system on chip (MPSoC) approach.

A key issue in the design of any multi core unit is the scalability at system level interconnections and controlling. This issue is also observed in the design of upcoming integration in Field-Programmable Gate Arrays (FPGAs). Approaches for developing System on chip design for NoC were outlined in following section.

2.1 International Status:

Many integration and design modules are commercialize in current usage. in the integration of network on chip at system on chip level, third party vendors IP are used for NoC interface. AMBA network interconnect from ARM [1] provides a IP library which defines the crossbars and bridges in developing interconnects to form NoC operation. The interconnects are designed at floor panning and buffering operation is presented in providing stall operation.

A mesh network interface is developed in Tilera TILE-Gx processor [2] which is consisting of 100 core processors. The interconnects are connected in a 2D mesh structure to provide a NoC operation. Intel's Teraflops [3] is a similar design w2ith 80 core processor design interconnected with mesh type interconnection. Using TI OMAP a NoC interconnect is developed for Arteris [4]. Other prototype such as TRIPS processor [5], and smart memories [6] interconnect the cores using NoC interface.

A Flexible Architecture of Unified Systems for Telecom (FAUST) using GALs and DSPIN is presented in [7]. This network interconnect is implement in a quasi-mesh network with routers connected in multiple core units. approaches of NoC design by BONE NoC group is developed using parallel processing for visual attention engine and

recognition process [8,9]. The bus architecture in such system has migrated to a bridge or multi layer bus system. The design is has a several level of bus hierarchy for complex operation. a large chip cores area observed in the TI's OMAP [10], Infineon XMM/X-Gold [11] or ST's Nomadik [12].

In the operation of NoC, many designs are developed for a synchronous operation such as ×pipes [13], NOSTRUM [14], Spidergon [15]. Under asynchronous operation, system such as Mango [16], FAUST [17] and ANOC [18] are developed. Various other system are developed in monitoring the quality based operation using specified design such as Æthereal [19], QNoC [20].

To automate the NoC operation, various research have been focused which include the issues of routing, topology, QoS, congestion in the router design. Mapping method on the multi core design is addressed in [21, 22]. Application specific design in ×pipes Compiler [23] and follow-up tools [24] were developed with heterogeneous topologies which are used for traffic management and design approach.

Operation of network on chip is optimized for power consumption using buffer management in a network on chip (NoC) design [25]. In developing power ui8tlization minimization traditional methods used a buffer less router, which routes the traffic to minimize contentions. However, the rapid increase of network traffic in a random manner degrades the operation. A modified buffer less traffic flow using partial buffering using critical and hierarchical interconnection is addressed in [25]. The partial traffic control offers a minimization of power consumption however the quality of the data flow is undressed.

In recent software defined network platform named Orion [26] is used for Google data enter (Jupiter) and wide area (B4) network. Orion was developed for a modular and micro service application which protects the system from large scale traffic in the network. In recent development advanced wireless system such as RT-WiFi attains a good real time performance in data speed and communication performance. In [27] a software defined communication using RT-WiFi is developed termed SRT-WiFi in providing full range communication in high speed real communication.

In developing the operational performance of the network on chip and multi-core design for NoC following mesh topology was introduced in [28]. This approach minimized the power consumption by using a inter communication among different cores in a close

interconnection. A FPGA design for network accelerator is developed in [29] for software based programmability for network traffic flow. Advanced approach of machine learning [30] was introduced in recent for software defined network (SDN) in power management, and operation control. A multi processor design for software defined network on chip (SDNoC) was proposed in [31] to interface the emerging cloud of chips (CoC) for flexible communication.

Various organizations such as Arteris [4], iNoCs [32], Silistix [33] have outcome with new tools for NoC design. This tool provides an interface for core type such as master or slave mode and the protocol used in communication. The tool provides a feasibility of interface for bandwidth, type of core used, system latency, QoS offered and traffic flow. A summary of the development in the NoC design in recent past by different organization is listed in table 1.

Table 1. Industrial Developments of NoC

Design	**Organization**	**Core deigns**	**Developing year**
vesrsal	Xilinx	NA	2020
Epiphany-V	Adapteva	RISC-V Core	2020
Loihi	Intel	Neuromorhic core	2020
Cloud A100	Qualcomm	Neural processor	2020
True north	IBM	Neurosynaptic core	2019
DaVinci Ascend 910	Huawei	Da Vinci core	2019

Internet Research Task Force (IRTF) has outcome with a international group of vendors, network designer, researcher which has developed a SDN research group (SDNRG) which work on the issue of cloud processing and routing control [34]. SDNRG has developed Interface to Routing System (I2RS) for interface of network controller for management of service application.

European Telecommunications Standards Institute (ETSI) outcome with an Industry Specification Group (ISG) for Network Functions Virtualization (NFV) [35]. NFV is developed as a corresponding technology to SDN for the visualization of network

framework for deployment of communication services. The International Telecommunications Union (ITU) has outcome with a joint coordination Committee (JCA) for SDN called JCA-SDN [36,37] which keeps a track on the development of research in the area of SDN.

2.2 National Status:

In recent advancement in NoC design has gained a lot interest due to the high service demand and automation of large traffic flow in the network. NoC are been proposed in various real time applications such as the Medical, automotive, institutional management, e-learning, data sharing etc. in optimizing the interface of NoC into real time application a Intellectual Power-Aware Routing(IPAR) was presented by [38]. This design is developed with the objective of providing dynamic and scalable resource utilization in NoC design.

In the design of NoC at System-on-Chip (SoC) a reconfigurable X-tolerant trace compressor [39] for observing the operation of device for post silicon validation is presented. The presented approach minimizes the trace overhead in testing and fault diagnosis in NoC design by a compression method developed. The simulation model developed on Xilinx tool which prevent the fault testing protection using tiling operation for avoiding recheck operation.

In improving the operation performance of NoC unit a virtual channel (VC) allocation in consideration to latency, power utilization and system throughput is presented in [40]. this approach presented the NoC operation using pipeline stage in minimizing the latency in comparison to conventional NoC design using tornado and transpose traffic design. The system attains a latency minimization of 58.57% in NoC design.

HDL modelling of SoC design for different network topologies is presented in [41]. The approach outlined methods for SoC based network topology design which improved the share bus system in interconnection for communication system.

A mesh topology based NoC design is developed in [42] for the design of network on chip (NoC). The design is developed in processing routing method for defined I/O ports on NoC design. The topology is developed for a scalable and simpler mode of operation. Four way switches are used in the process of port computing in NoC operation. The mesh topology is developed using a look up table (LUT) design for enhancement of routing process. The LUT are used by the virtual circuit interface (VCI) in scheduling the packet forwarding.

A security method in NoC option using data encryption-decryption called enhanced TACIT (E-TACIT) [43] for routing operation is presented. This approach outlines a method for protection of three dimensional routers in NoC design using HASH function based operation. The presented method is developed to resolve the issue of key and block size constraint in NoC design. It is developed as a generalized n-key, n-block operation. The NoC design is developed for Internet-of -Thing (IoT) interface. This design offers a high scalable design for low power utilization.

A Physical unclonable function (PUFs) in developing security interface for hardware security is outlined in [44]. This approach developed a PUF design for security usage in NoC design. The design outlines a method of re-usage of hardware resources and presented a design method for crossbar switches in NoC design. In another approach, a timing channel based security mechanism is developed in [45] for the security measure in NoC design.

The approach of security provisioning in NoC design which are developed for cloud-on-chip (CoC) in a multi-processor system-on-chip (MPSoC) design is presented in [46,47]. The design presented a CoC framework in developing scalable system. A Software defined Network on chip (SDNoC) is outlined a flexible and scalable design for a large distributed system. The system developed the method of secure interconnection communication between the devices for CoC security system using SDNoC approach.

2.3 Importance of the proposed project in the context of current status

In context to the developed approaches in recent time, it is observed that software defined Network on chip (SDNoC) is an emerging approach for optimal network performance in upcoming applications. In realizing the SDNoC operation, system on chip (SoC) design was proposed for integration of multiple processors (MPSoC) for faster and accurate router designing. Design methods for traffic interconnection management, latency minimization, and power minimization were developed in recent past. The SDNoC is developed as an integrated of software defined controllers and NoC design in providing optimal traffic flow and high system performance. However, the external interface an issue of network delay and complex computation in monitoring multiple parameters simultaneously. The switching overhead and system dependency are a considerable factor in NoC design. To alleviate the issue an integrated System on chip (SoC) design for SDNoC is focused in this proposed work. The proposed design address the operation of a

SDNoC architecture for monitoring of quality of service, routing overhead, switch controlling, and latency minimization using a multi core processor SDNoC design. This suggested work improves the existing SDNoC design with two aspects;

i) Providing high throughput to existing NoC, interfaced in multimedia data exchange.

ii) Providing standalone controlling to traffic controlling using integrated scheduler in NoC.

The proposed work, aims in eliminating routing overhead observed in multi core operation in bus hierarchies. The proposing system develops integration, controlling and resource utilization in a centralized manner resulting in more accurate operation. The interpolation model integrated into the SDNoC unit will offer a higher utilization of integrated device memory for large data storage and communication with higher visual quality.

3. Work Plan:

3.1 Methodology:

The proposed work, focus on developing a SDNoC architecture for integrated operation of monitoring quality of service, routing and latency issue. A scheduler design with data interpolation is proposed in performing the option of software defined option in a SoC unit. A framework for the proposed approach is shown in figure 1.

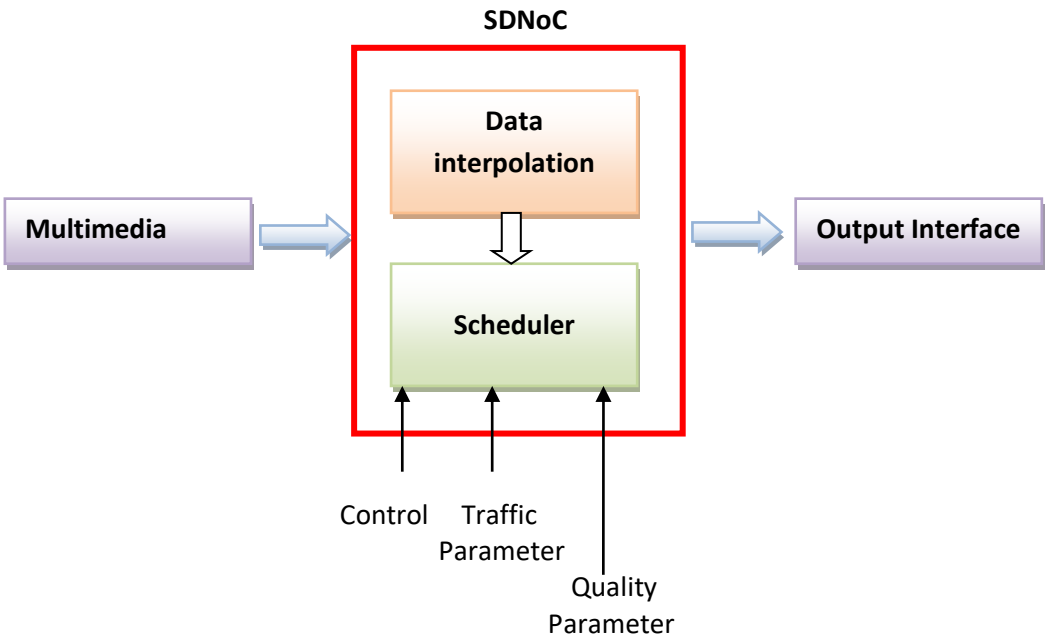

Figure 1. Proposed SDNoC framework

The Proposed architecture of SDNoC will interface multimedia data from capturing device and interface to SDNoC chip. The Data interpolation unit transform the video input into low resolution (LR) frames for storage or communication. A Scheduler unit reads the current traffic parameters and quality parameters for control of resource in data exchange. The scheduler unit control the allocation based on the load and interference in the network, derived from traffic parameter. The output interface is programmed with projection algorithm in interpolation of the LR frame to original size for display.

The data interpolation unit perform a frame transition where each frame is extracted and projected to a lower scale level grid for Low resolution (LR) interpolation. The projection is proposed to develop in spectral domain and stored as compressed data. The scheduler unit performs a computation on resource allocation by monitoring the current traffic condition and inference level.

The data interpolator is proposed to develop a grid mapping for transforming processing frame data for different resolutions. The spectral domain interpolation using fast Fourier transformation (FFT) is proposed. The spectral domain interpolation interpolates the data into a higher grid based on the scaling parameter and is more efficient in preserving the edges and finer detail in comparison to spatial pixel interpolation. The proposed approach of interpolation is shown in figure 2.

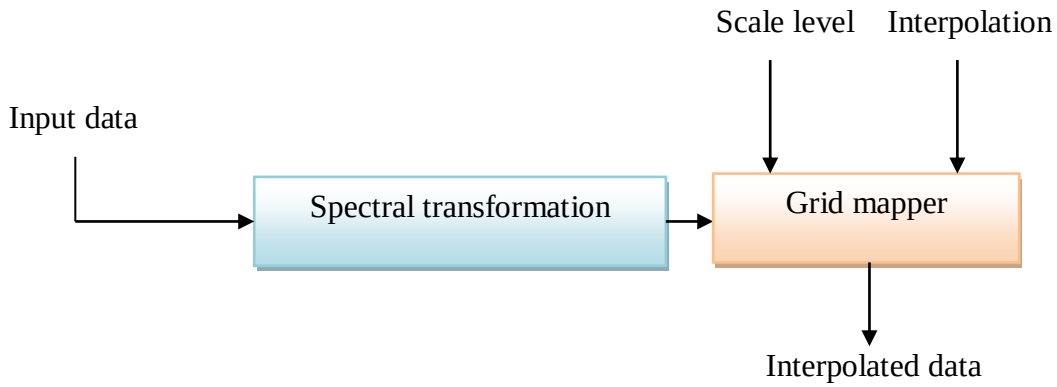

Figure 2. Functional units of proposed data interpolation block

The interpolation offers multiple benefits of data rate controlling, interference mitigation and higher system throughput. In controlling the routing overhead, the control operation performs a scheduling operation based on pooling logic. This unit will process

on the active traffic condition in allocation of data bandwidth for data exchange. The unit performs a multi factor analysis in allocation of resource which includes the monitoring of traffic overhead, interference in channel and demanded quality of service. The proposed scheduler unit also control the interconnection data flow control among different processing units. The proposed approach of the scheduler unit is presented in figure 3.

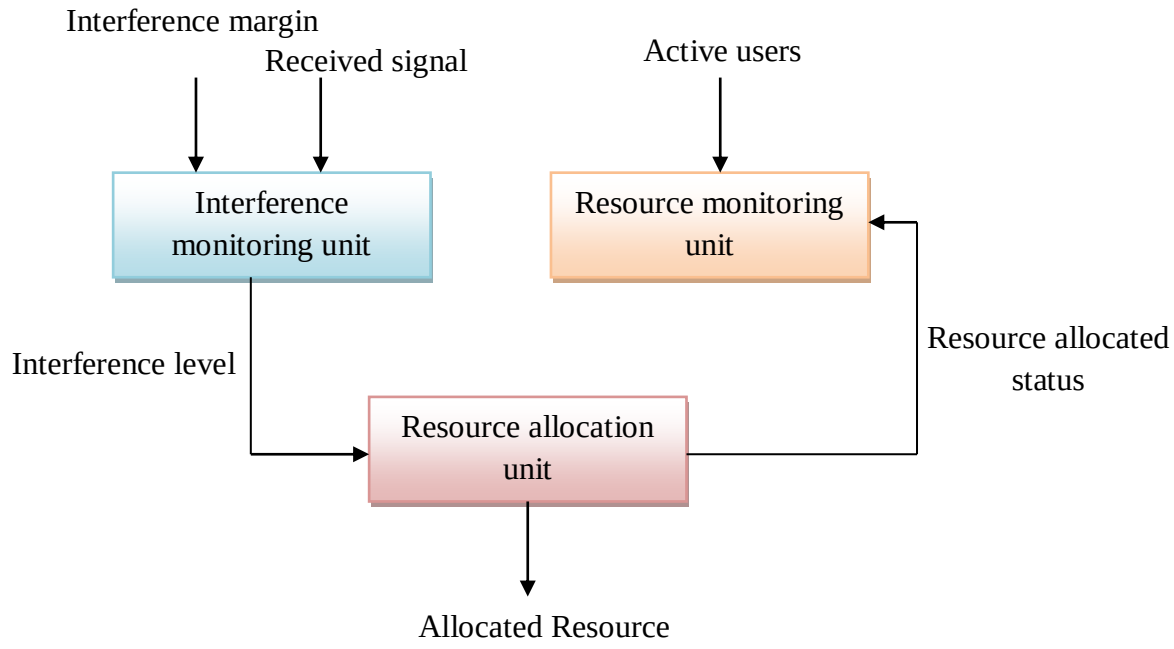

Figure 3. Proposed architecture of scheduler unit in SDNoC design

3.3 Suggested Plan of action for utilization of research outcome expected from the project.

The proposed design outcome with a compact SoC design of software defined network on chip (SDNoC). This design provides feasibility on integrating SDNoC for multimedia traffic in remote applications. The software control design and scheduler unit, control the operation with current state monitoring of network condition resulting in higher accuracy and network throughput. The proposing system will be useful in various applications such as providing high resolution presentation of E-Library, lecture Notes and live online presentation in academic applications at stand alone device level.

In utilization of the presented work, an interface for the proposed system SDNoC will be developed with all departments and library in the institution. The interface will be used for exchange of learning resources presented as video and audio input from different departments to share information's in campus with standalone device monitoring

3.2 Time Schedule of activities giving milestones through BAR diagram.

SNo.	Activity	Months					
		1-6	7-12	13-18	19-24	25-30	31-36
1.	Literature and system design						
2.	Algorithm developments and analysis						
3.	Software Implementation and simulation						
4.	Device programming and practical testing						
5.	Report drafting and publications						

3.4Environmental impact assessment and risk analysis. – NA

4. Expertise:

4.1 Expertise available with the investigators in executing the project:

4.2 Summary of roles/responsibilities for all Investigators:

S.No.	Name of the Investigators	Roles/Responsibilities
1.	Dr Shaik Fairooz	• Modeling , Algorithm and Simulation
2.	Dr A Pradeep Kumar	• Modeling , Algorithm and Simulation

4.3 Key publications published by the Investigators pertaining to the theme of the Proposal during the last 5 years.

[1] S.K.Fairooz and Dr.B.K.Madhavi , “Cross Layer Soc Design For Scalable Video Streaming”, International Conference on Advances in Engineering, Science and Management ,IEEE-(ICAESM -2012),pp 67-72, IEEE-2012.
[2] S.K.Fairooz and Dr.B.K.Madhavi , “Resolution and Scaling Video Coding For SoCs in Digital Modeling”,International Journal of Information and EducationTechnology, Vol. 2, No. 5, pp 490-493, Impact Factor :0.477, 2012.
[3] S.K.Fairooz and Dr.B.K.Madhavi , “ SoC Modeling for video coding with superscalar Projection” , Proceedings of the Second International Conference on Advances in Computing and Information Technology (ACITY) Vol2, AISC 177, pp.787-795,springer-2013.
[4] S.K.Fairooz and Dr.B.K.Madhavi ,”Reliable Error Free Coding For Resource Constraint Soc Design”, International Journal of Advanced Computing, Vol.46, Issue.3 ,Impact Factor : 1.2 ,2013.
[5] Shaik Fairooz, “

4.4 Bibliography

[1] http://www.arm.com/products/system-ip/amba/amba-open-specifications.php
[2] http://www.tilera.com/products/processors.php

[3] S. R. Vangal, et al. “An 80-Tile sub-100-w teraflops processor in 65-nm cmos”, Solid-State Circuits, IEEE Journal of, 43(1):29–41, 2008.

[4] http://www.arteris.com/flex_noc.php

[5] Gratz, Paul, Changkyu Kim, Karthikeyan Sankaralingam, Heather Hanson, Premkishore Shivakumar, Stephen W. Keckler, and Doug Burger. "On-chip interconnection networks of the TRIPS chip." IEEE Micro 27, no. 5 (2007): 41-50.

[6] Chen, Hui, Peng Chen, Jun Zhou, Luan HK Duong, and Weichen Liu. "ArSMART: An improved SMART NoC design supporting arbitrary-turn transmission." IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (2021).

[7] Miro-Panades, I. et al., “Physical Implementation of the DSPIN Network-on-Chip in the FAUST Architecture", NoC Symposium , 2008.

[8] Ziabari, Amir Kavyan, José L. Abellán, Yenai Ma, Ajay Joshi, and David Kaeli. "Asymmetric NoC architectures for GPU systems." In Proceedings of the 9th International Symposium on Networks-on-Chip, pp. 1-8. 2015.

[9] Bahn, Jun Ho, Seung Eun Lee, Yoon Seok Yang, Jungsook Yang, and Nader Bagherzadeh. "On design and application mapping of a Network-on-Chip (NoC) architecture." Parallel Processing Letters 18, no. 02 (2008): 239-255.

[10] J. Helmig, “Developing core software technologies for TI’s OMAPTM platform”, Texas Instruments, 2002. Available at http://www.ti.com.

[11] http://www.infineon.com/cms/en/corporate/press/news/releases/2006/170186.html

[12] A. Artieri, V. D Alto, R. Chesson, M. Hopkins, M. C. Rossi, “Nomadik Open Multimedia Platform for Next-generation Mobile Devices”, STMicroelectronics Technical Article TA305, 2003, available at http://www.st.com

[13] Stergiou, Stergios, Federico Angiolini, Salvatore Carta, Luigi Raffo, Davide Bertozzi, and Giovanni De Micheli. "/spl times/pipes Lite: a synthesis oriented design library for networks on chips." In Design, Automation and Test in Europe, pp. 1188-1193. IEEE, 2005.

[14] Lu, Zhonghai, Rikard Thid, Mikael Millberg, Erland Nilsson, and Axel Jantsch. "NNSE: Nostrum network-on-chip simulation environment." In Swedish system-on-chip conference. 2005.

[15] M. Coppola., “Spidergon: a novel on-chip communication network”, Proc. IEEE International Symposium on System-on-Chip 2004. 16–18, p. 15, Nov. 2004.

[16] Bjerregaard, Tobias, and Jens Sparsø. "Implementation of guaranteed services in the MANGO clockless network-on-chip." IEE Proceedings-Computers and Digital Techniques 153, no. 4 (2006): 217-229.

[17] Miro-Panades, Ivan, Fabien Clermidy, Pascal Vivet, and Alain Greiner. "Physical Implementation of the DSPIN Network-on-Chip in the FAUST Architecture." In Second ACM/IEEE International Symposium on Networks-on-Chip (nocs 2008), pp. 139-148. IEEE, 2008.

[18] E. Beigne et al., “An Asynchronous NoC Architecture Providing Low Latency Service and its Multi-Level Design framework”, ASYNC’2005, pp. 54-63, March 2005.

[19] Goossens, Kees, John Dielissen, and Andrei Radulescu. "Æthereal network on chip: concepts, architectures, and implementations." IEEE Design & Test of Computers 22, no. 5 (2005): 414-421.

[20] E. Bolotin, I. Cidon, R. Ginosar, A. Kolodny, "QNoC: QoS architecture and design process for Network on Chip", The Journal of Systems Architecture, pp. 105-128, Vol. 50, Issue: 2-3, Feb 2004.

[21] M. Taylor et al., "The Raw Microprocessor: A Computational Fabric for Software Circuits and General Purpose Programs", IEEE Micro, April 2002.

[22] Huang, C.H. HDA: Hierarchical and dependency-aware task mapping for network-on-chip based embedded systems. J. Syst. Archit. 2020, 108, 101740.

[23] Jalabert, Antoine, Srinivasan Murali, Luca Benini, and Giovanni De Micheli. "xpipesCompiler: A tool for instantiating application-specific Networks on Chip." In Design, Automation, and Test in Europe, pp. 157-171. Springer, Dordrecht, 2008.

[24] Ogras, Umit Y., Jingcao Hu, and Radu Marculescu. "Key research problems in NoC design: a holistic perspective." In Proceedings of the 3rd IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis, pp. 69-74. 2005.

[25] Ausavarungnirun, Rachata, and Onur Mutlu. "Energy-Efficient Deflection-based On-chip Networks: Topology, Routing, Flow Control." arXiv preprint arXiv:2112.02516 (2021).

[26] Ferguson, Andrew D., Steve Gribble, Chi-Yao Hong, Charles Killian, Waqar Mohsin, Henrik Muehe, Joon Ong et al. "Orion: Google's {Software-Defined} Networking Control Plane." In 18th USENIX Symposium on Networked Systems Design and Implementation (NSDI 21), pp. 83-98. 2021.

[27] Yun, Zelin, Peng Wu, Shengli Zhou, Aloysius K. Mok, Mark Nixon, and Song Han. "RT-WiFi on Software-Defined Radio: Design and Implementation." arXiv preprint arXiv:2203.10390 (2022).

[28] Salh, Walid Mokthar, and Azeddien M. Sllame. "Applying Genetic Algorithm to Solve Partitioning and Mapping Problem for Mesh Network-On-Chip Systems." International Journal of Computer Science & Information Technology (IJCSIT) Vol 13 (2021).

[29] Lai, Yi-Hsiang, Ecenur Ustun, Shaojie Xiang, Zhenman Fang, Hongbo Rong, and Zhiru Zhang. "Programming and Synthesis for Software-defined FPGA Acceleration: Status and Future Prospects." ACM Transactions on Reconfigurable Technology and Systems (TRETS) 14, no. 4 (2021): 1-39.

[30] Jurado Lasso, F. FERNANDO, Letizia Marchegiani, J. F. Jurado, A. A. Mahfouz, and X. Fafoutis. "A Survey on Software-Defined Wireless Sensor Networks: Current status, machine learning approaches and major challenges." TechRxiv (2021).

[31] Gomez-Rodriguez, Jose Ricardo, Remberto Sandoval-Arechiga, Salvador Ibarra-Delgado, Viktor Ivan Rodriguez-Abdala, Jose Luis Vazquez-Avila, and Ramon Parra-Michel. "A Survey of Software-Defined Networks-on-Chip: Motivations, Challenges and Opportunities." micromachines 12, no. 2 (2021): 183.

[32] http://www.inocs.com/

[33] http://www.silistix.com/

[34] Gomez-Rodriguez, Jose Ricardo, Remberto Sandoval-Arechiga, Salvador Ibarra-Delgado, Viktor Ivan Rodriguez-Abdala, Jose Luis Vazquez-Avila, and Ramon Parra-Michel. "A Survey of Software-Defined Networks-on-Chip: Motivations, Challenges and Opportunities." micromachines 12, no. 2 (2021): 183.

[35] Chen, Qianqiao, Vaibhawa Mishra, and Georgios Zervas. "Reconfigurable computing for network function virtualization: A protocol independent switch." In 2016 International Conference on ReConFigurable Computing and FPGAs (ReConFig), pp. 1-6. IEEE, 2016.

[36] Zhuang, Weihua, Qiang Ye, Feng Lyu, Nan Cheng, and Ju Ren. "SDN/NFV-empowered future IoV with enhanced communication, computing, and caching." Proceedings of the IEEE 108, no. 2 (2019): 274-291.

[37] Blanco, Bego, Jose Oscar Fajardo, Ioannis Giannoulakis, Emmanouil Kafetzakis, Shuping Peng, Jordi Pérez-Romero, Irena Trajkovska et al. "Technology pillars in the architecture of future 5G mobile networks: NFV, MEC and SDN." Computer Standards & Interfaces 54 (2017): 216-228.

[38] Mohanraj, S. "Intellectual Power Aware Routing (IPAR) methodology for configuring noc architecture." information technology in industry 9, No. 2 (2021): 1383-1392.

[39] Ponsudha, P. "A Novel Fault Zone Tiling Approach Based Error Correcting and Detecting Method for Network on Chip Design." Turkish Journal of Computer and Mathematics Education (TURCOMAT) 12, no. 12 (2021): 2873-2882.

[40] Katta, Monika, and T. K. Ramesh. "Latency improvement by using fill VC allocation for network on chip." In Data Engineering and Communication Technology, pp. 561-569. Springer, Singapore, 2021.

[41] Nagalaxmi, T., E. Sreenivasa Rao, and P. Chandrasekhar. "Design and Development of SOC Based Network on Chip Topologies." ICTACT Journal on Microelectronics 6, no. 4 (2021): 1041-1047.

[42] Rane, Udaysing V., Rajendra S. Gad, and Charanarur Panem. "Design of Network on Chip (NoC) Computing Node for Mesh Topology using Soft-core NIOS-II Processor." In Journal of Physics: Conference Series, vol. 1921, no. 1, p. 012075. IOP Publishing, 2021.

[43] Seetharaman, Gopalakrishnan, and Debadatta Pati. "Enhanced TACIT Encryption and Decryption Algorithm for Secured Data Routing in 3-D Network-on-Chip based Interconnection of SoC for IoT Application." Journal of Scientific and Industrial Research (JSIR) 80, no. 6 (2021): 520-527.

[44] Nagabhushanamgari, Prasad, Vikash Sehwag, Indrajit Chakrabarti, and Santanu Chattopadhyay. "Embedding delay-based physical unclonable functions in networks-on-chip." IET Circuits, Devices & Systems 15, no. 1 (2021): 27-41.

[45] Biswas, Arnab Kumar, and Biplab Sikdar. "Protecting network-on-chip intellectual property using timing channel fingerprinting." ACM Transactions on Embedded Computing Systems (TECS) 21, no. 2 (2022): 1-21.

[46] Sharma, Gaurav, Georgios Bousdras, Soultana Ellinidou, Olivier Markowitch, Jean-Michel Dricot, and Dragomir Milojevic. "Exploring the security landscape: NoC-based MPSoC to Cloud-of-Chips." Microprocessors and Microsystems 84 (2021): 103963.

[47] Haji, Saad H., S. R. Zeebaree, Rezgar Hasan Saeed, Siddeeq Y. Ameen, Hanan M. Shukur, Naaman Omar, Mohammed AM Sadeeq, Zainab Salih Ageed, Ibrahim Mahmood Ibrahim, and Hajar Maseeh Yasin. "Comparison of software defined networking with traditional networking." Asian Journal of Research in Computer Science (2021): 1-18.

Other references:

5. List of Projects submitted/implemented by the Investigators

5.1 Details of Projects submitted to various funding agencies:
5.2 Details of Projects under implementation: NA
5.3 Details of Projects completed during the last 5 years: NA

6. List of facilities being extended by parent institution(s) for the project implementation.
6.1 Infrastructural Facilities

Sr. No.	Infrastructural Facility	Yes/No/Not required Full or sharing basis
1.	Workshop Facility	Yes
2.	Water & Electricity	Yes
3.	Laboratory Space/ Furniture	Yes
4.	Power Generator	Yes
5.	AC Room or AC	Yes
6.	Telecommunication including e-mail &fax	Yes
7.	Transportation	Yes
8.	Administrative/ Secretarial support	Yes
9.	Information facilities like Internet/Library	Yes
10.	Computational facilities	Yes
11.	Animal/Glass House	No
12.	Any other special facility being provided	Not required

6.2 Equipment available with the Institute/ Group/ Department/Other Institutes for the project:

Equipment available with	Generic Name of Equipment	Model, Make & year of purchase	Remarks including accessories available and current usage of equipment
PI & his group	Xilinx	ISE 9.1, 2015	Available
PI's Department	Computers	Core i5 Processors, 2018	Available
Other Institute(s) in the region	NA		

7.Name and address of experts/ institution interested in the subject / outcome of the project.

Prof B. Rajendra Naik
M.E, PhD
OU , ECE , Osmania University , Hyderabad.

Material list:

SNo.	Details	Costing per unit	Quantity
1	Xilinx ISE Design Suite 11.1	$2,995	1
2	Intel EPF10K50EQC240-3N FPGA - Field Programmable Gate Array	Rs.49,990.18	2
3	Ethereal (Wireshark)	$69.95	1
4	Sony HDRCX405 9.2MP HD Handycam Camcorder	Rs.40,999.00	1
5	HP All-in-One 24-dp0888in PC	Rs.58,999/-	2

Budget Details

Institution wise Budget Breakup :

Budget Head	Malla Reddy Engineering College	Total
Research Personnel	12,80,400	**12,80,400**
Consumables	65,000	**65,000**
Travel	65,000	**65,000**
Equipment	4,88,739	**4,88,739**
Contingencies	75,000	**75,000**
Other cost	3,00,000	**3,00,000**
Overhead	3,00,000	**3,00,000**
Total	**25,74,139**	**25,74,139**

Institute Name : ***Malla Reddy Engineering College***

Year Wise Budget Summary (Amount in INR) :

Budget Head	Year-1	Year-2	Year-3	Total
Research Personnel	4,09,200	4,09,200	4,62,000	**12,80,400**
Consumables	15,000	25,000	25,000	**65,000**
Travel	15,000	20,000	30,000	**65,000**
Equipments	4,88,739	0	0	**4,88,739**
Contingencies	25,000	25,000	25,000	**75,000**
Other cost	1,00,000	1,00,000	1,00,000	**3,00,000**
Overhead	1,00,000	1,00,000	1,00,000	**3,00,000**
Grand Total	**11,52,939**	**6,79,200**	**7,42,000**	**25,74,139**

Research Personnel Budget Detail (Amount in INR) :

Designation	Year-1	Year-2	Year-3	Total
Junior Research Fellow *Keep and maintain the record of the results in presentable form (Soft as well as hard copy). Keep a track of contingencies/consumables required for the work. Assist the PI in preparation of various reports related to the research work.*	4,09,200	4,09,200	4,62,000	**12,80,400**

Consumable Budget Detail (Amount in INR) :

Justification	Year-1	Year-2	Year-3	Total
Laboratory supplies, laboratory notebooks, printer paper for research data and reports, and so forth usually can be justified as consumable supplies.	15,000	25,000	25,000	**65,000**

Travel Budget Detail (Amount in INR) :

Justification (Inland Travel)	Year-1	Year-2	Year-3	Total
ravel is necessary to accomplish the grant objectives: Disseminate the project's research results by presenting.	15,000	20,000	30,000	**65,000**

Equipment Budget Detail (Amount in INR) :

Generic Name ,Model No. , (Make)/ Justification	Quantity	Spare time	Estimated Cost
FPGA - Field Programmable Gate Array EPF10K50EQC240-3N (Intel) *To model into FPGA*	2	100 %	**99,980**
Xilinx ISE Design Suite 11.1 Version 11.1 (Xilinx) *Tool for modeling and simulation*	2	100 %	**2,27,620**
Ethereal (Wireshark) *To support of Project*	2	0 %	**140**
HP All-in-One 24-dp0888in PC (HP) *To print for the Documentation*	2	100 %	**1,20,000**
Handycam Camcorder Sony (HDRCX405 9.2MP HD) *To capture the Images*	1	100 %	**40,999**

Contingency Budget Detail (Amount in INR) :

Justification	Year-1	Year-2	Year-3	Total
The contingent grant can be utilized for purposes like, but not limited to: • Stationary (Paper, cartridges, Pen drive, CD's, Files) - Item, Qty, cost/piece.	25,000	25,000	25,000	**75,000**

Overhead Budget Detail (Amount in INR) :

Justification	Year-1	Year-2	Year-3	Total
Overhead expense by pointing out the sales increase and suggesting that the company must examine non-overhead costs, such as wages, that are leeching profits.	1,00,000	1,00,000	1,00,000	**3,00,000**

Other Budget Detail (Amount in INR) :

Description/Justification	Year-1	Year-2	Year-3	Total
Overhead Overhead expense by pointing out the sales increase and suggesting that the company must examine non-overhead costs, such as wages, that are leeching profits.	1,00,000	1,00,000	1,00,000	**3,00,000**

PROFORMAFORBIO-DATA

1. Nameandfullcorrespondenceaddress : DrShaikFairooz

2. Email(s)and contactnumber(s): fairoozsk74@gmail.com , 7842288040

3. Institution : Malla Reddy Engineering College ,Secunderabad , Telangana.

4. DateofBirth : 01-04-2974

5. Gender(M/F/T) : M

6. CategoryGen/SC/ST/OBC : Genaral

7. Whetherdifferently disabled(Yes/No) : No

8. AcademicQualification(UndergraduateOnwards)

	Degree	Year	Subject	University/Institution	%ofmarks
1.	B.Tech	2000	ECE	NargarjunaUniversity	85
2.	M.E	2006	Digital Systems	Osmania University	69
3.	Phd	2018	VLSI	JNTUH, Hyderabad	-----
4.					

9. Ph.Dthesistitle,Guide'sName,Institute/Organization/University,YearofAward.

Design of SoC for video coding with an Improved Performance,Dr. B.K.Madhavi **,**Professor in ECE Department, Siddhartha Institute of Engineering and Technology, Vinobha Nagar, Ibrahimpatnam, Hyderabad , 2018.

10. Workexperience(inchronologicalorder).

S.No.	Positionsheld	NameoftheI nstitute	From	To	PayScale
1	Associate Professor	Malla Reddy Engineering College	24-02-2021	Till date	37400-67000-9000
2	Associate Professor	Sreyas Institute of Engineering College	23-11-2018	31-01-2021	37400-67000-9000
3	Associate Professor	MLR Institute of Technology	24-07-2017	24-11-2018	37400-67000-9000
4	Associate Professor	Don Bosco Institute of Technology	14-07-2014	31-03-2017	37400-67000-9000
5	Associate Professor & HOD	ISL Womens Engineering College	14-08-2010	30-06-2014	15600-39100-3300
6	Associate Professor	Aurora's Scientific , Technological and Research Academy	07-07-2007	08-08-2010	15600-39100-3300
7	Associate Professor	CMR College of Engineering & Technology	01-09-2002	05-07-2007	8000-275-13500
8	Assistant Professor	Syed Hashim College of Science & Technology	20-10-2000	31-08-2002	8000-275-13500

11. ProfessionalRecognition/Award/Prize/Certificate,Fellowshipreceivedbytheapplicant.

S.No	NameofAward	AwardingAgency	Year

12. Publications*(ListofpaperspublishedinSCIJournals,inyear wisedescendingorder).*

S.No.	Author(s)	Title	NameofJournal	Volume	Page	Year
1	ShaikFairooz	Exploration on Mechanical Behaviours of Hyacinth Fibre Particles Reinforced Polymer Matrix-Based Hybrid Composites for Electronic Applications	Advances in Materials Science and Engineering	10	1155-1165	2021
2	ShaikFairooz	NMR configurations with novel majority voter circuits to mask multiple module faults	Journal of Ambient Intelligence and Humanized Computing	10	s12652-021-03074-3	2021
3	ShaikFairooz	Voice controlled home automation system by using raspberry pi	***Journal of Advanced Research in Dynamical and Control Systems***	10	1338–1343	2018

13. Detailofpatents.

S.No	PatentTitle	NameofApplicant(s)	PatentNo.	AwardDate	Agency/Country	Status
1	IOT based Crop Monitoring Scheme using Smart Device with Machine Learning Methodology	ShaikFairooz	202141031518	16-07-21	India	Active
2	Smart Renewable Energy Based Shoes to Support Healthy Life	ShaikFairooz	202141014146	16-04-21	India	Active
3	Smart Solar Shoe	ShaikFairooz	341853-001	26-03-21	India	Active
4	Renewable Energy Based Shoes for Supporting a Healthy Lifestyle	ShaikFairooz	AU 2021101865	19-05-21	International	Active

14. Books/Reports/Chapters/Generalarticlesetc.

S.No	Title	Author'sName	Publisher	YearofPublication
1	Design of CMOS Circuits Cognitive Radio Application with Power Analysis	ShaikFairooz	CRC Press,Taylor& Francis Group	2021
2	A Novel Design of 16 bit MAC Unit on Vedic Mathematics using FPGA hardware for Cognitive Radio Application	ShaikFairooz	CRC Press,Taylor& Francis Group	2021

15. Any other Information(maximum(500words)

Dr. SK.Fairooz is an Associate Professor in Electronics and Communication Department in Malla Reddy Engineering College , Hyderabad . He is having total Experience of 21.5 Yrs. He is completed PhD from JNTU Hyderabad in the research field VLSI in the year 2018. He was post graduated from Osmania University, Hyderabad in the year 2006 with the specialization Digital Systems and Secured Top rank from OU. He was graduated from VJREC, Vijayawada in the year 2000. His expertise in subjects like Network Analysis, Control Systems. He uses active and collaborative learning techniques, engage students in experiences, emphasize higher-order cognitive activities in the classroom, interact with students, challenge students academically, and value enriching educational experiences. He is one of the editorial member for annual department magazine ELECTRONICA FORUM 2014, 2015 and also an coordinator of International Conference ICrtSIV 2015. He presented and published several papers in International Journals / Conference Papers.

PROFORMA FOR BIO-DATA (to be uploaded)

1. Name and full correspondence address : Dr A. Pradeep Kumar

2. Email(s) and contact number(s): pradeepsujeeth@gmail.com, 7731036533

3. Institution : Malla Reddy Engineering College , Secunderabad , Telangana.

4. Date of Birth : 03-06-1982

5. Gender (M/F/T) : M

6. Category Gen/SC/ST/OBC : Genaral

7. Whether differently disabled (Yes/No) : No

8. Academic Qualification (Undergraduate Onwards)

	Degree	Year	Subject	University/Institution	% of marks
1.	B.Tech	2005	ECE	JNTUH, Hyderabad	64
2.	M.Tech	2010	VLSI System Design	JNTUH, Hyderabad	68
3.	Ph.d	2018	VLSI	JNTUH, Hyderabad	-----
4.					

9. Ph.D thesis title, Guide's Name, Institute/Organization/University, Year of Award.

Design of Optimized Memory in Neuromorphic VLSI Chips, Dr. Yash pal Singh, Om Prakash Joginder Singh (OPJS) University, 2018

10. Work experience (in chronological order).

S.No.	Positions held	Name of the Institute	From	To	Pay Scale
1	Associate Professor	Malla Reddy Engineering College	June 2014	Till Date	
2	Assistant Professor	Vignana Bharathi Institute of Technology	Oct 2008	Aril 2014	
3	Assistant Professor	Anwar Ul Uloom College of Engineering & Technology	Feb 2006	July 2007	

11. Professional Recognition/ Award/ Prize/ Certificate, Fellowship received by the applicant.

S.No	Name of Award	Awarding Agency	Year
1	Global Eminent Teacher Award	VIJ Trust, Thiruninravur, Thiruvallur, Chennai	2021

12. Publications *(List of papers published in SCI Journals, in year wise descending order).*

S.No.	Author(s)	Title	Name of Journal	Volume	Page	Year
1	Dr. A. Pradeep kumar, Y. Devendar Reddy, Dr. T. Srinivas Reddy and K. Jamal	An Efficient Interconnection System for Neural NOC Using Fault Tolerant Routing Method	Journal of Physics: Conference Series	2089	1-7	2021
2	Dr.A. Pradeep kumar, K. Anil Kumar	An Advanced Design of Pseudo Rand om Discrete Time Even System for Fault Detection	International Journal of Advanced Science and Technology (IJAST)	28	91-98	2019
3	Dr.A. Pradeep kumar	Ultrasonic flaw signal Classification based on Curvelet transform and Support Vector Machine	International Journal of Innovative Technology and Exploring Engineering (IJITEE)	8	449-453	2018

13. Detail of patents.

S.No	Patent Title	Name of Applicant(s)	Patent No.	Award Date	Agency/Country	Status
1	A Novel Method For Empowering Edge Computing For Source Allocation Based Learning For Industrial IOT	A. Pradeep Kumar	AU 2021101292 A4	06-05-2021	Australian Patent Office	Published
2	An Automated IOT Based Blood Glucose Measurement Device Along With LED	A. Pradeep Kumar	202041002455 A	07-02-2020	IP INDIA	Published
3	An Employee Management System	A. Pradeep Kumar	201841044752 A	07-12-2018	IP INDIA	Published

14. Books/Reports/Chapters/General articles etc.

S.No	Title	Author's Name	Publisher	Year of Publication
1	Implementation of Multifunction Residue Architectures on FPGA for Cryptography Applications: A Recent Study	Dr. A. Pradeep Kumar, V. Srinivas	B.P International	2021
2	Electrical Circuit Analysis-I	A. Pradeep Kumar, T.Srinivas Reddy	Spectrum Techno Press	2017

15. Any other Information (maximum 500 words)

Endorsement from the Head of the Institution of PI

This is to certify that:

1. Institute welcomes participation of Name : **Dr. Shaik Fairooz** , Designation : **Associate Professor** as the Principal Investigator and **Dr. A. Pradeep Kumar** as the Co- Investigator/s for the project titled "**Design and Implementation of software defined network on chip scheduler design for Quality oriented multimedia interface**" and that in the unforeseen event of discontinuance by the Principal Investigator, the Co-Investigator will assume the responsibility of the fruitful completion of the project with the approval of SERB.

2. The PI, **Dr.Shaik Fairooz** is a permanent or regular employee of this Institute/University/Organization and has **12** years of regular service left before superannuation

3. The project starts from the date on which the University/Institute/ Organization/College receives the grant from SCIENCE & ENGINEERING RESEARCH BOARD (SERB), New Delhi.

4. The investigator will be governed by the rules and regulations of University/ Institute/Organization/College and will be under administrative control of the University/ Institute/Organization/College for the duration of the project.

5. The grant-in-aid by the SCIENCE & ENGINEERING RESEARCH BOARD (SERB), New Delhi will be used to meet the expenditure on the project and for the period for which the project has been sanctioned as mentioned in the sanction order.

6. No administrative or other liability will be attached to SCIENCE & ENGINEERING RESEARCH BOARD (SERB), New Delhi at the end of the project.

7. The University/Institute/Organization/College will provide basic infrastructure and other required facilities to the investigator for undertaking the research project.

8. The University/ Institute/Organization/College will take into its books all assets created in the above project and its disposal would be at the discretion of SCIENCE & ENGINEERING RESEARCH BOARD (SERB), New Delhi.

9. The University/ Institute/Organization/College assumes to undertake the financial and other management responsibilities of the project.

Seal of

University/ Institute/Organization/College

Date:

Signature

Registrar of University/Head of the Institute/
Head of organization / Principal of College

Principal
Malla Reddy Engineering College
Maisammaguda, Dhulapally,
(Post Via Kompally), Sec'bad-500100.

Endorsement from the Head of the Institution of Co-PI

This is to certify that:

1. Institute welcomes participation of Name : **Dr. Shaik Fairooz** Designation **Associate Professor** as the Principal Investigator and **Dr.A.Pradeep Kumar** as the Co- Investigator for the project titled "**Design and Implementation of software defined network on chip scheduler design for Quality oriented multimedia interface**" and that in the unforeseen event of discontinuance by the Principal Investigator, the Co-Investigator will assume the responsibility of the fruitful completion of the project with the approval of SERB.

2. The Co-PI, **Dr.A.Pradeep Kumar** is a permanent or regular employee of this Institute/University/Organization and has **21** years of regular service left before superannuation

3. The Co-PI will be governed by the rules and regulations of University/ Institute/Organization/College and will be under administrative control of the University/ Institute/Organization/College for the duration of the project.

4. The grant-in-aid by the SCIENCE & ENGINEERING RESEARCH BOARD (SERB), New Delhi will be used to meet the expenditure on the project and for the period for which the project has been sanctioned as mentioned in the sanction order.

5. No administrative or other liability will be attached to SCIENCE & ENGINEERING RESEARCH BOARD (SERB), New Delhi at the end of the project.

6. The University/Institute/Organization/College will provide basic infrastructure and other required facilities to the investigator for undertaking the research project.

7. The University/ Institute/Organization/College will take into its books all assets created in the above project and its disposal would be at the discretion of SCIENCE & ENGINEERING RESEARCH BOARD (SERB), New Delhi.

8. The University/ Institute/Organization/College assumes to undertake the financial and other management responsibilities of the project.

Seal of

University/ Institute/Organization/College

Malla Reddy Engg. College 500 100 Hyderabad

Date:

Signature

Registrar of University/Head of the Institute/
Head of organization / Principal of College

Principal
Malla Reddy Engineering College
Maisammaguda, Dhulapally,
(Post Via Kompally), Sec'bad-500100.

Undertaking by the Principal Investigator

To

The Secretary
SERB, New Delhi

Sir

I Dr SK. FAIROZ

herby certify that the research proposal titled Software Defined Network on chip simulator design for Quality of Service in multimedia communication submitted for possible funding by SERB, New Delhi is my original idea and has not been copied/taken verbatim from anyone or from any other sources. I further certify that this proposal has been checked for plagiarism through a plagiarism detection tool i.e. turnitin approved by the Institute and the contents are original and not copied/taken from any one or many other sources. I am aware of the UGCs Regulations on prevention of Plagiarism i.e. University Grant Commission (Promotion of Academic Integrity and Prevention of Plagiarism in Higher Educational Institutions) Regulation, 2018. I also declare that there are no plagiarism charges established or pending against me in the last five years. If the funding agency notices any plagiarism or any other discrepancies in the above proposal of mine, I would abide by whatsoever action taken against me by SERB, as deemed necessary.

29/4/22

Signature of PI with date

Name / designation

Dr. SK. FAIROZ
Associate Professor
MREC
Secunderabad,
Telangana

Certificate from the Investigator

Project Title: Software defined network on chip scheduler design for quality of service in multimedia communication,

It is certified that

1. The same project proposal has not been submitted elsewhere for financial support.
2. We/I undertake that spare time on equipment procured in the project will be made available to other users.
3. We/I agree to submit a certificate from Institutional Biosafety Committee, if the project involves the utilization of genetically engineered organisms. We/I also declare that while conducting experiments, the Biosafety Guidelines of Department of Biotechnology, Department of Health Research, GOI would be followed in toto.
4. We/I agree to submit ethical clearance certificate from the concerned ethical committee, if the project involves field trails/experiments/exchange of specimens, human & animal materials etc.
5. The research work proposed in the scheme/project does not in any way duplicate the work already done or being carried out elsewhere on the subject.
6. We/I agree to abide by the terms and conditions of SERB grant.

Name and signature of Principal Investigator: Dr SK. FAIROOZ, [signature]

Date: 28/04/2022

Place: Secunderabad.

Name and signature of Co-PI (s) (if any): Dr. A. Pradeepkumar, [signature]

Date: 28/04/2022

Place: Secunderabad