MALLA REDDY ENGINEERING COLLEGE

(AUTONOMOUS)

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

LAB MANUAL

Linear and Digital IC Applications Lab

III B.Tech I Semester

Prepared By **Verified By** **Approved By**

IMPORTANCE OF LINEAR AND DIGITAL IC APPLICATIONS LAB

The term IC means Integrated circuit where all the active and passive components are fabricated on the same chip. IC technology has many advantages like small size, Low cost , Less weight , High speed etc. Based on the Applications IC's are divided into Digital IC's and Analog IC's. Various Technologies are used to fabricate the IC's. They are Monolithic Technology, Thick and Thin film Technology and Hybrid Technology**.** Based on the Chip size and circuit Complexity IC's are classified as SSI, MSI, LSI,VLSI, ULSI etc.

In this lab, the first cycle deals with Analog IC's where as second Cycle deals with Digital IC's. In Analog IC's most of the experiments is with µA741 Operational Amplifier. First four Experiments will cover both open and closed loop applications of IC µA741. Timer applications will be covered with the help of IC 555.

The Second Cycle Covered all the concepts learned in Switching Theory and Logic Design and IC Applications Theory with the help of Digital IC's. Different Digital IC's are introduced by which the student can become familiar with designing of Digital circuits in practical way.

2014-2015 **Code: 40416**

MALLA REDDY ENGINEERING COLLEGE
(AUTONOMOUS)

III Year B.Tech. ECE-I Sem

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Linear and Digital IC Applications Lab

MINIMUM TWELVE EXPERIMENTS MUST CONDUCT: (Six from each part A & B)
PART -A: TO VERIFY THE FOLLOWING FUNCTIONS

1. Adder, Subtractor, Comparator Circuits using IC 741 OP AMP .
2. Integrator and Differentiator Circuits using IC 741 OP AMP.
3. Active Low pass, High pass Butterworth (Second Order).
4. RC Phase Shift and Wien Bridge Oscillators using IC 741 Op-Amp.
5. IC 555 Timers – Monostable Operation Circuits.
6. Schmitt Trigger Circuits – using IC 741 and IC 555.
7. IC 565 –PLL applications
8. Voltage Regulator using IC 723,Three terminal voltage regulators 7805,7809, 7912
9. Sample and Hold LF398 IC

PART -B: TO VERIFY THE FOLLOWING FUNCTIONALITY Of the following 74 series TTL ICS

1. D-Flip Flop (74LS74) and JK Master Slave Flip-flop(74LS73)
2. Decade counter (74LS90) and Up-down Counter (74LS192)
3. Universal shift Register(74LS194/195)
4. 3-8 Decoder using (74LS138).
5. 4 – bit comparator (74LS85)
6. 8x1 Multiplexer - 74LS151 and 2x4 DeMultiplexer-74155.
7. RAM 16X4 -74189(read and write operation)
8. Stack and queue implementation using RAM, 74189.

Equipment required for Laboratories:

1. RPS
2. CRO
3. Function Generator
4. Multi Meters
5. Bread Boards
6. Components:- IC741, IC555, IC566, IC1496, IC723, 7805, 7809, 7912 and other essential components.
7. Analog IC Tester

LIST OF EXPERIMENTS

PART-A

1. **Adder, Subtractor, Comparator Circuits using IC741 OP-AMP.**
2. **Integrator and Differentiator Circuits using IC 741 OP-AMP.**
3. **Active Filter Applications – LPF, HPF Butterworth (Second Order).**
4. **RC Phase Shift and Wien Bridge Oscillators using IC 741 Op-Amp.**
5. **IC 555 Timers – Monostable Operation Circuits.**
6. **Schmitt Trigger Circuits – using IC 741 and IC 555.**
7. **IC 565 – PLL applications.**
8. **Voltage Regulator using IC 723,Three terminal voltage regulators 7805,7809,7912.**
9. **Sample and Hold LF398 IC.**

PART-B

1. **D-Flip Flop (74LS74) and JK Master Slave Flip-flop(74LS73) .**
2. **Decade counter (74LS90) and Up-down Counter (74LS192).**
3. **Universal shift Register(74LS194).**
4. **3-8 Decoder using (74LS138).**
5. **4 – bit comparator (74LS85).**
6. **8x1 Multiplexer - 74LS151 and 2x1 Multiplexer-74LS155.**
7. **RAM 16X4 – 74189(read and write operations).**
8. **Stack and queue implementation using RAM, 74189.**

PART-A

1. Adder, Subtractor, Comparator Circuits using IC741 OP-AMP

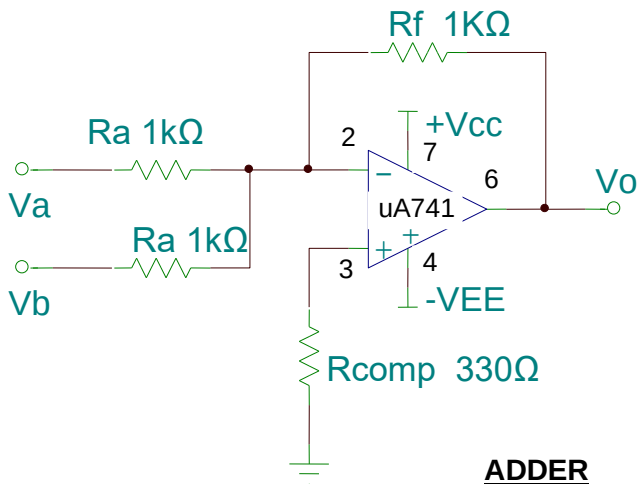
(a) Adder

AIM : To design and adder circuit using an Op – Amp and Obtain the Output for various Inputs

APPARATUS:

Dual Regulated power supply	-1 no's
Multimeter	- 1 no's
IC 741	- 1 no's
Resistor 1K	- 3 no's
330Ω	- 1 no's

CIRCUIT DIAGRAM:



ADDER

THEORY:

As the input impedance of an op-amp is extremely large, more than one input signal can be applied to the inverting amplifier. Such circuit gives the addition of the applied signals at the output. Hence it is called summer or adder circuit.

In this circuit, all the input signals to be added are applied to the Inverting input terminal(or Non inverting input)of the op-amp. The circuit with the two input signals at Inverting input is shown in figure.

Assume $R_i=\infty$, $A=\infty$ and No input offset voltage

As $R_i=\infty$, $I_{B1} = I_{B2} = 0$.

As Non-Inverting is grounded, due to virtual ground concept the node V_2 is also at virtual ground potential.

$Vo = A(V_1 - V_2)$; $V_1 - V_2 = Vo/A = 0$

as $V_2 = 0$ $V1 \approx 0$

$$V_0 = V_a + V_b + V_c$$

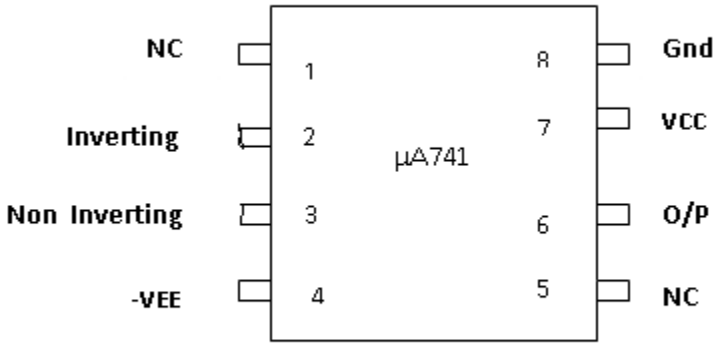
$$= -\frac{R_F}{R_A} V_a - \frac{R_F}{R_B} V_b$$

$$= -R_F \left[\frac{V_a}{R_a} + \frac{V_b}{R_b} \right]$$

If $R_F = R_a = R_b$

$V_0 = -(V_a + V_b + V_c)$.

PIN DIAGRAM :



PROCEDURE:

1. Connected the circuit as shown in the diagram.
2. Switched ON the DC supply and adjusted +Vcc=12V and $-V_{EE} = 12V$
3. For various values of V_a, V_b checked the o/p V_0 and verified whether it is sum of V_a, V_b with a –ve sine or not.

RESULT:

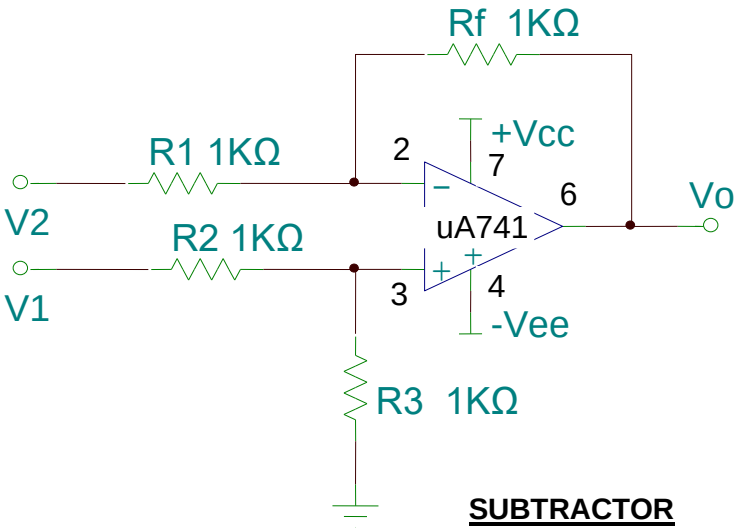
V_a	V_b	$V_{o(theoretical)}$	$V_{o(practical)}$

(b) Subtractor

AIM : To design and subtractor circuit using IC 741 and verify the outputs for Different inputs.

APPARATUS: Dual Regulated power supply - 1 no's
Multimeter - 1 no's
IC 741 - 1 no's
Resistor – 1K - 4 no's

CIRCUIT DIAGRAM :



SUBTRACTOR

THEORY :

The Circuit which will Subtract the Two inputs Voltages is called subtractor or difference Amplifier Circuit. In order to find the Relationship between Input and output we need to apply superposition theorem.

By making $V_2 = 0$, The Circuit will become No inverting Amplifier So

$$V_{01} = \left[1 + \frac{Rf}{R1}\right] \left[\frac{Rf}{R2+Rf}\right] V_2.$$

Similarly by making V1 =0 , The Circuit will become Inverting Amplifier.

$$V_{02} = -(Rf / R1)\, V_1.$$

As $V_o = V_{o1} + V_{o2}$

The total Output of the Difference Amplifier is

$$V_o = \frac{Rf}{R1}(V_1 - V_2)$$

$R_1 = R_2 = R_3 = R_F = R$,

Then **$V_O = V_1 – V_2$.**

PROCEDURE:

4. Connected the circuit as shown in the diagram
5. Switched ON the DC supply and adjusted +Vcc=15V and $– V_{EE} = 15V$
6. For various values of V_1, V_2, and checked V_0 and verified whether V_0 is, $(V_1 - V_2)$ or not.

RESULT:

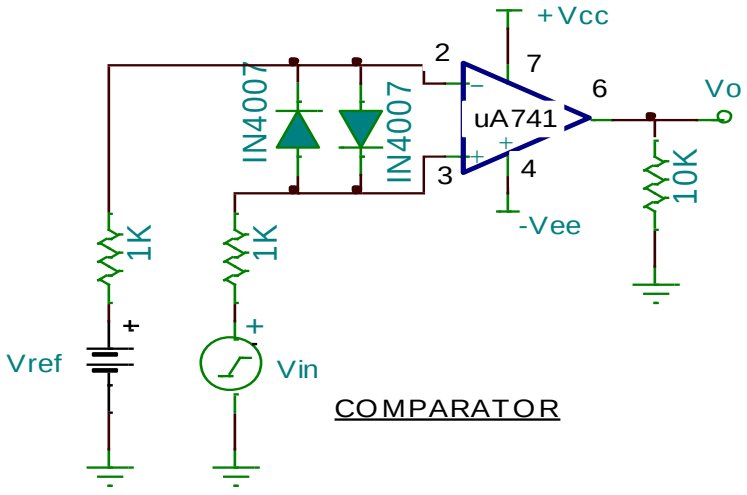
V_1	V_2	$V_{o(theoretical)}$	$V_{O(practical)}$

(C) Comparator

AIM : To sketch the o/p wave form and study the working of non – inverting comparator for positive and negative reference voltage.

APPARATUS: DC power supply - 1 no's
Function generator - 1 no's
CRO - 1 no's
Resistor – 1K - 2 no'
– 10K - 1 no's
Diodes – IN4007 - 2 no's

CIRCUIT DIAGRAM:



THEORY:

A comparator as its name implies, compare a signal voltage on one i/p of a op-amp with a known voltage called the Reference voltage on the other I/P In the comparator circuit, if fixed reference voltage is applied to the Inverting input and signal voltage Vin is applied to the Non Inverting input, then the arrangement is called non – inverting comparator. When $V_{in}<V_{ref,}$ the o/p voltage V_0 is at – Vsat ($\approx -V_{EE}$) because the voltage at (-) I/p is higher than that at the (+) I/p. When

$V_{in}>V_{ref,}$ the (+) i/p voltage becomes positive with respect to the (-) input and V_0 goes to + V_{sat} ($\approx +Vcc$) Thus V_0 changes from one saturation level to another.

PROCEDURE:

1. Made the connections as shown in the circuit diagram.
2. +Vcc = 12V, $-V_{EE}$ =12V are set by adjusting the dc supply.
3. Set V_{in} = 5V, 1Khz from the function generator and V_{ref} = 3V from the DC power supply.
4. Observed the Output waveform on CRO
5. Sketched the o/p wave forms for Vref = -3 Volt, 3Volt , 0 Volt

EXPECTED OUTPUT WAVEFORMS:

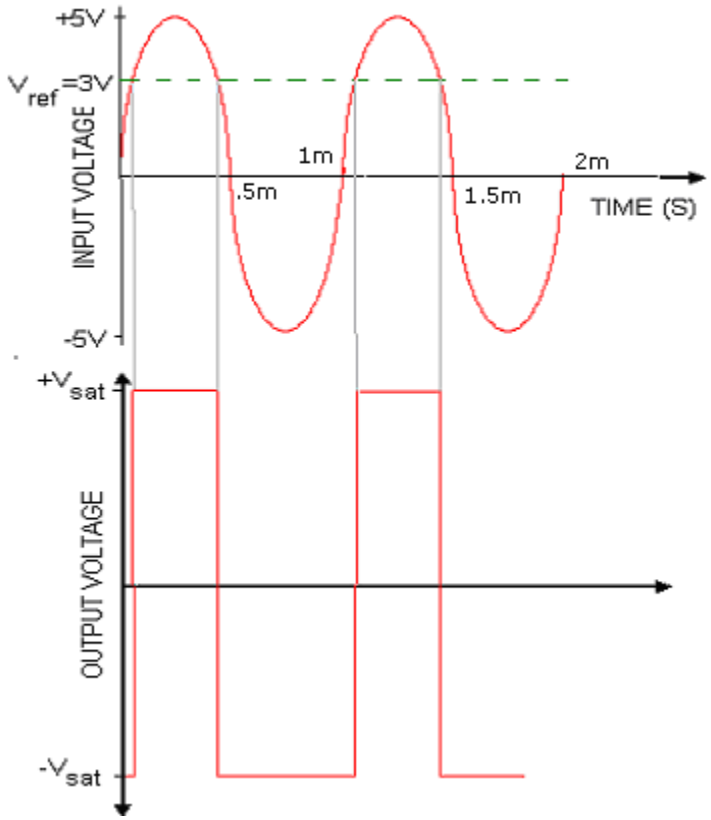


Fig. (a) When V_{ref} = 3V

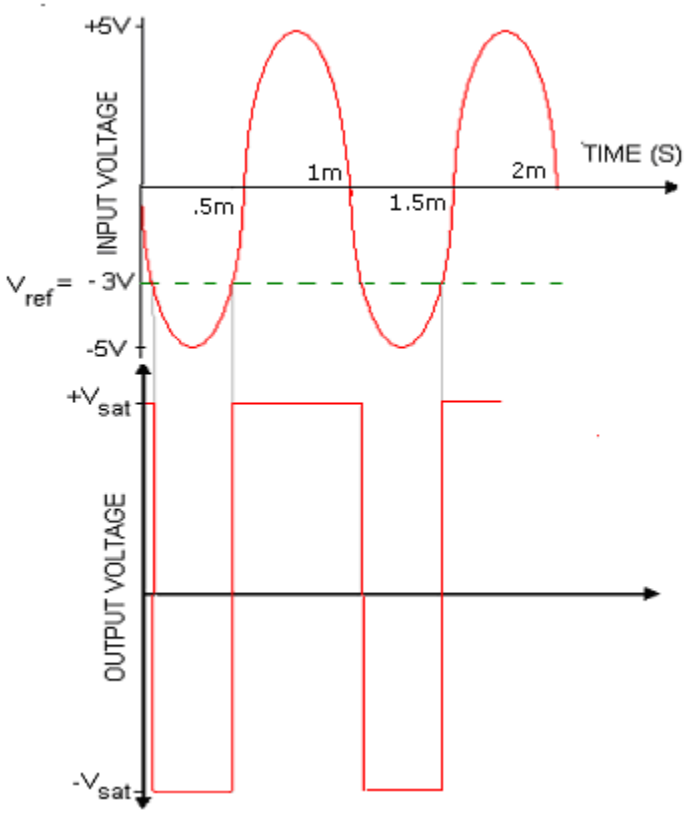


Fig. (b) When V_{ref} = - 3V

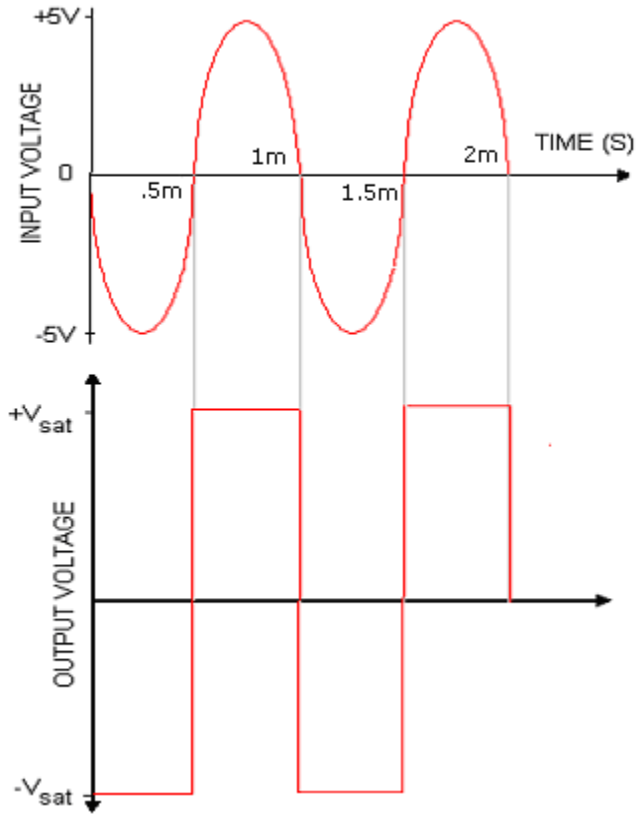


Fig. (c) When V_{ref} = 0V

RESULT: Input and Output waveforms of Comparator is Observed.

Viva Voice ;

1. Draw the Circuit Diagram of Non Inverting Comparator.
2. What is the Significance of Pin no 1 and 5.
3. Pin Configuration of any other Op amp.

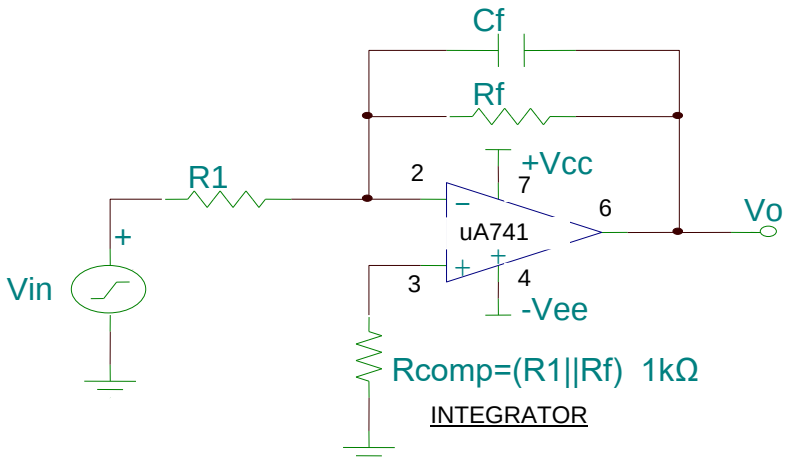
2. Integrator and Differentiator Circuits using IC 741 OP-AMP

(a)Integrator

AIM : To design and study the operation of an Integrator using IC741.

APPARATUS: IC741, Resistors - 10kΩ , 1KΩ , 100Ω (1 no each)
Capacitors - 0.1μF, 0.01μF (1 no each).

CIRCUIT:



THEORY :

The circuit witch gives the output voltage as the Integration of the Input Voltage is called Integrator. The fig Shown above is Practical Integrator. In Ideal Integrator we have two Disadvantages. First is In the Absence of Signal also the output is likely to be Offset towards the Positive and Negative saturation levels. And second problem is Ideal integrator is having very small Bandwidth. So it can be used for very small Frequency range of the input only. To avoid the above problems we will prefer Practical Integrator.

DESIGN PROCEDUE:

Gain limiting frequency $f_a = \frac{1}{2\pi R_F C_F}$

Frequency at which gain is zero $f_b = \frac{1}{2\pi R_1 C_F}$

Use $C_f = 0.001\mu F$ and $R_1 = 100\Omega$.

PROCEDURE:

1. Connected the circuit as per the circuit diagram.
2. The circuit functions as an integrator when $R_1C_f >> T$ **i.e.,**

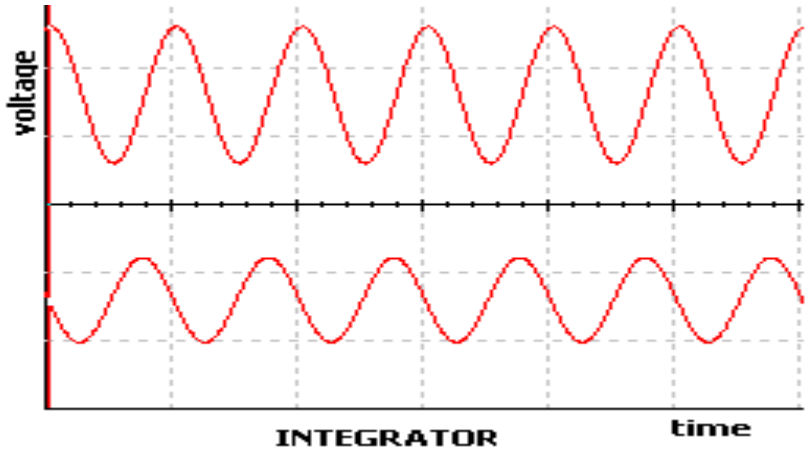
   Say $R_1C_f = 10T$. Let $R_f = 10k\Omega$, $R1 = 1K\Omega$, $Cf = 0.1\mu F$.

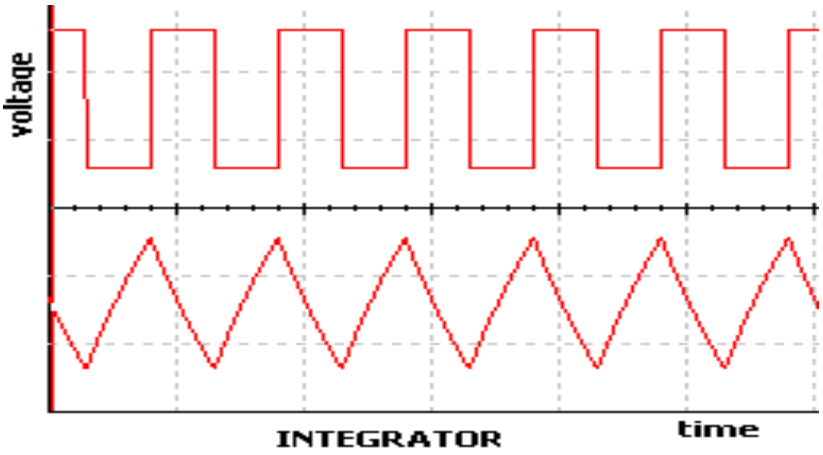
   Therefore, $T = \frac{1000 * 0.1 * 10^{-6}}{10}$ = 0.01ms.

   Where T = time period of input signal.

   Applied a square wave signal frequency f= 1/T i.e., 100 KHz and observed output waveform which is a triangular one. Made a note of input and output waveforms.
3. Applied a sinusoidal signal of frequency 100Hz and amplitude $V_{IN} = 0.1V$ and noted down the output voltage V_o. Calculated the voltage gain $A_v = V_0/V_i$ and A_v in dB = 20 log10 Vo/Vi.
4. Repeated the above step by keeping V_i constant and vary the frequency in steps up to 1MHz.
5. Plotted the frequency response graph and calculated f_a and f_b from the graph.

EXPECTED WAVEFORMS :





RESULT :

Theoretical fa	Practical fa	Theoretical fb	Practical fb

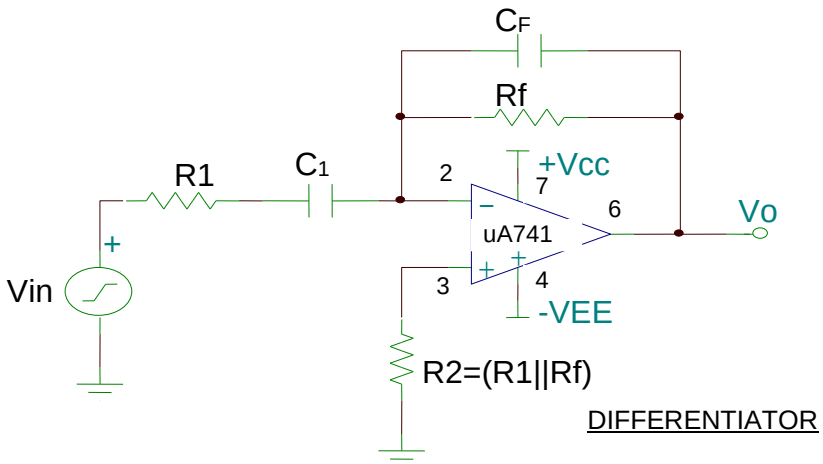
(b) Differentiator

AIM : To design and study the operation of a Differentiator using IC 741

APPARATUS:

Resistors (2Nos) -100 Ω
(1 No's) - 1K Ω
Capacitor - 0.1 µf,
0.01 µf - 1 each..
Op Amp 741 - 1No.
Function Generator, Dual Regulated Power Supply, CRO.

CIRCUIT :



DIFFERENTIATOR

THEORY:

The circuit which produces the differentiation of the input voltage at its output is called Differentiator. The Differentiator which uses active devices along with Passive elements for Differentiation is called Active differentiator. The circuit shown above is a Practical Differentiator.

Frequency at which gain is zero (0 dB) $f_a = \frac{1}{2\pi R_F C_1}$

Gain limiting frequency $f_b = \frac{1}{2\pi R_1 C_1}$

Use $C_f = 0.01\mu F$, $C_1 = 0.1\mu F$, $R_F = 1\ k\Omega$ and $R_1 = 100\Omega$.

PROCEDURE:

1. Connected the circuit as per the circuit diagram.

2. The circuit functions as differentiator when $R_F C_1 << T$ i.e.,

   Say $R_F C_1 = \frac{T}{10}$

   $T = 10\ R_F\ C_1 = 10 * 1 * 10^3 * 0.1 * 10^{-6} = 1ms.$

   Where T = time period of input signal.

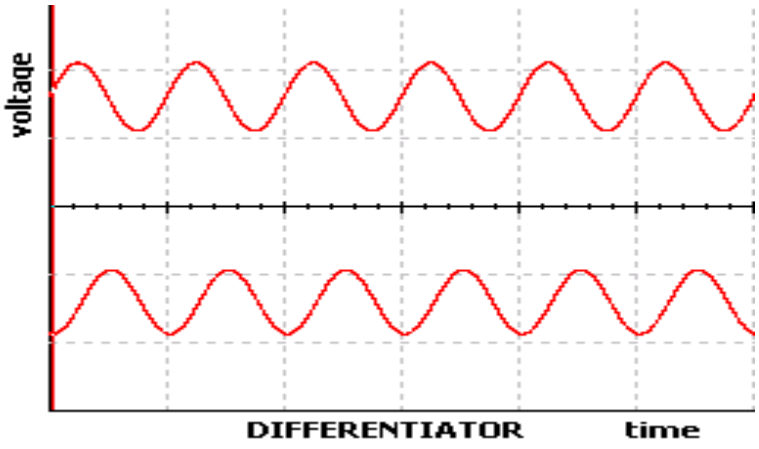
   Applied a square wave signal frequency f= 1/T i.e., 1 KHz and observed output waveform containing Positive and Negative Spikes. Make note of input and output waveforms.

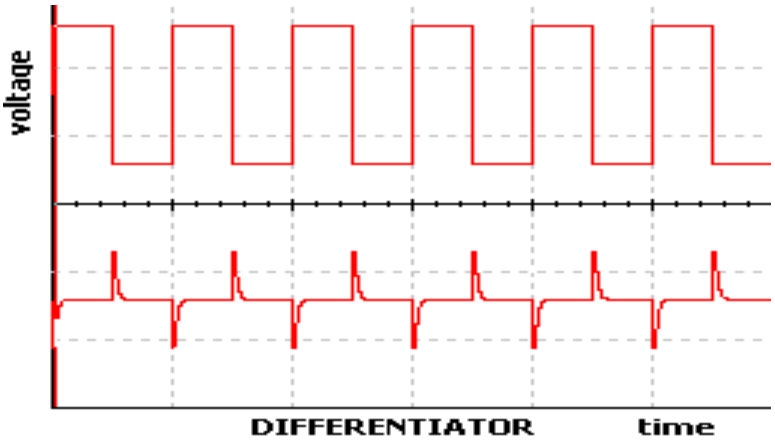
3. Applied a sinusoidal signal of frequency 100Hz and amplitude V_{IN} = 0.1V and noted down the output voltage V_o. Calculated the voltage gain $A_v = V_0/V_i$ and A_v in dB = 20 log10 Vo/Vi.

4. Repeated the above step by keeping V_i constant and varied the frequency in appropriate steps up to 1MHz.

5. Plotted the frequency response graph and calculated f_a and f_b from the graph.

EXPECTED WAVEFORMS:





RESULT :

Theoretical fa	Practical fa	Theoretical fb	Practical fb

Viva Voice:

1. Design the Passive Integrator and Differentiator Circuit for 1K ohms?

2. What are the Disadvantages of Ideal Differentiator Circuit?

3. What are the Disadvantages of Ideal Integrator Circuit?

4. What is advantage of Active Differentiator compared with Passive Differentiator?

3. Active filter applications - LPF, HPF Buuterworth (second order)

(a) SECOND ORDER LOW PASS BUTTERWORTH FILTER

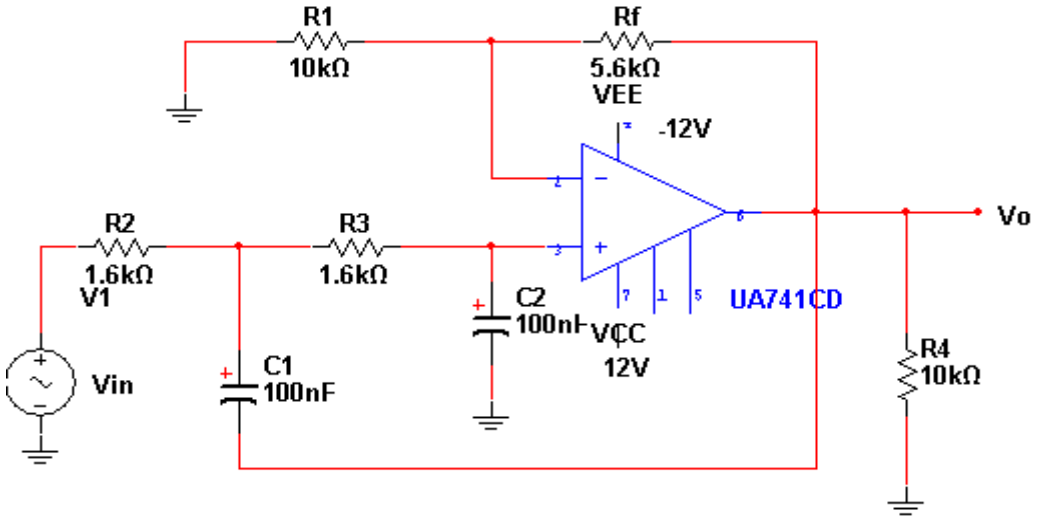
AIM : Design a Low Pass Filter ($2^{nd\ order}$) at a Cutoff frequency of 1 KHz with a Pass Band Gain of 1.586.

APPARATUS:

IC 741	-- 1 No.
Resistor 10KΩ	--- 2 No.
1.6KΩ	--- 2No
5.86KΩ	--- 1No
Capacitor 0.1 μF	--- 2No.

Function Generator, CRO, Dual Regulated Power Supply.

CIRCUIT DIAGRAM:



Second order Low pass Filter

THEORY :

In case of Low Pass Filter, it is always desirable that the gain rolls off very fast after the cut-off frequency i.e. in the Stop Band. In case of first order filter, it rolls off at a rate of 20 dB /decade. In case of second order filter, the gain rolls off at a rate of 40 dB/ decade. Thus,

the slope of the frequency response after f = f_H is -40dB/ decade, for a second order low pass filter.

A first order filter can be converted to second order type by using an additional RC network as Shown in the fig. The cut-off frequency f_H for the filter is decided by R_2, C_1, R_3, and C_2. The gain of the filter is as usual decided by op-amp i.e. the resistance R_1 and R_f.

Higher Cut off Frequency $f_H = \frac{1}{2\pi\sqrt{R2\ R3\ C1\ C2}}$

Gain of the Second Order Filter $A = |V_0/V_{in}| = \frac{Af}{\sqrt{1+(f/fH)4}}$

Where AF = Pass band gain of the Filter $(1 + R_F/R_{1)}$

f = frequency of the Input Signal

f_H = Higher Cut off frequency

DESIGN PROCEDURE: Given f_H = 1 KHz

Choose the value of 'C 'less than or equal to 1 μf ; let c = 0.1 μf

Then calculate R using the $f_H = \frac{1}{2\pi\sqrt{R2\ R3\ C1\ C2}}$

$R_2 = R_3 = R$

$C_1 = C_2 = C$

So $f_H = 1/2\pi RC$

1 K = 1/ 2 π . R. 0.1 μf

$R_2 = R_3 = R = 1.6$ K .

As A_F = Pass band gain of Second order Butter worth Filter = 1+(Rf / R1) = 1.586

For Second Order LPF $R_F = 0.586$ R1

Let R1 = 10 kΩ, R_F = 5.86 KΩ.

PROCEDURE :

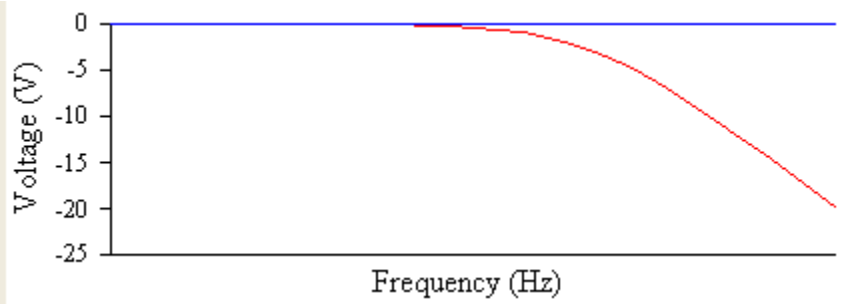
1. Made connections as per the Circuit diagram.
2. Set Vin = 1V varied frequency from 5 Hz to 1 MHz and noted down the Amplitude of output wave form (Vo).
3. Calculated Gain and Gain in db.

4. Ploted the frequency response curve and determined FH.Also marked the pass band and stop band.

TABULAR COLUMN:

Input Frequency(f) in Hz	**Vo(V)**	**Gain** $(\frac{Vo}{Vin})$	**Gain in db** $20\log_{10}(\frac{Vo}{Vin})$

EXPECTED GRAPH:



RESULT:

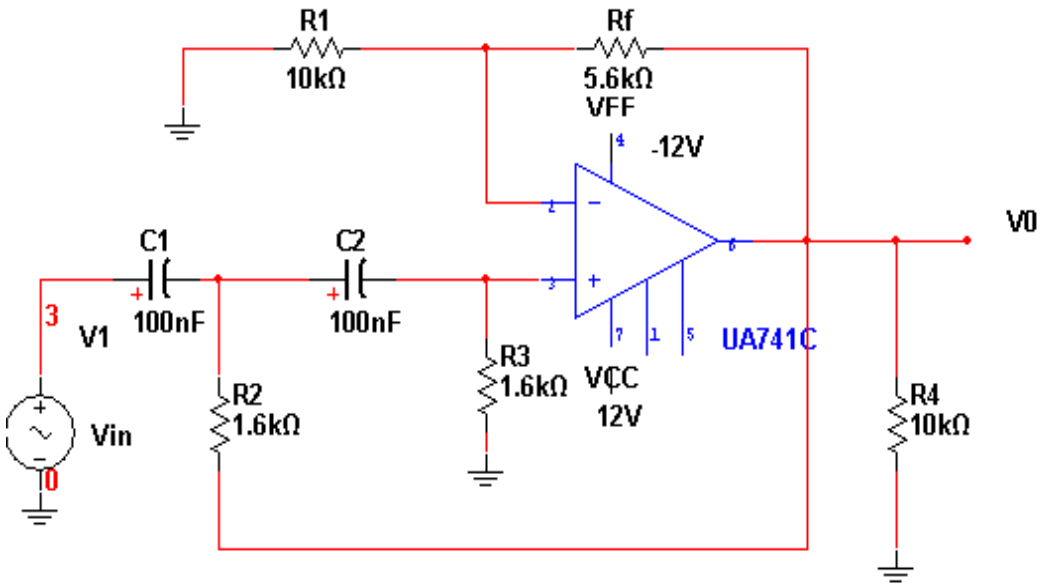
	THEORITICAL	PRACTICAL
f_L		
A		

(b) SECOND ORDER HIGH PASS BUTTER WORTH FILTER

AIM : Design High Pass Filter (2nd order) at a cut of frequency of 1 KHz with pass Band Gain of 1.586

APPARATUS: IC 741 -- 1 No.
Resistor 10KΩ --- 2 No.
1.6KΩ --- 2No
5.86KΩ --- 1No
Capacitor0.1 μF --- 2No.
Function Generator, CRO, Dual Regulated Power Supply.

CIRCUIT DIAGRAM:



Second Order High Pass Filter

THEORY : In case of High Pass Filter, it is always desirable that the gain rolls off very fast before the cut-off frequency i.e. In the Stop Band. In case of first order filter, it rolls off at a rate of 20 dB /decade. In case of second order filter, the gain rolls off at a rate of 40 dB/ decade. Thus, the slope of the frequency response before f = f_L is +40dB/ decade, for a second order high pass filter.

A Second order Low pass filter can be converted to second order High pass Filter type by interchanging the positions of Capacitors and Resistors as given in fig. The cut-off

frequency f_L for the filter is decided by R_2, C1, R_3, and C_2. The gain of the filter is as usual decided by op-amp i.e. the resistance R_1 and R_f

Lower Cut off Frequency $f_L = \frac{1}{2\pi\sqrt{R2\ R3\ C1\ C2}}$

Gain of the Second Order Filter A $= |V_0/V_{in}| = \frac{Af}{\sqrt{1+(fL/f)4}}$

Where A_F = Pass band gain of the Filter $(1 + R_F/R_{1)}$

f = frequency of the Input Signal

f_H = Higher Cut off frequency.

DESIGN PROCEDURE:

Given f_L = 1 KHz

Choose the value of C less than or equal to 1 μf ; let c = 0.1 μf

Then calculate R using the $f_L = 1/2\pi\sqrt{R_2 R_3 C_2 C_3}$

$R_2 = R_3 = R$

$C_1 = C2 = C$

So $f_L = 1/2\pi RC$

$1\ K = 1/2\pi . R. 0.1\ \mu f$

$R_2 = R_3 = R = 1.6$ K.

For Second Order HPF Rf= 0.586 R1

Let R_1 = 10 kΩ, R_F = 5.86 KΩ.

Frequency Response

$$|V_0/V_{in}| = \frac{Af}{\sqrt{1+(fl/f)4}}$$

Where A_F = Pass band gain of Second order Butter worth Filter = $1 + (R_f/R_1) = 1.586$

f = frequency of the Input Signal

f_L = Lower Cut off frequency.

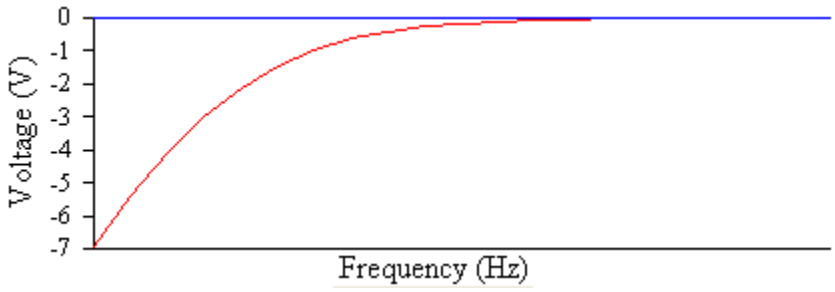
PROCEDURE:

1. Made Connections as per the Circuit diagram.
2. Set Vin = 1V varied frequency from 5Hz to 1 MHz and noted down the Amplitude of output wave form (Vo).
3. Calculated gain, gain in db.
4. Plotted the frequency response curve and determined FL.Also marked the pass band and stop band.

TABULAR COLUMN:

Input Frequency(f) in Hz	**Vo(V)**	**Gain** $(\frac{Vo}{Vin})$	**Gain in db** $20\log_{10}(\frac{Vo}{Vin})$

EXPECTED GRAPH:



RESULT:

	THEORITICAL	PRACTICAL
fL		
A		

Viva Voice : 1. Draw the Circuit of Third Order Low Pass Filter.

2. Draw the Frequency Response of Band Pass Filter.

3. Draw the Ideal Frequency Response of All types of Filers.

4. RC Phase Shift and Wien Bridge Oscillators using IC 741 Op-Amp

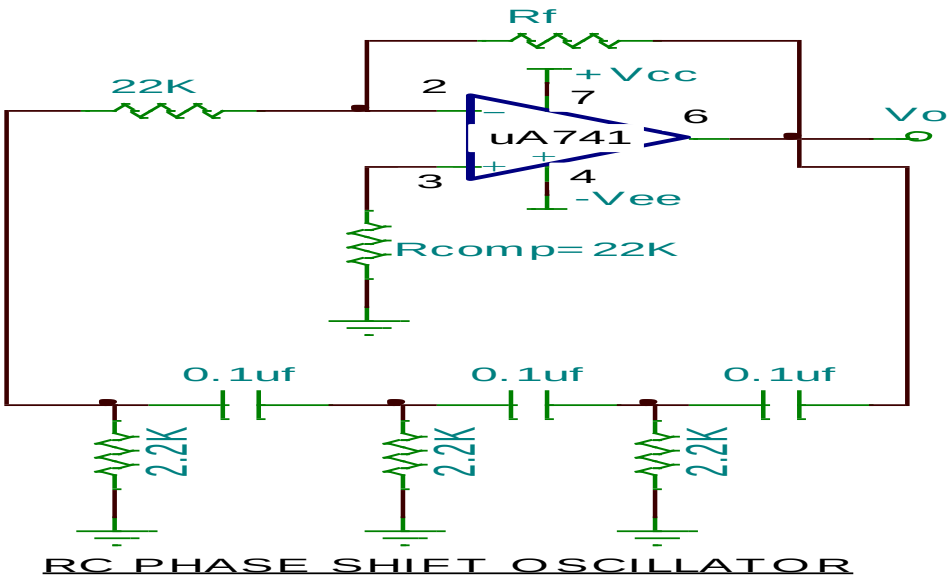
(a) RC PHASE SHIFT OSCILLATOR

AIM : Design a RC Phase Shift Oscillator with a frequency of oscillator of 300Hz

APPARATUS :

IC µA741 - 1 no's
Resistors – 22KΩ - 1 no's
– 2.2KΩ - 3 no's
Capacitor 0.1µF - 3 no's.
CRO, Dual Regulated Power Supply.

CIRCUIT DIAGRAM :



THEORY:

RC Phase Shift oscillator consists of an op-amp as the amplifier stage and three RC cascaded networks as the feed back circuit. The feedback circuit provides feedback voltage from the o/p back to the i/p of the Amplifier. The Op-Amp is used in the Inverting mode- therefore any signal that appears at the inverting terminal is shifted by 180^0 at the o/p. An additional 180 phase shift required for oscillation is provided by the cascaded RC networks. Thus the total phase shift of around the loop is 360^0. At some specific frequency when the phase shift of the

cascaded RC networks is exactly 180^0 and the gain of the amplifier is sufficiently large, the circuit will oscillates. This frequency is called the frequency of oscillation f_0 and is given by

$$f_0 = \frac{1}{2\pi RC\sqrt{6}}$$

to generate this frequency, the gain A_v must be at least 29

$$|R_f / R_1| = 29$$

$$R_f = 29\, R_1.$$

DESIGN PROCEDURE:

Let C= 0.1μF, $f_0 = \frac{1}{2\pi RC\sqrt{6}}$.

By substituting f_0 , $R = 1/ 2\pi\sqrt{6}(300)\ (0.1\text{x}10^{-6}) = 2.16\text{K}$, $R \approx 2.2\text{K}$

Since $|R_f / R_1| = 29$

$$R_f = 29\, R_1$$

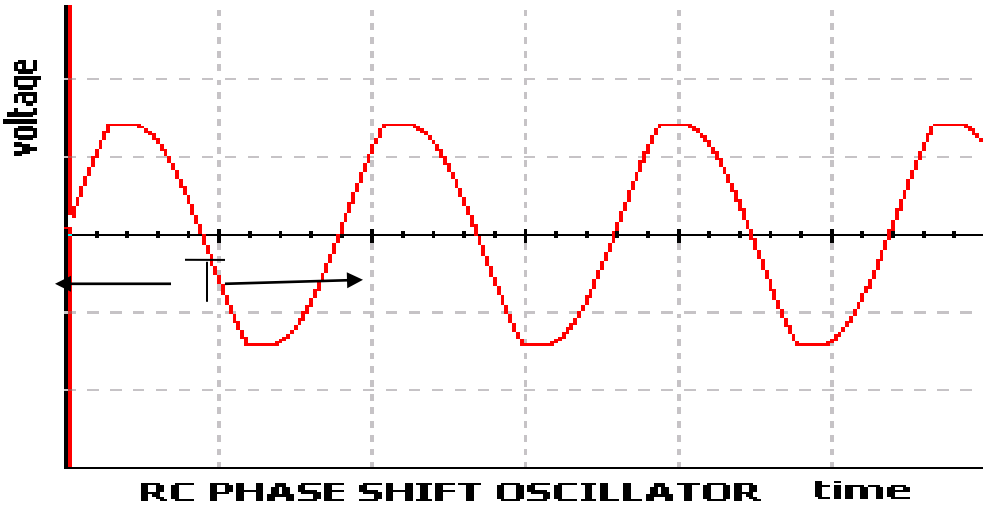
and $R_1 \geq 10R$

Let R_1 = 22K, and $R_f = 29R_1 = 29(22\text{K}) = 638\text{K}$, $\underline{R_f \approx 640\text{K}}$

PROCEDURE:

1. Made connections as per circuit diagram.
2. Switched on the dc supply to fix $+V_{cc}$ and $-V_{EE}$
3. Adjusted Rf pot until it satisfies the condition and output waveform.
4. Observed the o/p wave form on CRO Screen.
5. Ploted it on a graph sheet and foundd its time period.

EXPECTED WAVEFORM :



RESULT:

$f_{0(theoretical)}$ =_____Hz $f_{0(practical)}$ =_____Hz

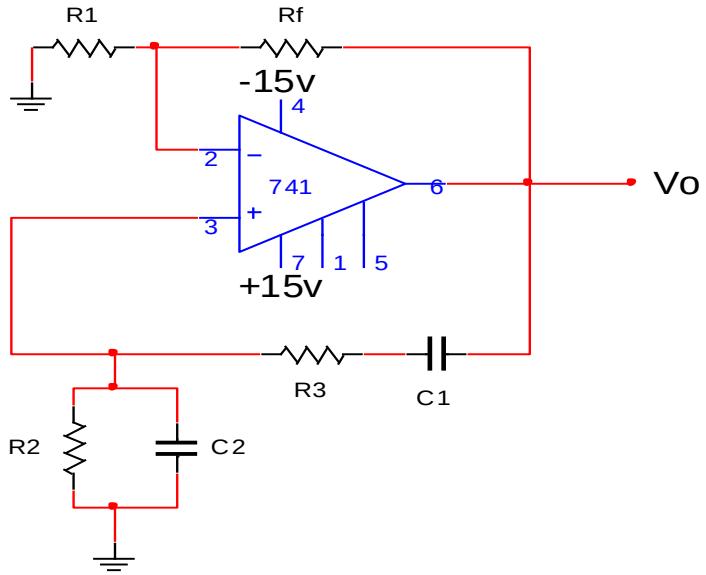
(b) WEIN BRIDGE OSCILLATOR

AIM : Design a wein bridge oscillator so that the frequency of oscillator is 1KHz.

APPARATUS:

IC 741 - 1 no
Resistors - 16KΩ - 2no's
10KΩ, 20 KΩ - 1 no each
Capacitors 0.01 µf – 2no's.
CRO, Dual Regulated Power Supply.

CIRCUIT DIAGRAM :



THEORY:

Wein bride oscillator consists of a bridge circuit connected between the amplifier output & input terminals. The bride has a series RC network in one arm and a parallel RC network in the adjoining arm. In the remaining two arms resistors R_1 and R_2 are connected. The phase angle criterion for oscillator is that the total phase shift around the circuit must be 0^0. This condition occurs when the bridge is balanced and as the circuit is in Non Inverting mode it will not produce any Phase Shift.

The Frequency Generated by the Circuit is $\mathbf{f = \frac{1}{2\pi RC}}$

To satisfy the Barkhausen Criterion that $A\beta \geq 1$. It is necessary that the gain of the non inverting Op-Amp Amplifier must be minimum 3.

$|A| \geq 3$ i.e. $1 + R_f/R_1 \geq 3$.

$R_f > 2R_1$.

DESIGN PROCEDURE:

Frequency Generated in a Wein bridge Oscillator is

$f = \frac{1}{2\Pi RC}$, Let $R = R_2 = R_3$

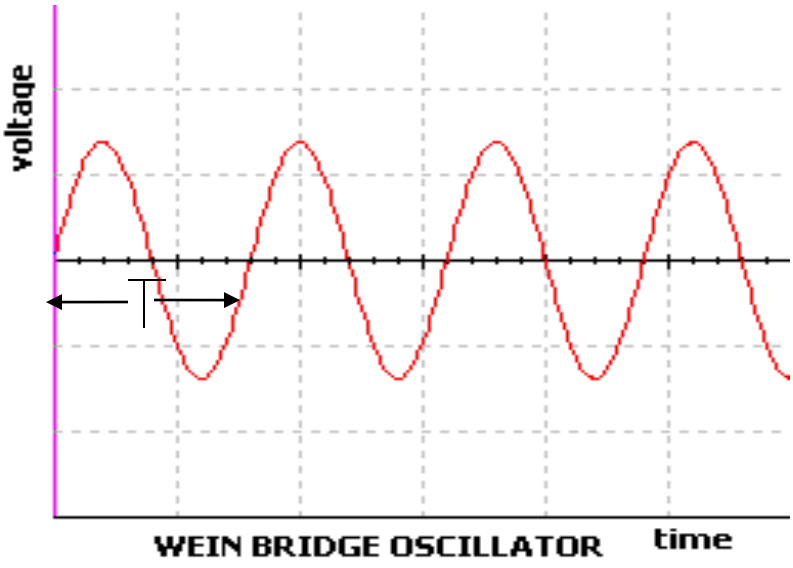
Let C = 0.01µf , then $R = \frac{1}{2\Pi . f . C} = \frac{1}{2\Pi x 10^{3} x 0.01 x 10^{-6}}$,

So $R = R_2 = R_3$ =16 K Ohms let R_1 = 10 K, As $R_f \geq 2R_1 \geq 20$K ohms.

PROCEDURE:

1. Connected the circuit as per the circuit diagram.
2. Switched on the DC power to fix + and – ve Voltages V_{CC} and - $V_{EE.}$
3. Observed the output waveform on CRO screen and trace it on a graph sheet.
4. Found out the period.

EXPECTED WAVEFORMS :



RESULT :

$F_{0(\text{ theoretical })}$ =_____Hz. $F_{0(\text{Practical })}$_____ Hz.

Viva Voice :

1. What is meant by barkhausen Criteria?

2. Examples of LC Oscillators.

3. Why we need only Positive feed back for Oscillator.

5. IC 555 Timers – Monostable Operation Circuits

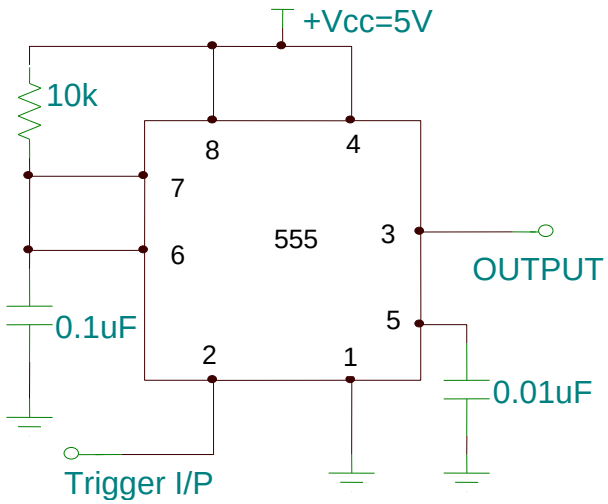
AIM **:** Study of Monostable Multivibrator using **555** IC timers.

APPARATUS:

IC 555		- 1no
Resistor	10KΩ	- 1no
Capacitors	0.1µF	- 1no.
	0.01µF	- 1 no's.

Function Generator, CRO, Dual Regulated Power Supply.

CIRCUIT DIAGRAM:



MONOSTABLE MULTIVIBRATOR

THEORY:

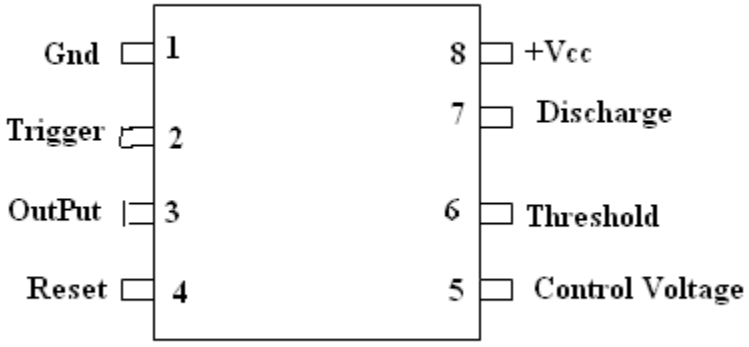
In a Steady state, transistor Q_1 of 555 timer is on and capacitor 'C' is shorted out to ground. However, upon application of a negative trigger pulse to pin2, transistor Q_1 is turned off, which release the short circuit across the external capacitor C and drives the o/p high. The capacitor now starts charging up towards V_{CC} through 10 K Resistor.

When the voltage across capacitor equals to 2/3 V_{CC} , comparators output switches from low to high, which in turn drives the o/p to its low via the o/p of the flip-flop. At the same time, the o/p of the flip-flop turns transistor Q_1 on, and hence capacitor C rapidly discharges through the transistor. The o/p of monostable remains low until a trigger pulse is again applied. Then the cycle repeats. So a Rectangular wave is produced at the output. The pulse width of the Pulse is

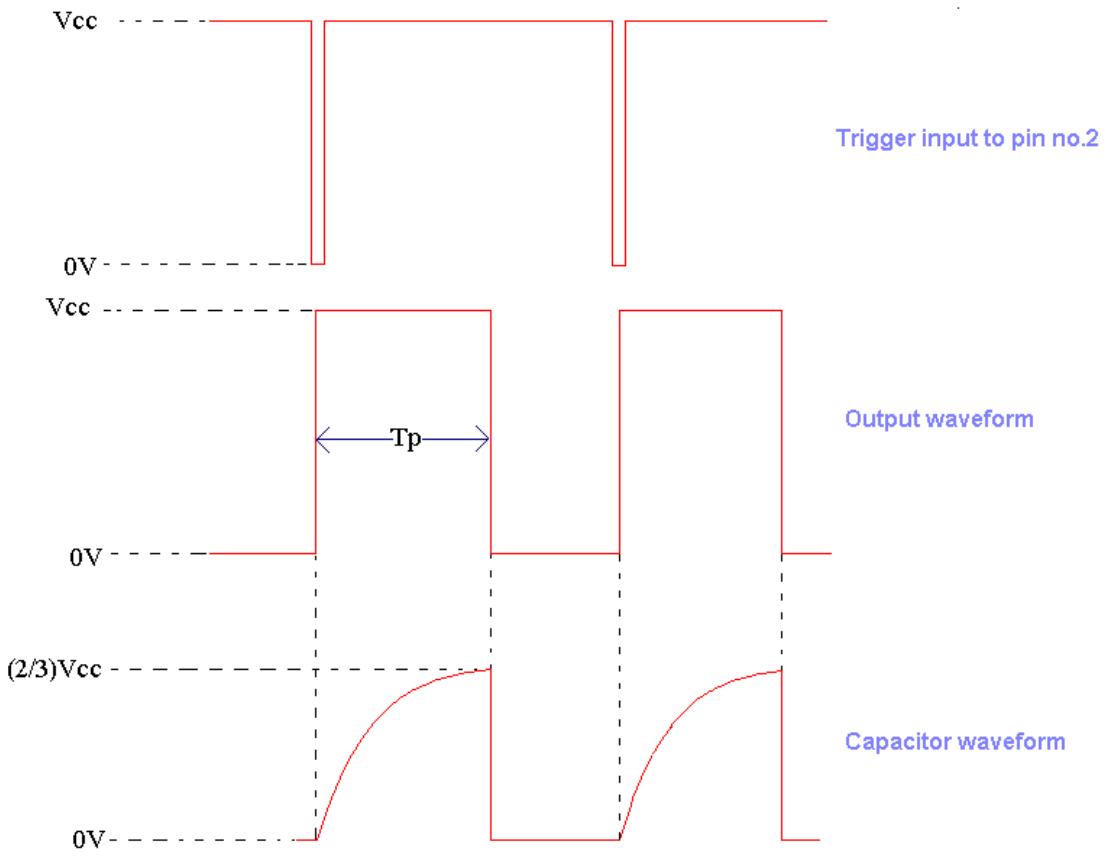
Controlled by the Charging time of the Capacitor. This depends on the time constant RC. Thus RC controls the Pulse width.

Pulse width $t_P = 1.1\ RC$.

PIN DIAGRAM OF 555 IC :



EXPECTED WAVEFORMS:



RESULT: Theoretical t_P = ----------

Practical t_P = ----------

Viva –Voice:

1. Explain the functionality of RESET pin.

2. List out the Applications of Monostable Multivibrator.

3. What is the Functionality of Control Voltage?

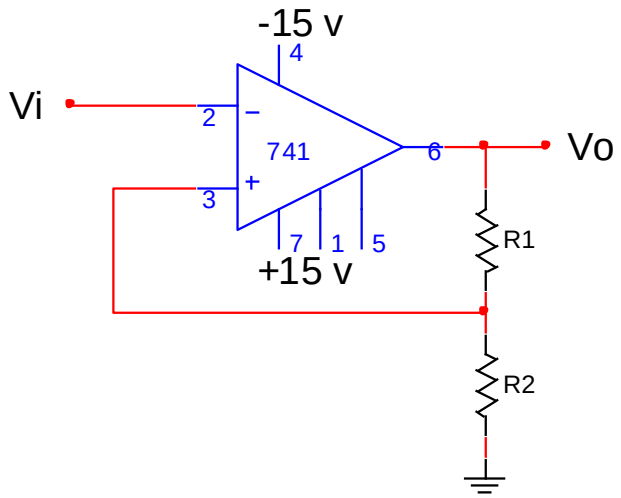
6. Schmitt Trigger Circuits – using IC 741 and IC 555

(a) Schmitt Trigger Using 741 IC

AIM : To design a Schmitt trigger circuit using IC 741. Draw input and output waveforms and transfer characteristic.

APPARATUS: IC - 741,
Resistors - 10k Ω
2.2 kΩ
Function Generator, CRO, Dual Regulated Power Supply, Multimeter.

CIRCUIT DIAGRAM:



THEORY:

As the input signal is applied to the Inverting terminal, it is also called Inverting Schmitt Trigger circuit. The Inverting mode produces opposite polarity output. There is a feedback to the Non inverting input which is of same polarity as that of output. This ensures positive feedback. Let the Feed back Voltage to the Non Inverting is V_{ref}.

When V_{in} is slightly positive than V_{ref} , the output gets driven into negative saturation at $-V_{sat}$ level. When V_{in} becomes more negative than $-V_{ref}$, then output gets driven into positive saturation at $+V_{sat}$ level. Thus output voltage is always at $+V_{sat}$ or $-V_{sat}$ but the voltage at which it changes its state is controlled by the resistance R_1 and R_2(feedback network).

+Vref is for positive saturation when Vo=+V_{sat} and is called Upper threshold voltage denoted as V_{ut}. –Vref is for negative saturation when Vo = -Vsat and is called lower threshold voltage denoted as V_{lt}.The values of these threshold voltage levels can be determined and adjusted by selecting proper values of R1 and R2.

Thus

$$VUT = \frac{+\,\text{Vsat R2}}{(\text{R1} + \text{R2})}$$

$$Vlt = \frac{-Vsat\ R2}{(R1+R2)}$$

Hysteresis is the graph of output voltage against input voltage. This is called transfer characteristics of Schmitt Trigger. The graph indicates that once the output changes its state, it remains there indefinitely until the input voltage crosses any of the threshold voltage levels. This is called **hysteresis** of Schmitt trigger. The hysteresis is also called **dead band** or **dead zone**.

The difference between V_{ut} and V_{lt} is called width of the hysteresis denoted as H.

$$H = Vut - Vlt = \frac{+Vsat\ R2}{R1 + R2} - [\frac{-Vsat\ R2}{R1 + R2}]$$

Therefore,

$$\text{H} = \frac{2\ \text{Vsat R2}}{\text{R1} + \text{R2}}$$

PROCEDURE :

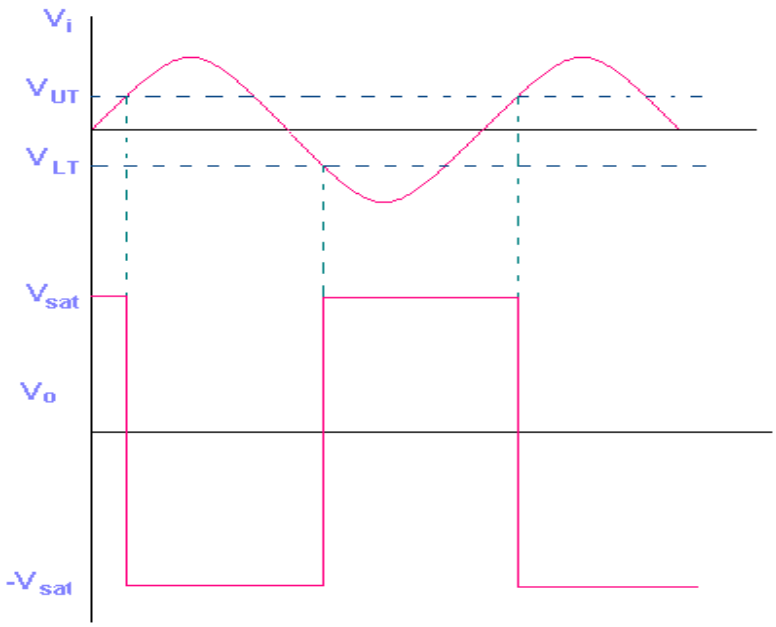
1. Connected the components as per the circuit diagram, let R1 = 10 K and R2 = 2.2kOhms.
2. Observed the output voltage, which is at positive saturation V_+ initially.
3. Applied a DC input voltage and increased it from 0 v slowly, observing the output.

4. Noted down the input voltage at which output transition occured from V_+ to V_-. This is upper triggering point (UTP).
5. Then slowly decreased the input while observing the output . Noted down the input voltage at which reverse transition occured in the output i.e. from V_-. to V_+. This is lower triggering point (LTP).
6. Found the hysteresis voltage which is the difference between UTP and LTP.

$$V_H = V_{UTP} -- V_{LTP}$$

7. Applied a square wave input of 10 v at 1 kHz.
8. Measured and sketched output and transfer characteristics.
9. From transfer characteristic measured LTP, UTP and hysteresis voltage V_H.

EXPECTED WAVEFORMS : Input and output waveforms:



RESULT :

Theoretical Values of UTP : ---------- LTP : ----------

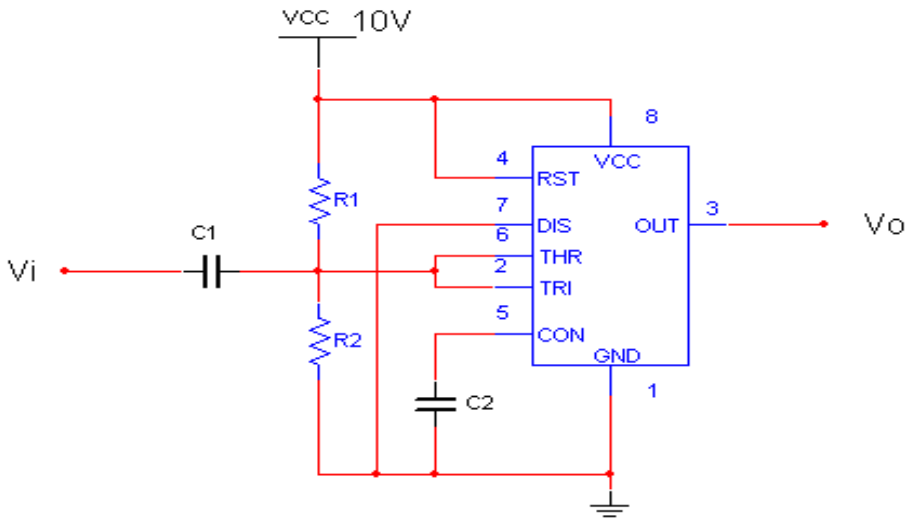
Practical Values of UTP : ---------- LTP : ----------

(b) SCHMITT TRRIGER using IC 555

AIM : To design a Schmitt trigger circuit using IC 555. Draw input and output Waveforms and transfer characteristic.

APPARATUS: IC 555
Resistors $R_1 = R_2 = 100K\Omega$,
Capacitors $C_1 = C_2 = 0.01\mu F$.
Function Generator, CRO, Dual Regulated Power Supply.

CIRCUIT DIAGRAM:



THEROY:

The input is given to the pins 2 and 6 which are tied together. Pin 4 and 8 are connected to supply voltage +Vcc . The common point of two pins 2 and 6 is externally biased at Vcc/2 Through the resistance network R_1 and R_2. Generally $R_1=R_2$ to get the biasing of Vcc/2. The upper comparator will trip at 2/3 Vcc while lower comparator at1/3 Vcc . The bias provided by R1 and R2 is centered within these two thresholds. Thus when sine wave of sufficient amplitude, greater than Vcc/6 is applied to the circuit as input, it causes the internal flip- flop to alternately set and reset. Due to this, the circuit produces the square wave at the output, as shown in the figure. The frequency of square wave remains same as that of input. The Schmitt trigger can operate with the input frequencies up to 50 kHz.

PROCEDURE:

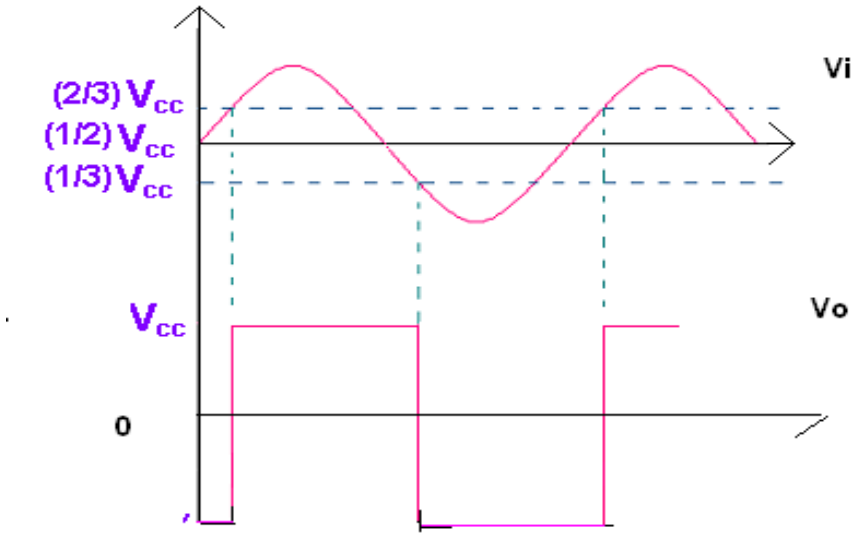
1. Connected the components as per the circuit diagram.
2. Observed the output voltage, which is at V+ initially.
3. Applied a DC input voltage and increased it from 0 v slowly, observing the output.(For this disconnect C1 capacitor).
4. Noted down the input voltage at which output transition occured from V_+ to V_-.This is upper triggering point (UTP).
5. Then slowly decreased the input while observing the output. Note down the input voltage at which reverse transition occured in the output i.e. from V_-. To V_+. This is lower triggering point (LTP).
6. Found the hysteresis voltage, which is the difference between UTP and LTP.

$$V_H = V_{UTP} - V_{LTP}$$

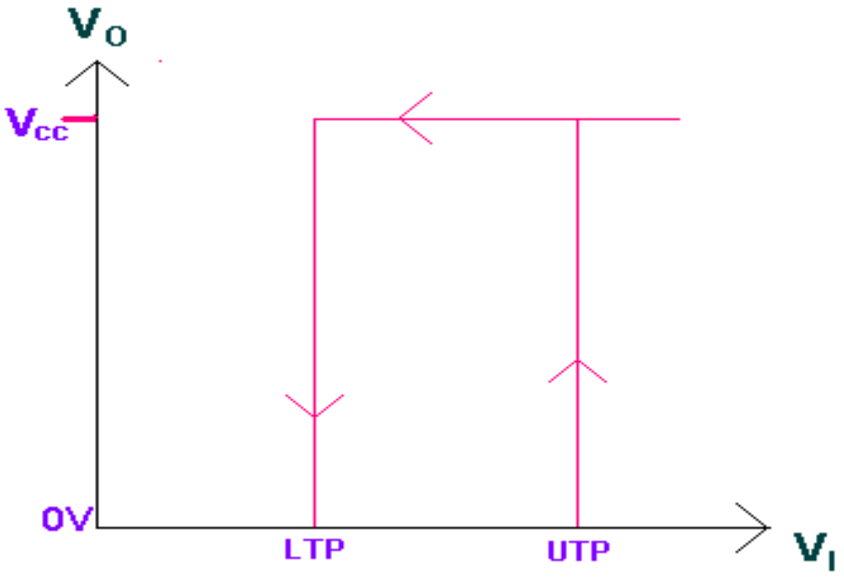
7. Applied a sine wave input of 10v at 1 kHz.
8. Measured and sketched output and transfer characteristics.
9. From transfer characteristic measured LTP, UTP and hysteresis voltage V_H.

EXPECTED WAVEFORMS:

Input and output waveforms:



Transfer characteristic:



RESULT:

Theoretical Values of UTP : ---------- LTP : ----------

Practical Values of UTP : ---------- LTP : ----------

Viva Voice:

1. What is the main application of Schmitt trigger?

2. What is the Difference between Astable and Schmitt trigger?

3. Why 741 Schmitt trigger is called Regenerator Ckt.

7. IC 565 – PLL Applications

Aim: To study phase lock loop and its capture range, lock range and free running VCO Frequency.

Apparatus and Components Required:

S.No	Equipment/Component	Specifications/Value	Quantity
1	565 IC	- --	1
2	Capacitors	0.1μF,0.01μF ,1μF	Each one
3	Resistors	10kΩ 680Ω	1 2
4	Regulated Power supply	(0 – 30V),1A	1
5	Function Generator	(1HZ – 1MHz)	1
6	Cathode ray oscilloscope	(0 – 20MHz)	1
7	Bread board		1

Circuit Diagram:

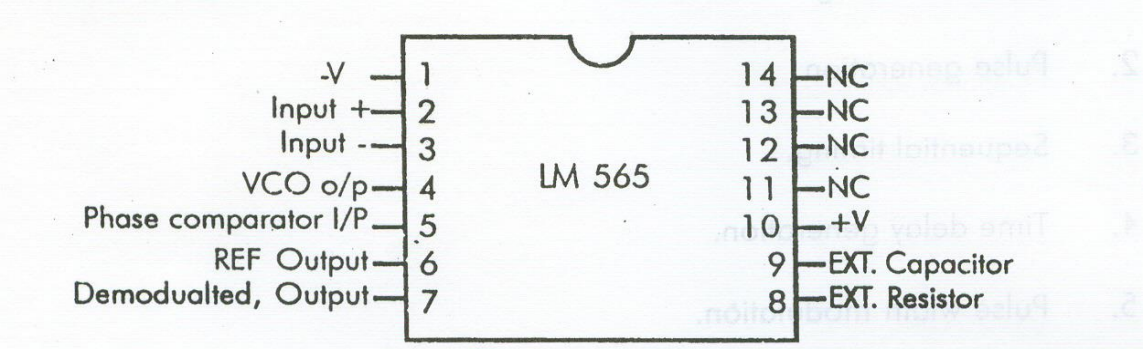


Fig.1 Pin Diagram of LM 565

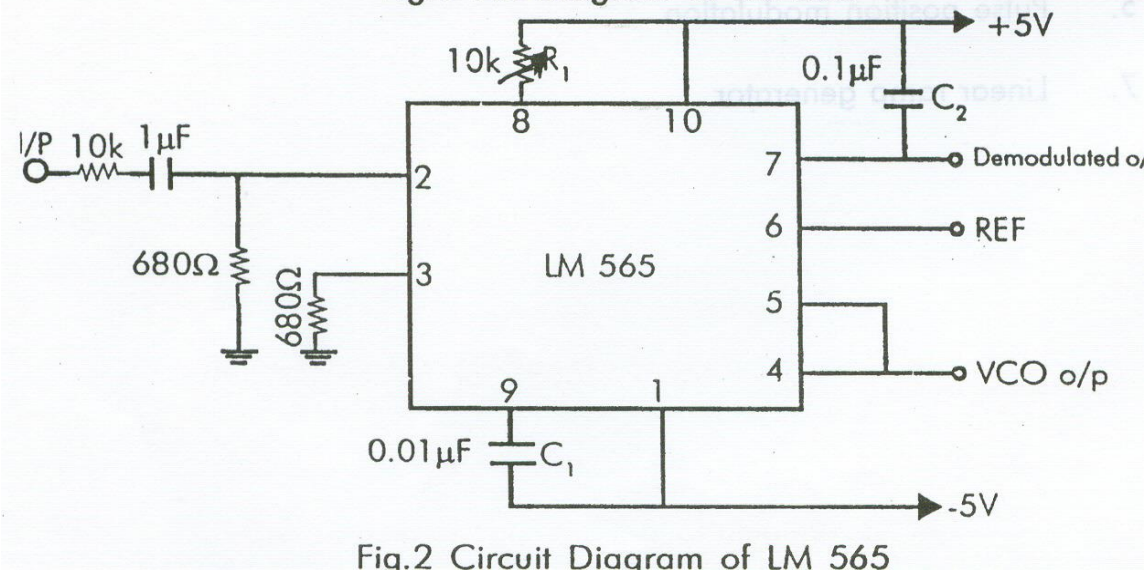
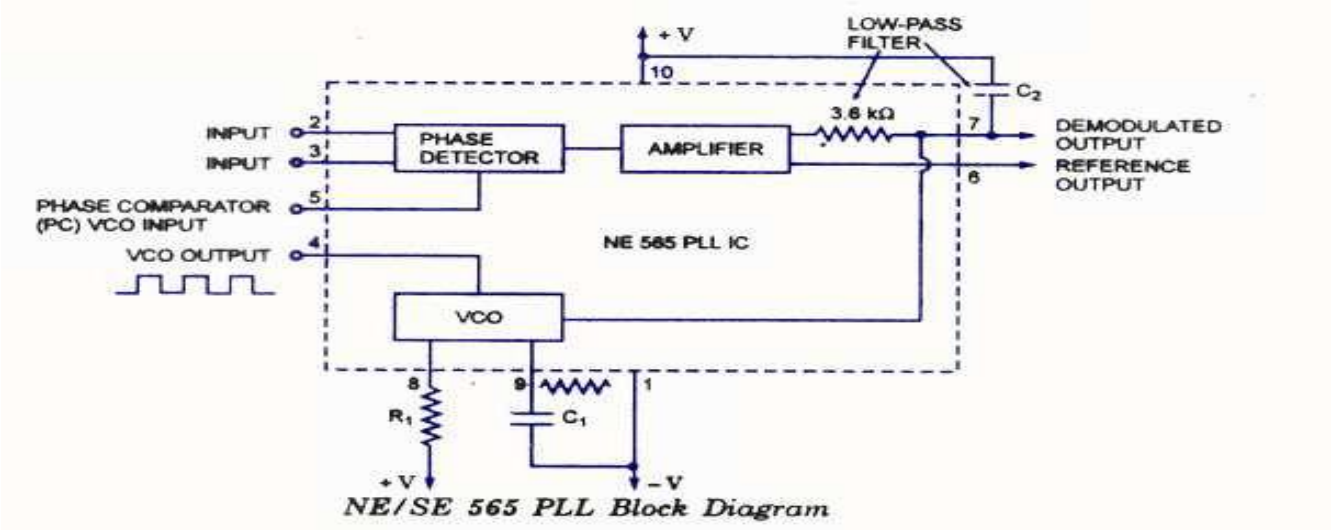


Fig.2 Circuit Diagram of LM 565

Theory:

PLL has emerged as one of the fundamental building block in electronic technology. It is used for the frequency multiplication, FM stereo detector, FM demodulator, frequency shift keying decoders, local Oscillators in TV and FM tuner.The block diagram of a PLL is shown in the fig. below.



NE/SE 565 PLL Block Diagram

The PLL goes through 3 states:

1. Free running state
2. Capture range/mode
3. Phase lock state.

Before input is applied, the PLL is in the free running state. Once the input frequency is applied, the VCO frequency starts to change and the PLL is said to be the capture range/mode. .

The VCO frequency continues to change (output frequency)until it equals the input frequency and the PLL is then in the phase locked state. when phase is locked, the loop tracks any change in the input frequency through its repetitive action.

Lock Range or Tracking Range:

$$F_L = \pm \frac{8f_o}{V} \text{ Hz [v=peak to peak voltage of VCO at CRO]}$$

Capture Range :(fc): is the range of frequencies in the vicinity of fo over which the loop will acquire lock with an input signal initially starting out of lock and is given by..

$$\text{Capture range } F_C = \pm \left\{ \frac{F_L}{2\pi(3.6*10^3)C_2} \right\}^{1/2}$$

Where C_2=is the filter capacitor in micro farads.

Procedure:

1. Make connections of the PLL as shown in figure 1.
2. Measure the free running frequency of" VCO at pin 4.wilh the i/p signal Vin, setequal to zero. Compare it with the calculated value = 0.25/RTCT
3. Now apply the i/p signal of 1 VPP, square wave at a 1 KHz to pin 2.connect onechannel of the scope to pin2 and display this signal on the scope.
4. Gradually increase the i/p frequency till the PLL is locked to the input frequency. Thisfrequency f1 gives the lower end of the capture range.Go on increasing the i/pfrequency, till PLL tracks the i/p signal, say. to a frequency gives the upper end of the lock range. if i/p frequency is increased further,theloop will get unlocked.
5. Now gradually decrease the i/p frequency t i l l the PLL is again locked. This is thefrequency (f the upper end of the capture range. Keep on decreasing the i/pfrequency until the loop is unlocked. This frequency ‘f4’ gives lower end of lock range.
6. The lock range ΔfL=f2-f4. Compare it with the calculated value of ± Also the capture range is Δfc= (f3-f1). Compare it with the calculated Value of capture range.

Tabular Column:

S.No.	Theoretical calculations	Practical calculations
1.Freerunning Oscillations(in KHz)		
2. Lock range(in KHz)		
3. Capture Range(in KHz)		

Result:

Theoretical values of lock range, capture range, free running frequency are compared With the practical values.

Review Questions:

1. What is PLL?

2. What are the basic building blocks of a PLL?

3. What is the need for a low-pass filter in a PLL?

4. What is the role of VCO in a PLL chip?

5. In a PLL system define the locked state.

6. Define the lock range of a PLL system

7. Define capture range of a PLL

8. Voltage Regulator using IC 723, Three terminal voltage regulators 7805, 7809, 7912

Aim: To design a low voltage variable regulator of 2 to 7V using IC 723 and obtain the regulation characteristics of three terminal voltage regulators.

Apparatus and Components Required:

S.No.	Equipment/ Component name	Specifications/ Value	Quantity
1	IC723,7805,7809, 7912	----	1
2	Resistors	3.3KΩ,4.7KΩ,100 Ω,1KΩ,	Each one
3	Variable Resistors	1KΩ, 5.6KΩ	Each one
4	Regulated Power supply	0 -30V,1A	1
5	Multimeter	3 ½ digit display	1
6	Milli ammeter	0-150 mA	1

Theory:

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage variations. Using IC 723, we can design both low voltage and high voltage regulators with adjustable voltages.

For a low voltage regulator, the output VO can be varied in the range of voltages Vo<Vref, where as for high voltage regulator, it is VO >Vref. The voltage Vref is

generally about 7.5V. Although voltage regulators can be designed using Op-amps, it is quicker and easier to use IC voltage Regulators.IC 723 is a general purpose regulator and is a 14-pin IC with internal short circuit current limiting, thermal shutdown, current/voltage boosting etc. Furthermore it is andjustable voltage regulator which can be varied over both positive and negative voltage ranges. By simply varying the connections made externally, we can operate the IC in the required mode of operation.

Typical performance parameters are line and load regulations which determine the precise characteristics of a regulator. The pin configuration and specifications are shown in the Appendix-A.

A voltage regulator is a circuit that supplies a constant voltage regardless of changes in load current and input voltage. IC voltage regulators are versatile, relatively inexpensive and are available with features such as programmable output, current/voltage boosting, internal short circuit current limiting, thermal shunt down and floating operation for high voltage applications. The 78XX series consists of three-terminal positive voltage regulators with seven voltage options. These IC's are designed as fixed voltage regulators and with adequate heat sinking can deliver output currents in excess of 1A.The 79XX series of fixed output voltage regulators are complements to the 78XX series devices. These negative regulators are available in same seven voltage options. Typical performance parameters for voltage regulators are line regulation, load regulation, temperature stability and ripple rejection. The pin configurations and typical parameters at 25^0C.

Circuit Diagram:

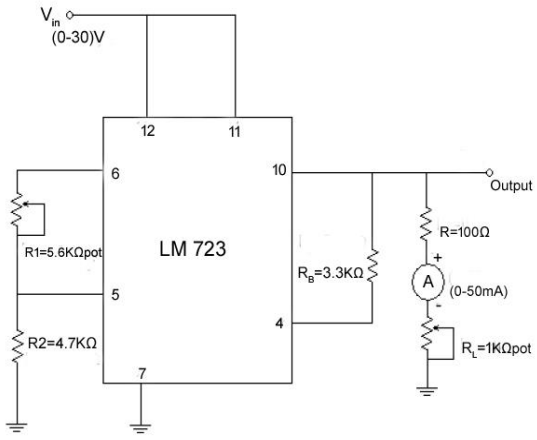


Figure:1.Voltage Regulator

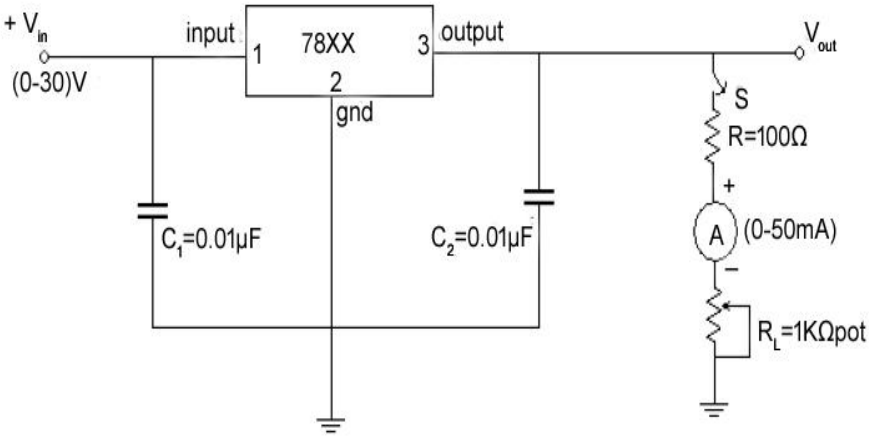


Figure: 2. Possitive Voltage Regulator

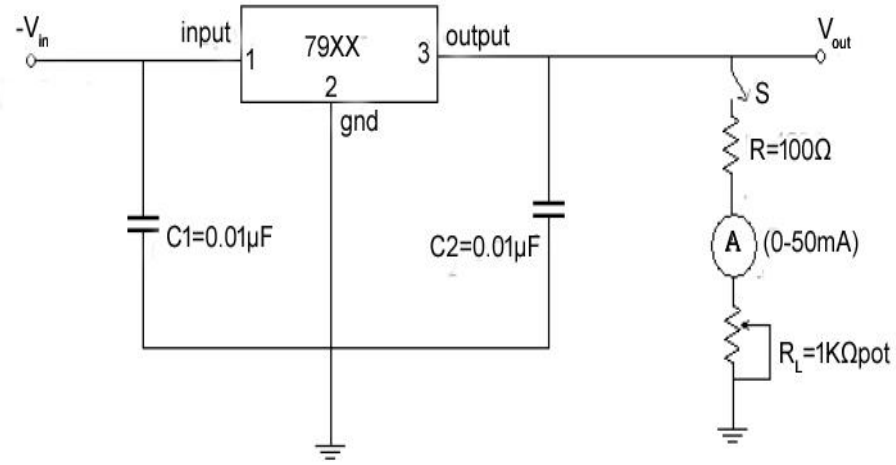


Figure: 3. Negative Voltage Regulator

Design of Low voltage Regulator :-

Assume I_o= 1mA,V_R=7.5V
R_B = 3.3 KΩ
For given V_o
$R_1 = (V_R – V_O) / I_o$
$R_2 = V_O / I_o$

Procedure:

a) Line Regulation*:*

1. Connect the circuit as shown in Figure 1.
2. Obtain R_1 and R_2 for V_o=5V
3. By varying V_n from 2 to 10V, measure the output voltage V_o.
4. Draw the graph between V_n and V_o as shown in model graph (a)
5. Repeat the above steps for V_o=3V
6. Connect the circuit as shown in figure 1 by keeping S open for 7805.
7. Vary the dc input voltage from 0 to 10V in suitable stages and note down the Output voltage in each case as shown in Table1 and plot the graph between input Voltage and output voltage.
8. Repeat the above steps for negative voltage regulator as shown in Fig.2 for 7912 for an input of 0 to -15V.
9. Note down the dropout voltage whose typical value = 2V and line regulation typical value = 4mv for Vin =7V to 25V.

b) Load Regulation*: For V_o=5V*

1. Set $V_i$such that V_O= 5 V
2. By varying R_L, measure I_L and V_o
3. Plot the graph between I_L and $V_o$as shown in model graph (b)
4. Repeat above steps 1 to 3 for V_O=3V.
5. Connect the circuit as shown in the figure 1 by keeping S closed for load regulation.
6. Now vary R1 and measure current IL and note down the output voltage Vo in each case as shown in Table 2 and plot the graph between current IL and Vo.
7. Repeat the above steps as shown in Fig 2 by keeping switch S closed for Negative Voltage regulator 7912.

c) Output Resistance:

Ro= (VNL – VFL)/ VFL Ohms

VNL - load voltage with no load current

VFL - load voltage with full load current

IFL - full load current

Sample Readings:

a) Line Regulation:

$V_o$set to 5V Vo set to 3V

V_i (V)	V_o(V)

V_i (V)	V_o(V)

a) Load Regulation:

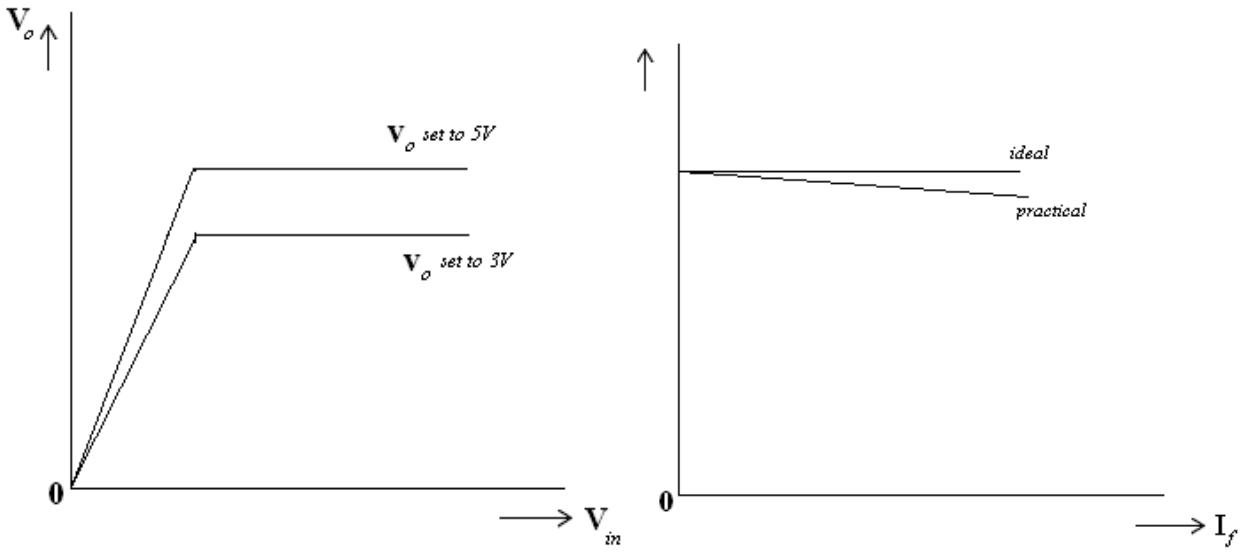
Vo set to 5VVo set to 3V

I_L(mA)	V_o(V)

I_L (mA)	V_o(V)

Model graphs:

a) Line Regulation: **b) Load Regulation**:



Results: Low voltage variable Regulator of 2V to 7V using IC 723, 7805, 7809.7912 is Designed. Load and Line Regulation characteristics are plotted.

Viva Questions:

1. What is the effect of R_1 on the output voltage?
2. What are the applications of voltage regulators?
3. What is the effect of V_i on output?

9. Sample and Hold LF398 IC

Aim: To observe the working of Sample and Hold Circuit by using LF398 IC.

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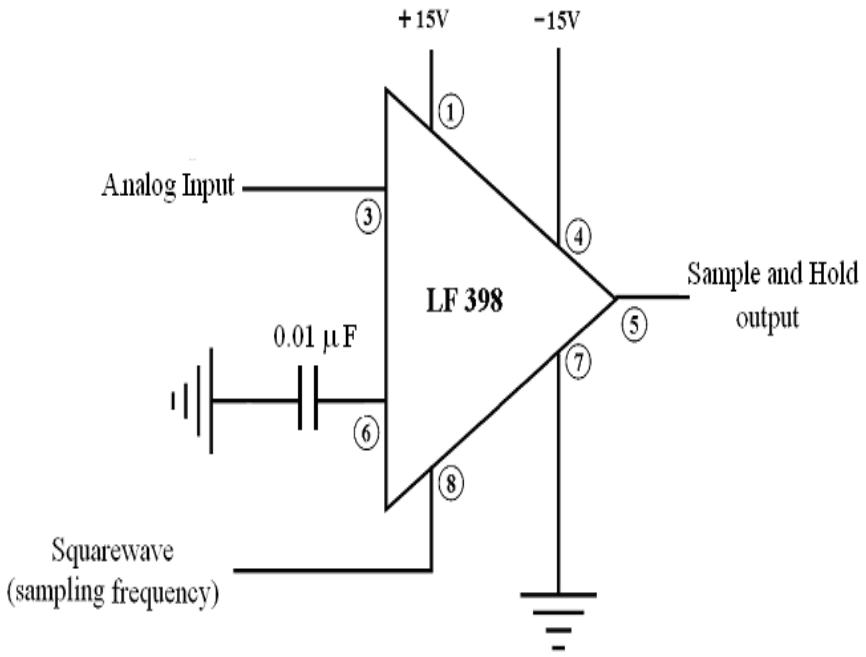
Apparatus: IC LF398
Capacitor – 0.01uf
Function generator
Regulated power supply
CRO
Connecting wires.

Theory:

In sample and hold circuit, it converts continuously varying analog signal to discrete flat top samples and holds its value at a constant level for a specified minimum period of time. LF398 is a monolithic sample-and-hold circuit utilizing BI-FET technology for accurate fast acquisition of input signal. A sample and hold circuit is an analog device that samples (captures) the voltage of a continuously varying analog signal and holds (locks) its value at a constant level for a specified minimum period of time (hold time). They are typically used in analog-to digital converters to eliminate variations in input signal that can corrupt the conversion process.

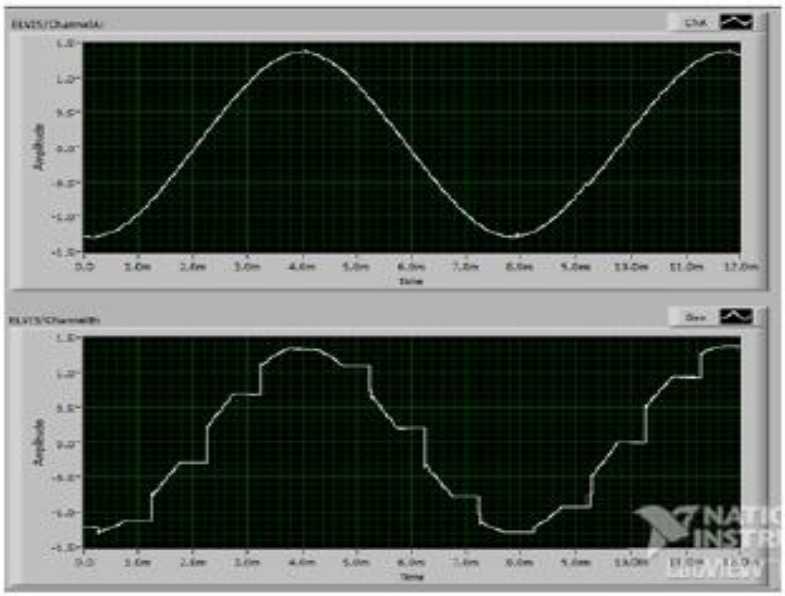
Circuit diagram:



Procedure:

1. Connect the circuit as shown in the above figure.
2. Apply analog input sine wave of 1 kHz to pin 3 of the IC.
3. Apply Sampling signal square wave of frequency in between 15 kHz-20 kHz of 80% duty cycle to pin 8 of the IC.
4. Observe the output from pin 5 and draw the wave forms.

Model graphs:



Result: Hence, the operation of IC LF398 is observed.

PART-B

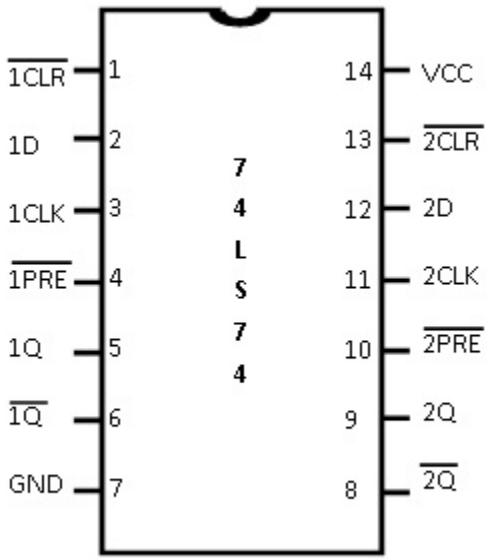
1. D Flip-flop(74LS74)& JK Master Slave Flip-flop(74LS73)

(a) D – FLIP FLOP

AIM : To verify the working of a D – Flip flop using digital IC 74LS74

APPARATUS : IC 7474, Breadboard Trainer system, Patch chords

PIN DIAGRAM:



THEORY:

The D flip-flop tracks the input, making transitions with match those of the input D. The D stands for "data"; this flip-flop stores the value that is on the data line. It can be thought of as a basic memory cell. This Integrated Circuit contain two independent D-type positive-edge triggered flip flop circuits. A low level at the preset or clear input pins set or resets the outputs regardless of the levels of the other inputs. When preset and clear are disabled (high logic level), data at the D input meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Following the hold time interval, data at the D input may be changed without affecting the levels at the outputs.

PROCEDURE:

1. Connected the trainer to the mains and switched on the power supply, Used the power supply. i.e. +5V [note: supply is internally connect to the circuit so no need to connect externally].
2. Made the connections of preset and Clear, Clock as given in Truth Table.
3. Verified the operation of D – FF for various combination of preset (S) and clear (R)

TRUTH TABLE:

INPUTS				OUTPUTS	
$\overline{PRE}$	$\overline{CLR}$	CLK	D	Q_{n+1}	$\overline{Q}_{n+1}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	H	H	H	L
H	H	H	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

RESULT: Verified the working of D – Flip flop using digital IC 74LS74.

(b)JK Master Slave Flip-flop

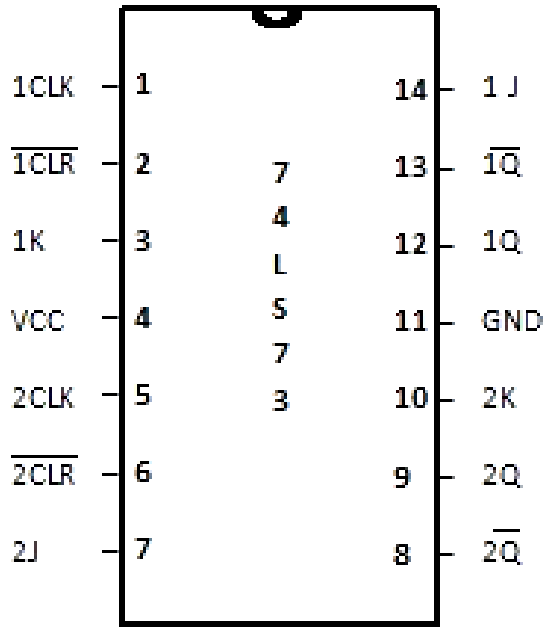
AIM : To verify the working of a JK Master Slave Flip flop using digital IC7473.

APPARATUS: IC 7473

Breadboard Trainer system

Patch chords

PIN DIAGRAM:



THEORY:

Master Slave JK Flip flop is a cascaded of two SR flip flops with feedback from the outputs of the second to the inputs of the first. Positive clock pulses are applied to the first flip flop and the clock pulses are inverted before these are applied to the second flip-flop. Since the Second flip-flop simply follows the first one and is called as slave and the first one is called as master. Hence this configuration is called as Master Slave flip-flop. The state of the master – slave flip-flop changes at the negative transition (trailing edge) of the clock pulse. Thus the race around condition is eliminated in master slave JK Flip flop.

This Integrated Circuit contain two independent J-K type positive-edge triggered flip flop circuits. A low level at the preset or clear input pin resets the outputs regardless of the levels of the other inputs, this lack of regard to the clock cycle is called asynchronous. The values at J and K determine the mode of operation for the flip flop. If both J K are high, then with each

clock pulse received, the outputs Q and Q' will toggle. JK Flip Flop circuits are important in building synchronous and asynchronous counters, registers, frequency divide by two circuits, etc.

1J , 1K , 1 CLK, 1CLR' are the inputs to the JK Flop – Flop1.

2J , 2K , 2 CLK, 2CLR' are the inputs to the JK Flop – Flop2.

PROCEDURE:

1. Made the connections as shown in figure using the pin details of the IC used.
2. Switched on the Power Supply and kept CLR =0 verified weather the Outputs are cleared or not.
3. Kept CLR =1 and Applied the Clock pulse for different input Combinations of JK.

TRUTH TABLE:

INPUTS				OUTPUTS	
CLR	CLK	J	K	Q_{n+1}	Q'_{n+1}
L	X	X	X	L	H
H	H	L	L	Q_0	Q_0
H	H	H	L	H	L
H	H	L	H	L	H
H	H	H	H	Toggle	

RESULT: Verified the working of JK Master Slave Flip flop using digital IC 74LS73.

Viva Voice:

1. Using IC 7474 and Required AOI obtain the Truth table of JK Flip Flop.

2. What is meant by a clocked flip-flop?

3 What is meant by excitation table?

4 What is the difference between flip-flop and latch?

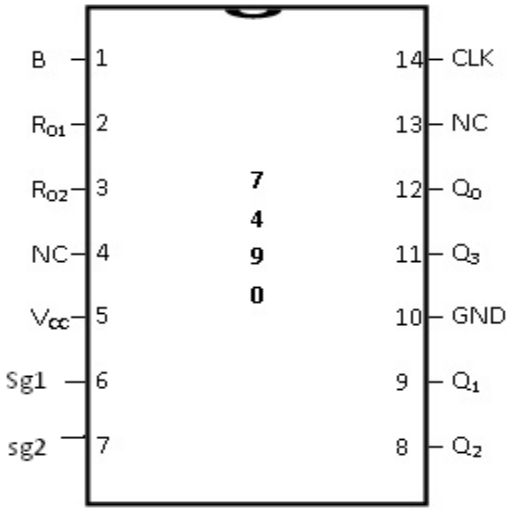
2. Decade counter (74LS90) and Up-down Counter (74LS192)

(a) Decade Counter using 74LS90

AIM : To verify the working of a decade counter using digital IC.

APPARATUS: IC 7490, IC Trainer Kit, Connecting wires , CRO

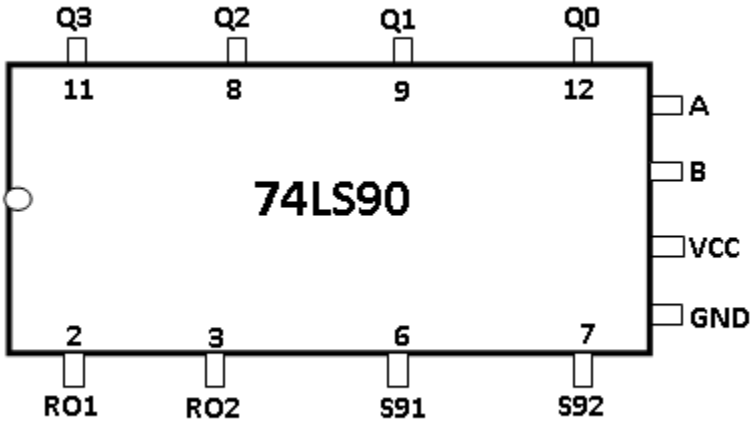
PIN DIAGRAM:



THEORY:

The 7490 IC can be configured into different modes depending on the applications required. In its most common mode, the 7490 is used as a general purpose decade counter, where only one of its 10 lines is active at any given time. Sending in clock pulses into its CLK input pin causes the currently active line to shut off and consequentially enables the next line in the sequence. After ten occurrences of this pattern, the device resets and line 0 starts the sequence over. By running one of the output lines into the reset pin, count sequences can be controlled to any length from one to ten. This chip is suitable for chasing light circuits where only one light is one at a time. If counts of more than 10 are required, multiple 7490s can be cascaded, with suitable external controlling logic, to expand the sequence. Other applications might include, sequence controllers, stepper motor controllers, microcontroller assisted display drivers, etc.

FUNCTIONAL DIAGRAM :



Q0 , Q1, Q2, Q3 --------- Outputs

PROCEDURE:

1. Given CLK to A and connected B to Qo output.
2. Connected R01, R02, Sg1 and Sg2 to logic 0(zero)
3. Checked for the count from 0000 – 1001.
4. To observe counter output in decimal, connected counter outputs Q0,Q1,Q2 and Q3 to the seven segment display (D0,D1,D2 and D3) pins. Or (Connect to the LEDs in Sequence).

FUNCTIONAL TABLE:

R_{01}	R_{02}	R_{03}	R_{04}	Q_3	Q_2	Q_1	Q_0
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
X	L	X	L	COUNT			
L	X	L	X	COUNT			
L	X	X	L	COUNT			
X	L	L	X	COUNT			

TRUTH TABLE:

	OUTPUT			
COUNT	Q_3	Q_2	Q_1	Q_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

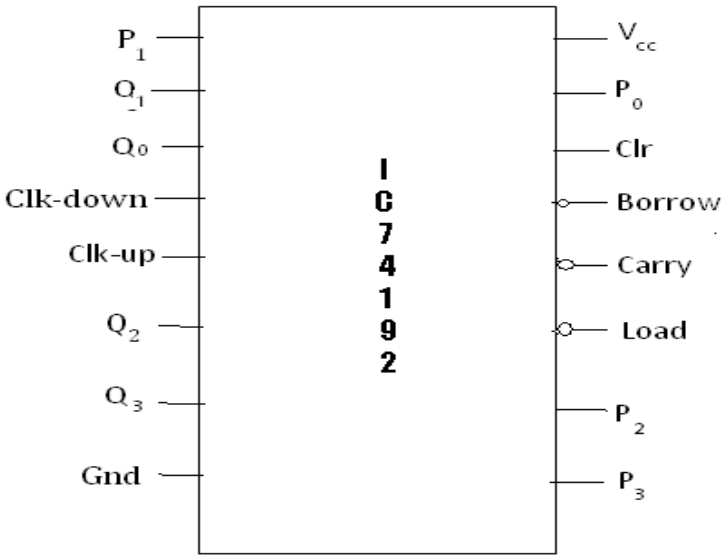
RESULT: verified the working of a decade counter using 74LS90 digital IC.

b) UP DOWN COUNTER

AIM : Realization of 4-bit synchronous up/down counter and mod- N counter using IC 74192 .

APPARATUS : IC Trainer kit,
IC 74192.

PIN CONIGURATION :



Here, P_0, P_1, P_2, and P_3 are preset inputs.

Clr is the clear input.

Clk-up and Clk-down are clock inputs.

Q_0, Q1, Q_2 and Q_4 are the counter outputs.

Carry and Borrow are the outputs used for cascading the counters.

THEORY:

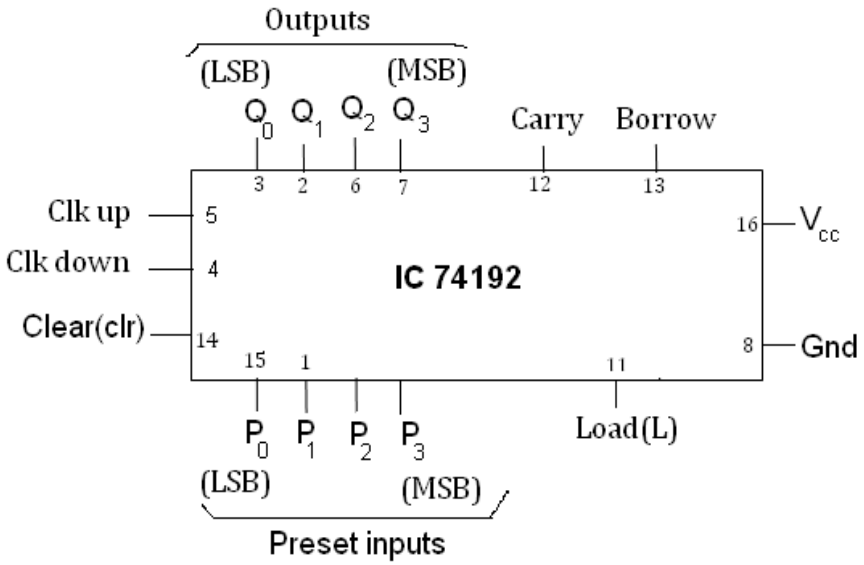
Asynchronous counters have the advantage of simplicity, but their speed is very low since the flip-flops are not clocked simultaneously and in these counters output of one flip-flop is used as clock input for the next flip-flop.

These limitations can be overcome with the use of synchronous or parallel counters in which all the flip-flops are clocked simultaneously. Thus the total delay is less no matter how many flip- flops are used in the counters and this delay will be much lower than asynchronous counters with the same number of flip-flops and Also synchronous counters can be designed for any count sequence, that is need not be straight binary. These counters can be designed with S-R, J-K, D or T- type flip- flops.

The drawback of synchronous counters is that it requires more circuitry than the asynchronous counters. Some synchronous counters are available in MSI. All these IC's are positive edge triggered, that is change of output state, synchronous loading and clearing takes place on the positive edge of the input clock pulse.IC74192 is a 4-bit decade (BCD) up/down counter with asynchronous preset and clear features. IC74193 is a 4-bit binary (mod 16) up/down synchronous counter with asynchronous preset and clear features.

In these counters for up counting the clock is applied at CK- UP terminal with CK-DOWN connected to logic '1' and for down counting clock is applied at the CK-DOWN terminal with CK-UP connected to logic '1'. For cascading these counter IC's the carry and borrow outputs of each stage are to be connected to the CK-UP and CK-DOWN inputs of the succeeding stage respectively.

FUNCTIONAL DIAGRAM:



FUNCTION TABLE :

Load	Clear	Clock up	Clock down	Mode
×	1	×	×	Reset to Zero
1	0	↑	1	Up Count
1	0	1	↑	Down Count
0	0	×	×	Preset
1	0	1	1	Stop Count

PROCEDURE: a) Realization of 4 bit-Up-Counter (÷ 10 Counter)

1) Connected the circuit as shown in Functional Diagram using the pin details of the IC used.
2) Switched on the power supply. For up- counting, initially cleared the outputs by connecting the clear input to logic '1' level then kept Clear=0, Load=1,Clk-down =1 levels and applied 1Hz clock or mono pulse to clock-up input,
3) Observed the count sequence at the outputs Q,Q, Q and Q .the count sequence is given by:0000 to 1001(i.e.,0,1,2,……..,8,9,0,1,2…….).

Truth Table (Count Sequence Table):

Number of input pulses	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

Note: The carry and borrow outputs are normally at logic '1' level. If the outputs Q_3,Q_2, Q_1 and Q_0 changes from 1001 to 0000 , then carry = 0, else carry =1.

PROCEDURE: b)Realization of 4- bit Down – Counter:

1) Connected the circuit as shown in figure-1 using the pin details of the IC used.
2) Switched on the power supply. For Down- Counting, initially cleared the outputs by connecting the clear input to logic '1' level then kept Clear=0, Load=1,Clk-up =1 levels and applied 1Hz clock or mono pulse to clock-down input.
3) Observed the count sequence at the outputs Q_3,Q_2, Q_1 and Q_0 .The count sequence is given by:1001 to 0000(i.e.,9,8,7,……..,2,1,0,9,8,7…….).

Number of input pulses	Outputs			
	Q_3	Q_2	Q_1	Q_0
0	1	0	0	1
1	1	0	0	0
2	0	1	1	1
3	0	1	1	0
4	0	1	0	1
5	0	1	0	0
6	0	0	1	1
7	0	0	1	0
8	0	0	0	1
9	0	0	0	0
10	1	0	0	1

Note: If the outputs Q_3,Q_2, Q_1 and Q_0 changes from 0000 to 1001, then borrow = 0,else borrow = 1.

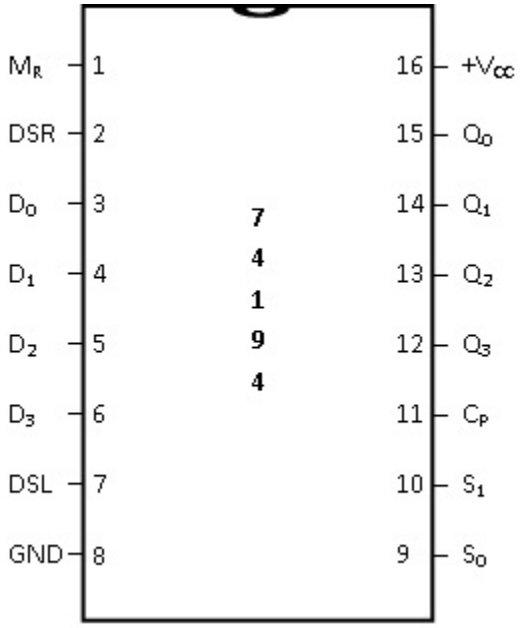
RESULT: verified the working of a updown counter using 74LS192 digital IC.

3. Universal shift Register(74LS194)

AIM : To study the shift right logic, shift left logic, parallel load applications with Universal shift using IC 74194.

APPARATUS: IC 74194, Logic Trainer Board, Connecting wires

PIN DIAGRAM:



PIN DESCRIPTION:

PIN	SYMBOL	DESCRIPTION
1	MR	Asynchronous matter
2	DSR	Serial data input(shift right)
3	D_0	Parallel data input
4	D_1	Parallel data input
5	D_2	Parallel data input
6	D_3	Parallel data input
7	DSL	Serial data input(shift left)
8	GND	Ground
9	S_0	Mode control input
10	S_1	Mode control input

11	C_P	Clock input(low, high, edge triggered)
12	Q_3	Parallel output
13	Q_2	Parallel output
14	Q_1	Parallel output
15	Q_0	Parallel output
16	V_{CC}	Supply Voltage

THOERY:

The Integrated Circuit 74194 is a very adaptable shift register. The Shift Register is another type of sequential logic circuit that is used for the storage or transfer of data in the form of binary numbers and then "shifts" the data out once every clock cycle, hence the name shift register. It basically consists of several single bit "D-Type Data Latches", one for each bit (0 or 1) connected together in a serial or daisy-chain arrangement so that the output from one data latch becomes the input of the next latch and so on. Shift Registers are used for data storage or data movement and are used in calculators or computers to store data such as two binary numbers before they are added together, or to convert the data from either a serial to parallel or parallel to serial format.

A Register may operate in any of the modes like SISO, SIPO, PISO, PIPO or bidirectional. If a Register can be operated in all possible ways it is known as Universal Shift register. IC 74194 has a parallel data inputs (D_0 – D_3) and So and S_1 are the Control inputs. When S_0 and S_1 are High then data appearing at D_0 - D_3 input is transferred to the Q_0 – Q_3 outputs, respectively, following the next LOW to High Transition of the clock. Shift right is accomplished by setting S_1S_0= 01, and serial data is entered at the shift right serial input D_{SR}. Shift Left is Accomplished by setting S_1S_0 = 10 and serial data is entered at the Shift left serial input D_{SL}.

TRUTH TABLE:

INPUTS								OUTPUTS			
OPERATION MODE	C_P	M_R	S_1	S_0	DSR	DSL	D_n	Q_0	Q_1	Q_2	Q_3
RESET	X	0	X	X	X	X	X	0	0	0	0
SHIFT LEFT		before clock →						Q_0	Q_1	Q_2	Q_3
	↑	1	1	0	X	1	X	Q_1	Q_2	Q_3	1
		1	1	0	X	0	X	Q_1	Q_2	Q_3	0
SHIFT RIGHT		before clock →						Q_0	Q_1	Q_2	Q_3
	↑	1	0	1	1	X	X	1	Q_0	Q_1	Q_2
		1	0	1	0	X	X	0	Q_0	Q_1	Q_2
PARALLEL LOAD	↑	1	1	1	X	X	D_n	D_0	D_1	D_2	D_3
HOLD	X	1	0	0	X	X	X	Q_0	Q_1	Q_2	Q_3

PROCEDURE:

1. Reset all outputs by making MR=0.
2. SHIFT LEFT REGISTERS: Made MR=1 and s1s0=10. Applied DSL=1 and observed Q0,Q1,Q2,Q3 for 4 clock pulses. Then made DSL=0 and observed Q0,Q1,Q2,Q3 for 4 clock pulses.
3. SHIFT RIGHT REGISTERS: Made MR=1 and s1s0=01. Applied DSR=1 and observed Q0,Q1,Q2,Q3 for 4 clock pulses. Then made DSR=0 and observed Q0,Q1,Q2,Q3 for 4 clock pulses
4. PARALLEL LOAD: Made MR=1 and s1s0=11 to transfer the data parallel to output at the clock positive transition change the input data and observed the change at the output
5. HOLD: Made MR=1 and s1s0=00 then the shifting operation is ceased and output would show previous one.

RESULT: Verified the operations of Universal shift register using IC 74194.

Viva Voice : 1. What is a shift register?

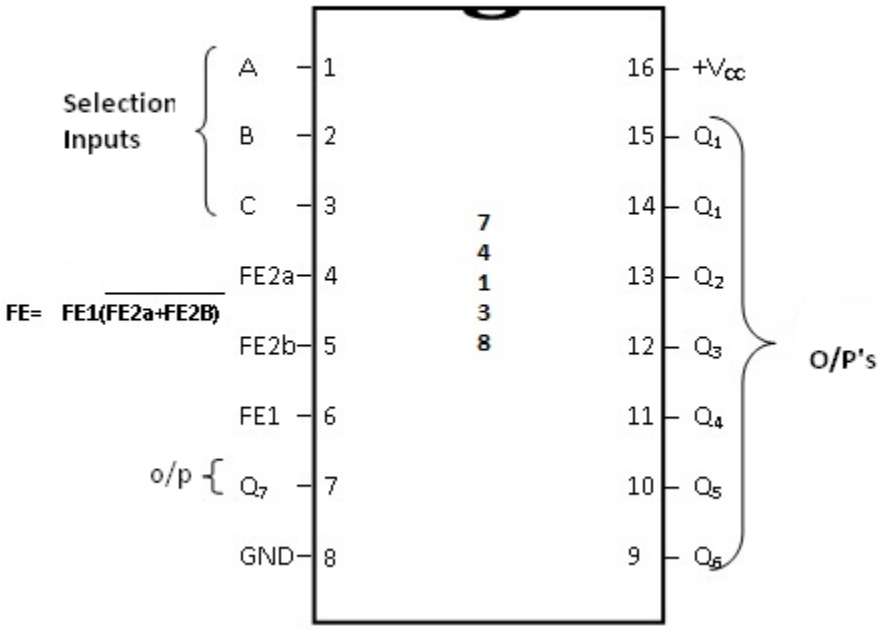
2. Write some applications of shift register?

4. 3-8 Decoder using (74LS138)

AIM : To verify the working of a 3-8decoder using digital IC – 74138.

APPARATUS: IC 74138, Breadboard Trainer System, Connecting Wires.

PIN DIAGRAM:



THEORY:

High-performance memory-decoding or data-routing applications require very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

PROCEDURE:

1. Wired the decoder as shown in diagram.
2. Kept the enable pins - 4 and 5 at active low and enabled pin -6 at active high.
3. Connected the pins – 1,2 and 3 to the logical input switches.
4. Connected the pins- 7, 9, 10, 11,12,13,14 and 15 to the output LED indicators.
5. VCC =5V and GND is provided on the trainer itself.
6. Now switched ON the trainer and verified the function table.

FUNCTION TABLE:

S.NO	INPUTS						OUT PUTS							
	FE2a	FE2b	FE1	A	B	C	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
1	H	X	X	X	X	X	H	H	H	H	H	H	H	H
2	X	H	X	X	X	X	H	H	H	H	H	H	H	H
3	X	X	L	X	X	X	H	H	H	H	H	H	H	H
4	L	L	H	L	L	L	L	H	H	H	H	H	H	H
5	L	L	H	H	L	L	H	L	H	H	H	H	H	H
6	L	L	H	L	H	L	H	H	L	H	H	H	H	H
7	L	L	H	H	H	L	H	H	H	L	H	H	H	H
8	L	L	H	L	L	H	H	H	H	H	L	H	H	H
9	L	L	H	H	L	H	H	H	H	H	H	L	H	H
10	L	L	H	L	H	H	H	H	H	H	H	H	L	H
11	L	L	H	H	H	H	H	H	H	H	H	H	H	L

RESULT: Verified the working of a 3-8decoder using digital IC – 74138.

VIVA VOICE :

1. How many decoders are needed to construct 4X16 Decoder?

2. What is the difference between decoder and Encoder?

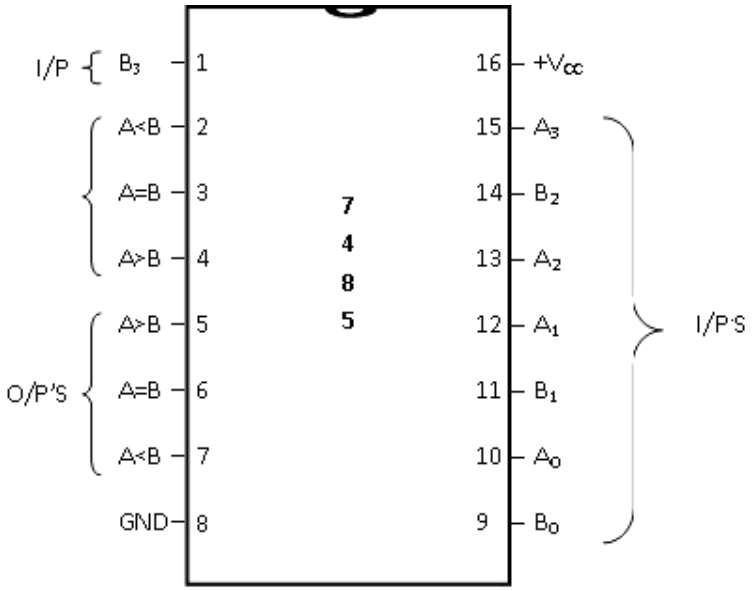
3. Applications of a Decoder ?

5. 4 – bit comparator (74LS85)

AIM **:** To verify the working of a 4 – bit comparator using digital IC 7485.

APPARATUS: IC 7485 – 1 no, Digital Trainer kit, Connecting Wires

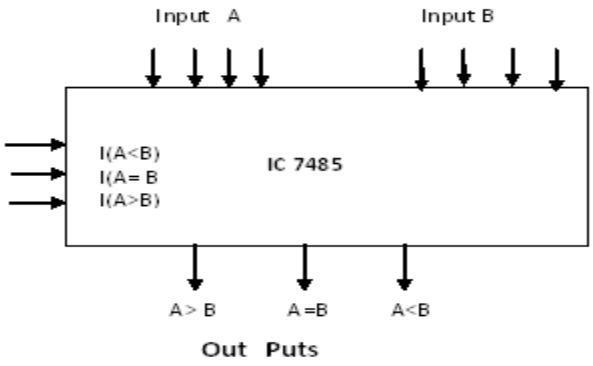
PIN DIAGRAM:



THEORY:

These 4-bit magnitude comparators perform comparison of straight binary or BCD codes. Three fully-decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. Words of greater length may be compared by connecting comparators in cascade. The A<B, A>B, and A=B outputs of a stage handling less-significant bits are connected to the corresponding inputs of the next stage handling more-significant bits. The stage handling the least-significant bits must have a high-level voltage applied to the A , B input. The cascading paths are implemented with only a two-gate-level delay to reduce overall comparison times for long word.

FUNCTIONAL DIAGRAM:



PROCEDURE:

1. Let the input words to the comparator be "A3, A2, A1, A0" and "B3, B2, B1, B0"
2. For various combinations of these two words, checked if A>B, A<B or A=B.
3. Tabulated the result.

TRUTH TABLE:

INPUTS				OUTPUTS		
A3>B3	**X**	**X**	**X**	**H**	**L**	**L**
A3<B3	**X**	**X**	**X**	**L**	**H**	**L**
A3=B3	**A2>B2**	**X**	**X**	**H**	**L**	**L**
A3=B3	**A2<B2**	**X**	**X**	**L**	**H**	**L**
A3=B3	**A2=B2**	**A1>B1**	**X**	**H**	**L**	**L**
A3=B3	**A2=B2**	**A1<B1**	**X**	**L**	**H**	**L**
A3=B3	**A2=B2**	**A1=B1**	**A0>B0**	**H**	**L**	**L**
A3=B3	**A2=B2**	**A1=B1**	**A0<B0**	**L**	**H**	**L**
A3=B3	**A2=B2**	**A1=B1**	**A0=B0**	**L**	**L**	**H**

RESULT:. Verified the working of a 4 – bit comparator using digital IC 7485.

VIVA VOICE :

1. How many 4-bit comparators are needed to construct 12-bit comparator?

2. What does a digital comparator mean?

3. Design a 2-bit comparator using gates?

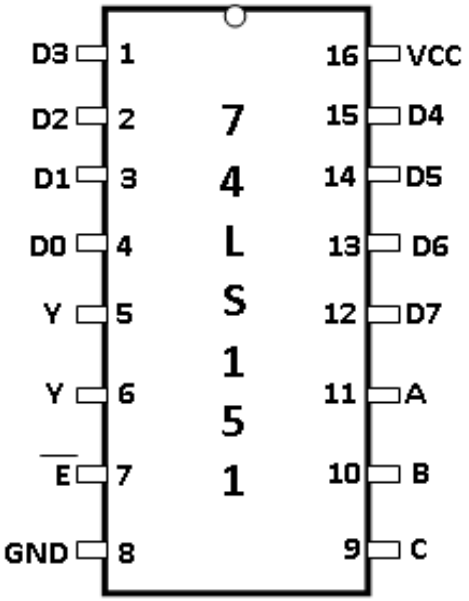
6. 8x1 Multiplexer - 74LS151 and 2x1 Multiplexer-74LS155

(a) 8X1 MULTIPLEXER USING 74151

AIM **:** To verify the working of a 8x1 multiplexer using IC 74151

APPARATUS: IC 7415 1 – 1 no, Digital Trainer Kit, Connecting wires

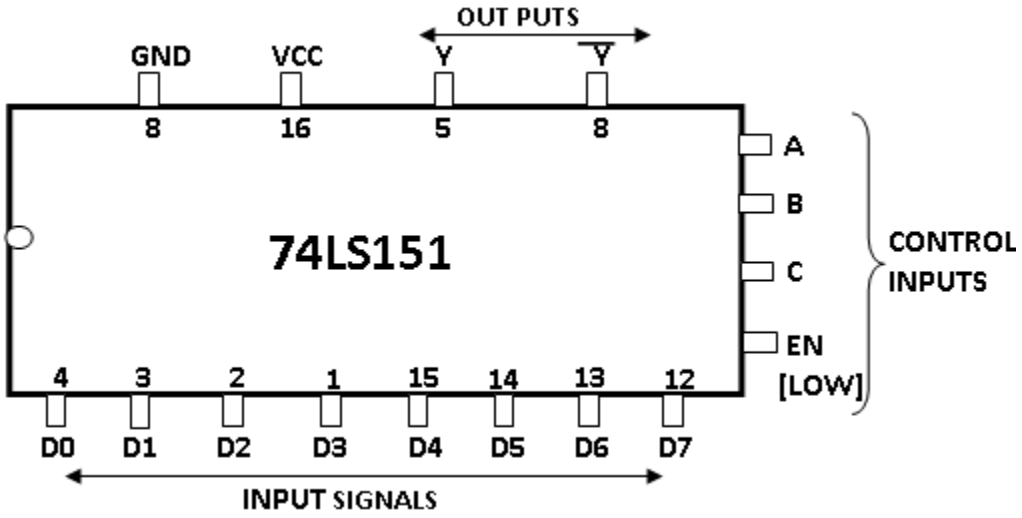
PIN DIAGRAM:



THEORY:

The 74LS151 is a high speed 8-input Digital Multiplexer. It provides, in one package, the ability to select one bit of data from up to eight sources. The 74LS151 can be used as a universal function generator to generate any logic function of four variables. Both assertion and negation outputs are provided. The 74151 can also function as a 1-8 line selector. The 74LS151 provides the ability, in one package, to select from eight sources of data or control information. By proper manipulation of the inputs, the LS151 can provide any logic function of four variables and its negation.

FUNCTIONAL DIAGRAM:



PROCEDURE:

1. Eo,E1,……E7 are the inputs the MUX,A,B,C are selected inputs and Q is the output.
2. For an input data word, checked the output for various combinations of selected inputs.
3. Tabulated the results.

FUNCTION TABLE:

S.NO	INPUTS												OUTPUTS	
	E	C	B	A	D0	D1	D2	D3	D4	D5	D6	D7	$\overline{Y}$	Y
1	H	X	X	X	X	X	X	X	X	X	X	X	H	L
2	L	L	L	L	L	X	X	X	X	X	X	X	D'_0	D_0
3	L	L	L	L	H	X	X	X	X	X	X	X		
4	L	L	L	H	X	L	X	X	X	X	X	X	D'_1	D_1
5	L	L	L	H	X	H	X	X	X	X	X	X		
6	L	L	H	L	X	X	L	X	X	X	X	X	D'_2	D_2
7	L	L	H	L	X	X	H	X	X	X	X	X		
8	L	L	H	H	X	X	X	L	X	X	X	X	D'_3	D_3
9	L	L	H	H	X	X	X	H	X	X	X	X		
10	L	H	L	L	X	X	X	X	L	X	X	X	D'_4	D_4
11	L	H	L	L	X	X	X	X	H	X	X	X		
12	L	H	L	H	X	X	X	X	X	L	X	X	D'_5	D_5
13	L	H	L	H	X	X	X	X	X	H	X	X		
14	L	H	H	L	X	X	X	X	X	X	L	X	D'_6	D_6
15	L	H	H	L	X	X	X	X	X	X	H	X		
16	L	H	H	H	X	X	X	X	X	X	X	L	D'_7	D_7
17	L	H	H	H	X	X	X	X	X	X	X	H		

RESULT: Verified the working of a 8x1 multiplexer using IC 74151.

VIVA VOICE:

1. What is meant by multiplexer?

2. What does demultiplexer mean?

3. How many 8X1 multiplexers are needed to construct 16X1 multiplexer?

4 . Compare decoder with demultiplexer?

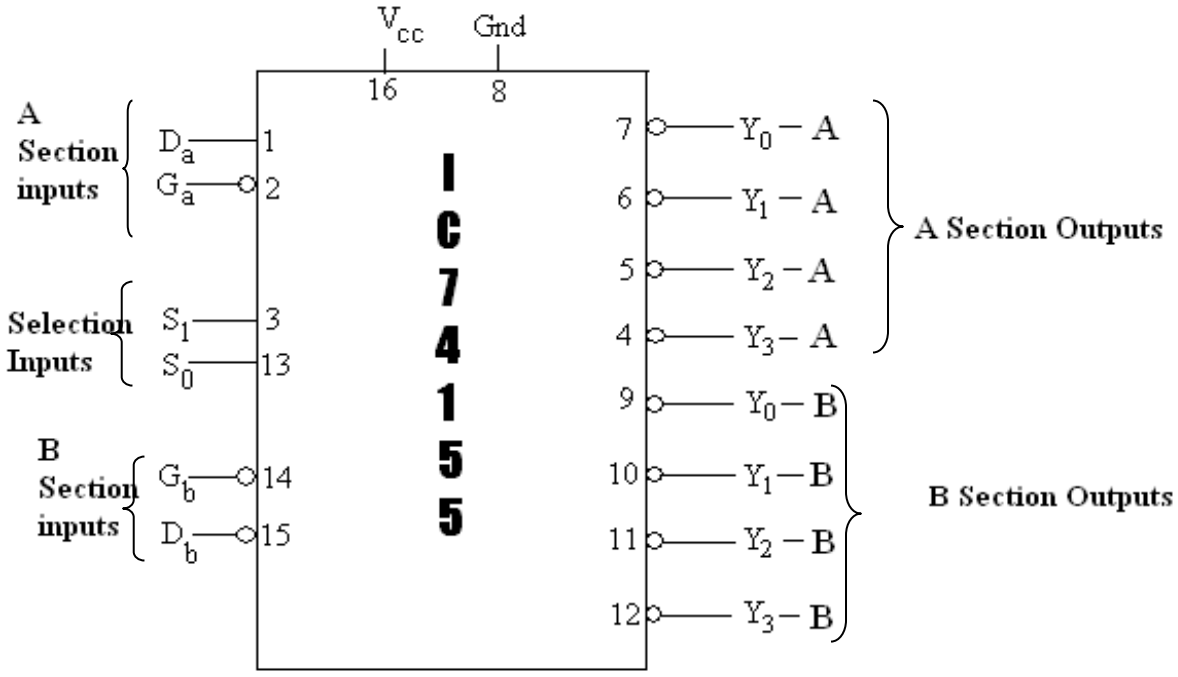
5. Design a full adder using 8X1 multiplexer?

(b) 2 X4 DEMULTIPLEXER

Aim **:** To verify the Functionality of 2X4 Demultiplexer using IC 74155.

Apparatus: IC Trainer, IC 74155, Patch cards.

Functional Diagram :



Theory **:**

Demultiplexer (Demux) takes single i/p & distributes it over several o/ps. It has one data line, n o/p lines & m select lines where $2^m = n$. MSI ICs available in TTL family for demux are 74138(3 line to 8 line Decoder/Demux.), 74139(dual 2 to 4 line Decoder/ Driver) , 74154(4 to 16 line Decoder/Demux), 74155(dual 2 to 4 line Decoder) etc. IC 74155 is a dual 2 to 4 line Decoder.

IC 74155 has two Sections A and B With independent Data (D) inputs, Strobe (G) inputs and Data (Y3, Y2, Y1, Y0) outputs. Both the Section shares a common set of select inputs S1 and S0 and therefore are selected in parallel. Section A has an active high data input (Da) and Section B has an active low data input (Db). The function tables for sections A and B are given in tables A, B.

Two sets of active low outputs are 1Y0 to 1Y3 & 2Y0 to 2Y3. A & B are the select terminals common for both the demux. C1, C2 & G1, G2 are the data lines & Strobe (enable) inputs for the two Demuxes. C1 is active high, C2, G1, G2 are active low. The two 2 line to 4 line demux. Can be combined to implement 3 lines to 8 line demux.

Function table for section A

Inputs				outputs			
S1	S0	Ga	Da	Y0-A	Y1-A	Y2-A	Y3-A
x	x	1	x	1	1	1	1
x	x	x	0	1	1	1	1
0	0	0	1	0	1	1	1
0	1	0	1	1	0	1	1
1	0	0	1	1	1	0	1
1	1	0	1	1	1	1	0

Function table for section B

Inputs				outputs			
S1	S0	Gb	Db	Y0-b	Y1-b	Y2-b	Y3-b
x	x	1	x	1	1	1	1
x	x	x	0	1	1	1	1
0	0	0	1	0	1	1	1
0	1	0	1	1	0	1	1
1	0	0	1	1	1	0	1
1	1	0	1	1	1	1	0

PROCEDURE:

(1) Made the connections as shown in figure using the pin details of the IC used.
(2) Set up the circuit of a 2 line to 4 line decoder as follows.
(3) Connected Ga to logic 0 and Da to logic 1.
(4) Applied 00 through 11 at select inputs S1 and S0 and observed the outputs of the section A and verified that the ckt functions as 2 line to 4 line decoder..
(5) Similarly section B also can be used as 2 to 4 decoder.

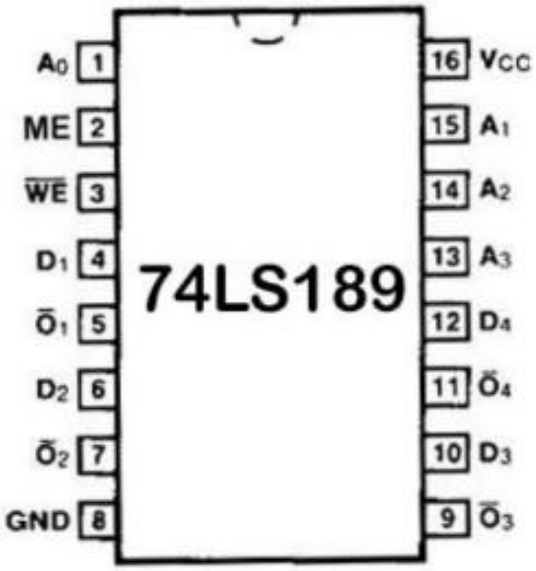
RESULT: Verified the Functionality of 2X4 Demultiplexer using IC 74155.

7. RAM 16X4 – 74189 (read and write operation)

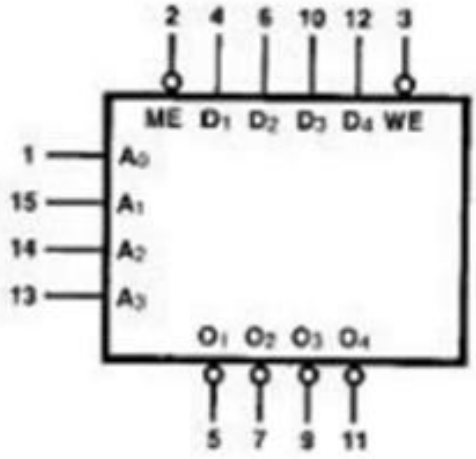
Aim : To verify the operation of (16X4) RAM using IC 74189 (Read and Write operations).

Apparatus: Breead board IC Trainer kit, IC 74189, Patch cards and connecting wires.

Pin Diagram :



Logic symbol :



VCC = Pin 16
GND = Pin 8

Function table:

Memory enable	Write enable	operation
H	X	All data outputs are high
L	H	Read mode
L	L	Write mode

Theory:

The 74LS189 is a high speed 64 bit RAM organized as a 16 word by 4 bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs of 3 states and in the high impedance state whenever the memory enable input is high. The outputs are active only in the read mode and the output data is the complement of the stored data. Here A0-A3 are the address inputs.D1-D4 are the data inputs.O1-O4 are the inverted data outputs.

Procedure:

1. The memory enable pin is used to select one of n ICs that is like a chip select signal.
2. The address lines are given through an up-down counter with preset capability.
3. The address and data bits are used to set an address and enter the data.
4. The read/write switch is used to write data on the RAM.

a) <u>Clearing the memory</u>

The RAM 74189 is a volatile memory. It does not come with a "clear memory" signal. The memory has to be clear manually.

1. Position the stack/queue switch in the queue position.
2. Position the set address switch in the "1" position.
3. Set the address bits to 0h (first byte in the memory)
4. Position the set address switch in the "0" position to disable random access and enable the counter.
5. Position the' Read/Write 'switch in the' Write' position to write data on to the memory.
6. Set the data bits to 0h (clearing the content).
7. Observe that the LEDs (D3 to D0) glow. This is to indicate that the content is 0h. Refer the truth table above and observe that the data outputs of the RAM will be compliments of the data inputs.
8. Position the 'Increment/Decrement 'switch in the 'Increment' position.
9. Press the 'Clock' to increment the counter to the next address. As the 'Read /Write ' switch is already in the 'Write' position, and the data bits are set to the 0h, the content in the new location is also replaced with 0h.

b) Write operation

1. Assume that the following data has to be written on to the RAM. The address and data are given in the hexadecimal format.

Address	Data
0h - 0000	Ah - 1010
1h - 0001	Bh - 1011
2h - 0010	4h - 0100
3h - 0011	7h - 0111
4h - 0100	Ch - 1100
5h - 0101	1h - 0001
6h - 0110	Fh - 1111
7h - 0111	5h - 0101
8h - 1000	8h - 1000
9h - 1001	3h - 0011
10h - 1010	Eh - 1110
11h - 1011	9h - 1001
12h - 1100	Dh - 1101
13h - 1101	0h - 0000
14h - 1110	2h - 0010
15h - 1111	6h - 0110

2. Position the 'Stack/Queue' switch in the 'Queue' position.
3. Position the' Read/Write 'switch in the' Write' position to enable the entry of data to the RAM.
4. Position the set address switch in the "1" position to allow the RAM.
5. Set the desired address (any address at random) using the address bit switches.
6. Set the desired data (refer table for the data to be entered in each location) using the data bit switches.
7. Observe that the data is indicated by the LEDs (D3 toD0). This is because the data is written on to the RAM.
8. Also observe that the data is indicated by the data outputs is the compliment of the data input (refer truth table condition ME =L and WE=L).
9. After each data entry, make a note of the location where data is entered. This is to make sure that we are not re –entering data in the same location.
10. Repeat steps 4 and 5 until data has been entered in all the addresses listed in the above table
11. Position the' Read/Write 'switch in the' Read' position, to disable data entry.
12. This completes data entry.

c) Read operation

1. Position the 'Stack/Queue' switch in the 'Queue' position.
2. Position the 'Set Address' switch in the '0' position to allow random access of memory.
3. Position Read/Write 'switches in the' Read' position, to disable unauthorized entry of data.
4. Set the desired address (any address at random).
5. Observe that the data entered in the location is indicated by the LEDs (D3 toD0). This is because the data was written during the data entry procedure.
5. Also observe that the data indicated by the data out puts is the compliment of the data input (refer truth table condition ME=L and WE=H).

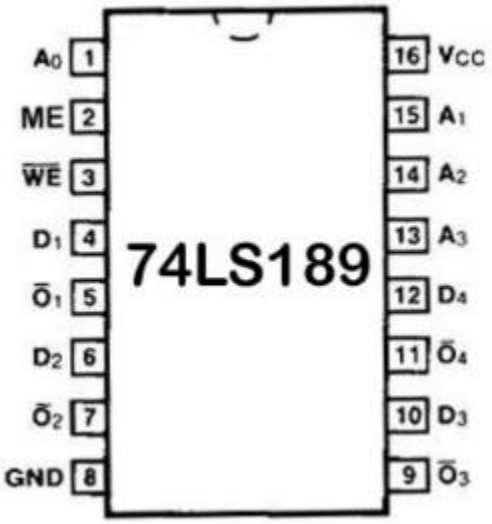
Result: The operation of the RAM IC 74LS189 has been verified.

8. Stack and queue implementation using RAM, 74189

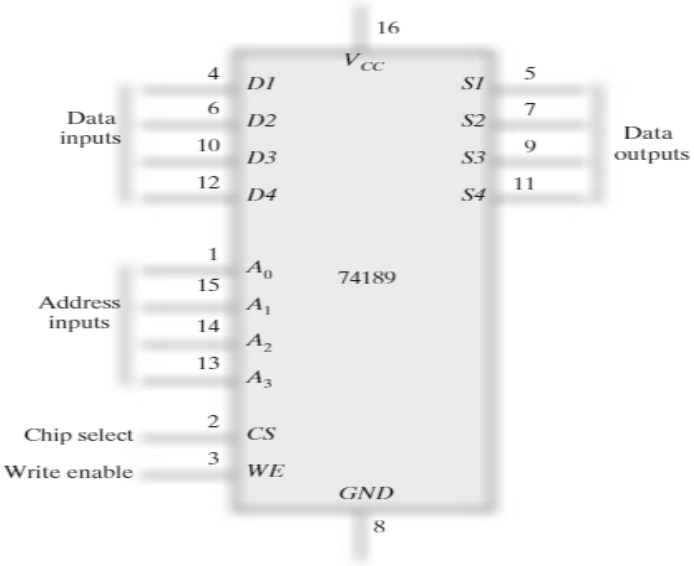
Aim: To verify the Stack and queue operation of RAM IC 74189.

Apparatus: Breead board IC Trainer kit, IC 74189, Patch cards and connecting wires.

Pin diagram:



Logic symbol



Theory:

The 74LS189 is a high speed 64 bit RAM organized as a 16 word by 4 bit array. Address inputs are buffered to minimize loading and are fully decoded on chip. The outputs of 3 states and in the high impedance state whenever the memory enable input is high. The outputs are

active only in the read mode and the output data is the complement of the stored data. Here A0-A3 are the address inputs.D1-D4 are the data inputs.O1-O4 are the inverted data outputs.

Procedure:

a) Stacking operation (LIFO)

1. Position the 'Stack/Queue' switch in the 'Stack' position.
2. Position the' Read/Write 'switch in the' Write' position to enable the entry of data to the RAM.
3. Position the set address switch in the "1" position to allow the RAM.
4. Set the desired address (any address at random) using the address bit switches.
5. Set the desired data using the data bit switches.
6. Observe that the data is indicated by the LEDs (D3 toD0). This is because the data is written on to the RAM.
7. Also observe that the data is indicated by the data outputs is the compliment of the data input (refer truth table condition ME =L and WE=L).
8. After each data entry, make a note of the location where data is entered. This is to make sure that we are not re –entering data in the same location.
9. Repeat steps 4 and 5 until data has been entered in all the addresses.
10. Position the' Read/Write 'switch in the' Read' position, to disable data entry.
11. Position Read/Write 'switches in the' Read' position. The data comes in "last in first out order".

b) Queuing operation (FIFO)

1. Position the 'Stack/Queue' switch in the 'Queue' position.
2. Position the' Read/Write 'switch in the' Write' position to enable the entry of data to the RAM.
3. Position the set address switch in the "1" position to allow the RAM.
4. Set the desired address (any address at random) using the address bit switches.
5. Set the desired data using the data bit switches.
6. Observe that the data is indicated by the LEDs (D3 toD0). This is because the data is written on to the RAM.
7. Also observe that the data is indicated by the data outputs is the compliment of the data input (refer truth table condition ME =L and WE=L).
8. After each data entry, make a note of the location where data is entered. This is to make sure that we are not re –entering data in the same location.
9. Repeat steps 4 and 5 until data has been entered in all the addresses.
10. Position the' Read/Write 'switch in the' Read' position, to disable data entry.
11. Position Read/Write 'switches in the' Read' position. The data comes in "first in first out order".

Result: The Stack and queue operation of the RAM IC 74LS189 has been verified.