LDICA [Linear and Digital Integrated circuit Applications].

Module 1 : Integrated circuits and operational Amplifiers

* Integrated circuit [IC] :- Integrated circuit where all components like active and passive components are fabricated on a single chip of silicon (Si).
* All the active elements like transistor and diode and passive elements like Resistor, Inductor, capacitor are fabricated on a single piece of semiconductor material (Si).
* Advantages of Ic Technology :-
  - Miniaturization and (or) small in size. and hence increase the equipment density.
  - Low cost due to batch processing.
  - Improved system reliability due to the elimination of soldered joints.
  - Better functional performance.
  - Matched devices.
  - Increased operating speeds.
  - Low power consumption.
  - Low supply voltages.
  - Less weight [weight of Ic much less compared to descrete circuit consisting of same number of components.

* classifications of ICs :-

Integrated circuits offer a wide range of applications and are broadly classified as.

- Linear ICs
- Digital ICs

- Linear ICs :- Linear ICs accepts analog input and delivers analog output.
- The relationship between the input and output of a circuit is linear.

Ex :- operational amplifier [op-amp].
- Timer IC 555
- Phase locked loop IC 565.
- voltage Regulator IC 723.
- Waveform generator IC [8038].

* Digital ICs :- The circuit is either in on-state or off-state and not in between the two.
- Digital ICs accepts input in two discrete voltages levels : logic 0 (zero) or logic 1 [+5V]. The output is also discrete in two specific voltage levels only. i.e zero (0) & one (1).
- Hence noise immunity is better in digital circuits compared to analog circuits.

Ex :- Logic gates 7400, 7404
Multiplexers
Microprocessor 8085, 8086, 80486.

- Based on technology used, ICs are classified as.
  (i) Monolithic IC's
  (ii) Thin and Thick film IC's.
  (iii) Hybrid ICs.
- Monolithic IC's:-

The word monolithic comes from the Greek word 'monos' and 'lithos' which means 'single' and 'stone'.

- The monolithic IC's refer to a single stone or a single crystal.
- The single crystal refers to a single silicon ~~chi~~chip as the semiconductor material on top of which all the passive and active components are interconnected.
- Monolithic ICs are considered as the best mode of Manufacturing ICs as:
  1. It can be made identical.
  2. High reliability.
  3. Manufactured in bulk in very less time
  4. Low cost.

* Limitations:

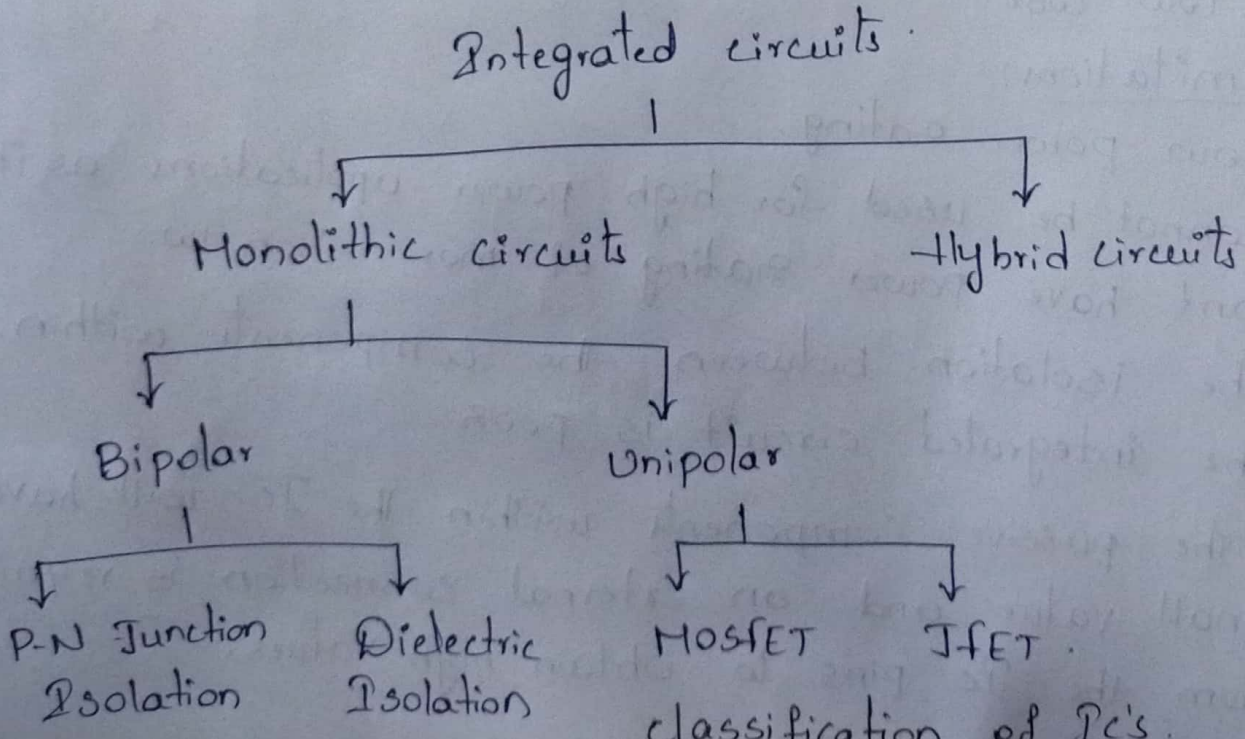
- Low power rating.
- Cannot be used for high power applications as it can't have power rating of more than 1W.
- The isolation between the components within the integrated circuit is poor.
- The passive components within the IC will have small value and an external connection is required from the IC pins to obtain high values.

* Thin and Thick film Ic :-

- These Ics are larger than monolithic Ic's and smaller than discrete ckts.
- It can be used in high power applications.
- Diodes and transistors if required can be externally connected on to its corresponding pins.

* Hybrid Ic's :-

- The circuit is fabricated by interconnecting a number of individual chips.
- Used for high power audio amplifier applications.
- In Hybrid Ics separate components are attached to ceramic substrate and interconnected by means of either metallization pattern or wire bonds. This technology is adaplable to small quantity custom circuits.
- Based on active devices used Monolithic Ic's are further classified as bipolar Ic's and unipolar Ic's.



classification of Ic's.

* Ic chip size and circuit complexity :-

* The invention of the transistor in 1947 by william B. Shockley, Watter H. brattain and John Bardeen of Bell laboratiies was followed by invention of Ic.
* The concept of Ic was introduced at beginning of 1960 by with Texas Instruments and fairchild semiconductors.
* The first Integrated circuit has only a few devices, Perhaps as many as ten diodes, transistors, Resistors and capacitors making it possible to fabricate one or more logic gates on a single chip.
* As an increasing the number of components los transistor Per integrated circuit the technology was developed as

• Invention of Transistor (Ge)		1947
• Development of silicon transistor		1955-1959
• Silicon planar Technology	Junction transistor diode	1959
• first Ics, small scale Integration [SSI]	3 to 30 gates/chip approx. or 100 transistors/chip [logic gates, flip-flops]	1960-1965
• Medium scale Integration [MSI]	30 to 300 gates/chip or 100 to 1000 transistor/chip (Counters, Multiplexers, Adders]	1965-1970.
• Large scale Integration [LSI]	300 to 3000 gates/chip or 1000-20,000 transistors/chip [8 bit microprocessors, ROM, RAM]	1970-1980

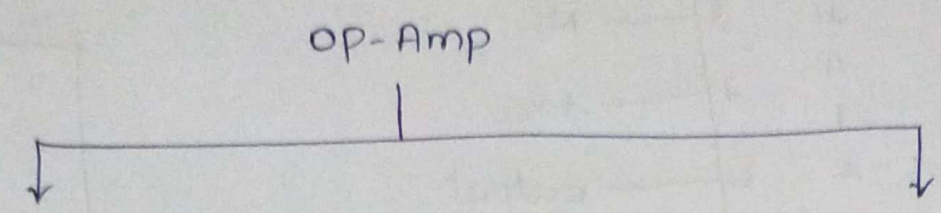
• Very Large Scale Integration [VLSI]	More than 3000 gates/chip or 20,000 - 1,00,00,00 transistors/chip (16 and 32 bit microprocessors)	1980 - 1990
• Ultra large scale Integration (ULSI]	10^6 - 10^7 transistors/chip [special processors, virtual reality) machines, smart sensors	1990 - 2000
• Giant-scale Integration [GSI]	$>10^7$ transistors/chip. Embedded systems, systems on chip.	

* Linear integrated circuits are being used in a number of electronic applications such as fields like audio, Radio communication, medical electronics, etc.
* An important linear IC is operational amplifier.
* operational Amplifier :- [Abbreviated as op-Amp].

operational Amplifiers used to perform several applications like adder, subtractor, ~~multip~~ differentiator and integrator.

• op-Amp is a directly coupled high gain IC amplifier with two high impedance input terminals and one low output impedance. The op-amp consists of a differential amplifier input stage and an Emitter follower output stage.
• An operational amplifier available as a single integrated circuit package.
• It can be used to amplify dc as well as ac input signals and was originally designed for computing such as operational or mathematical operations like addition, subtraction, Multiplication, differentation and integration.

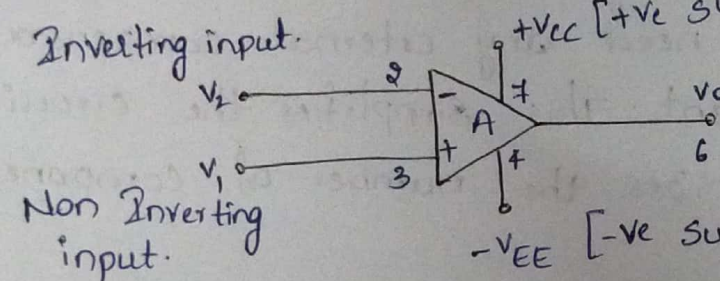
• With the addition of suitable external feedback components the op-amp can be used for a variety of applications such as ac and dc signal amplifications, active filters, oscillators, comparators, regulators etc.



General purpose op-Amps
• They can be used for a variety of applications such as
1. Integrator 2. Differentiator
3. Summing Amp and others
Ex: Widely used general purpose op-amp is 741.

Special purpose op-amps.
• They are used only for the specific applications
Ex: LM 380 op-Amp is used only for audio power applications.

* Schematic symbol of IC 741:-



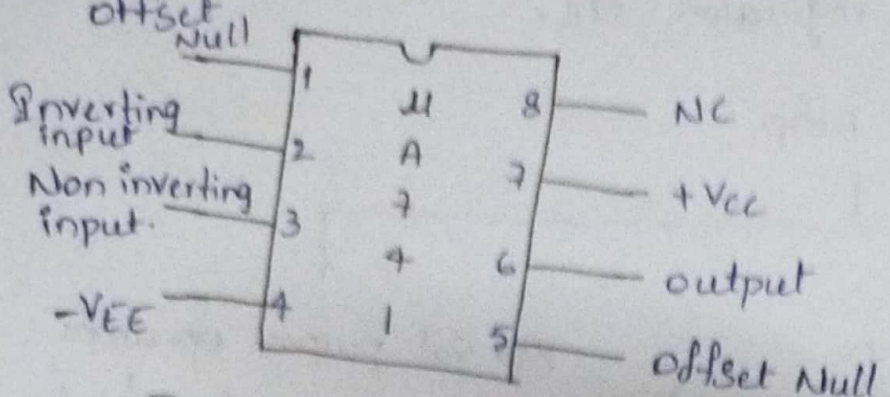
* The positive input is the non-inverting input. An ac signal [(or) dc voltage] applied to this input produces an inphase [or same polarity] signal at the output.
* The negative input is the inverting input. An ac signal [or dc voltage] applied to this input produces out-of-phase [or opposite polarity] signal at the output.

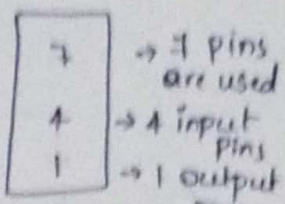
V_1 - Voltage at the non inverting Input [volts]
V_2 - Voltage at the Inverting Input [volts]

V_o - output voltage [volts]

A - large signal voltage gain

* PIN Diagram of IC 741





* Features of 741 op-Amp :-

- Short circuit and overload protection provided.
- large common mode rejection ratio [CMMR] and differential voltage ranges.
  Ideally CMMR is infinity
- No external frequency compensation is required. It also does not need any external compensation for phase component. This simplifies the circuit design and minimizes the number of components used.
- offset voltage null capability.
- No latch-up problem
- low power consumption.

* Identification code :-

1. fairchild - μA, μAf
2. National semiconductor - LM, Lf, IH
3. Motorola - MC

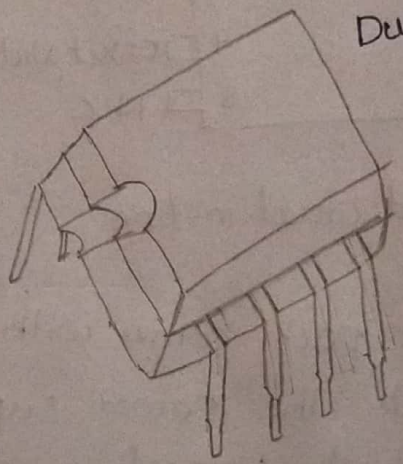
4. NE/SE, N/S - Signetics
5. Burr - Brown - BB
6. Texas Instruments - TI
7. RCA - CA, CD
8. Intersil - ICA.

* Packages :-

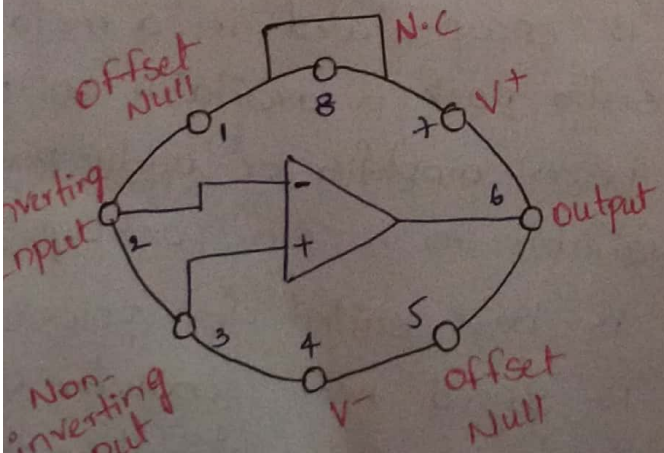
. There are three popular packages available.
* Metal can (TO) package.
* Dual-in-line package [DIP].
* Flat package. [Ceramic]

. The op-amp packages may consists of single, two [dual] and four [Quard] op-Amps. Typically packages have 8 terminals [DIP] (or) 10 terminals [flat packs] and 14 terminals [DIP]

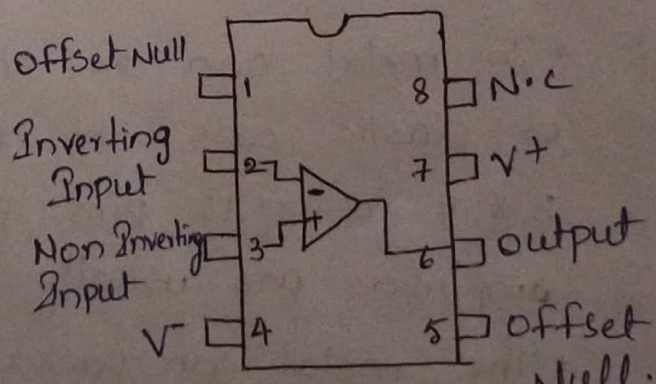
TO-5-style package
Tab locates Pin 8



Dual-in line plastic package

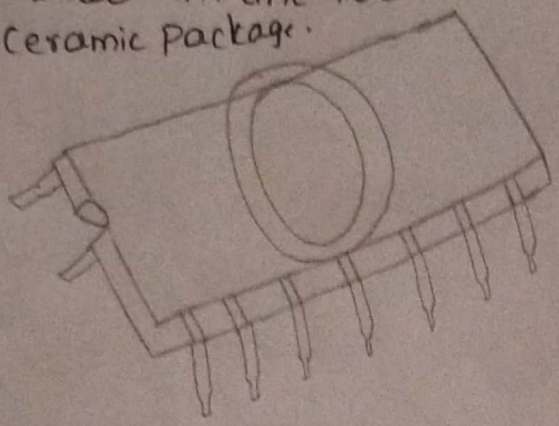


(a) 8-pin Metal can.

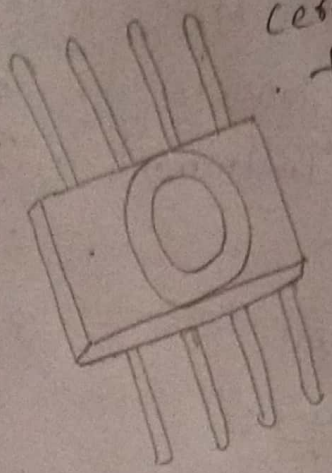


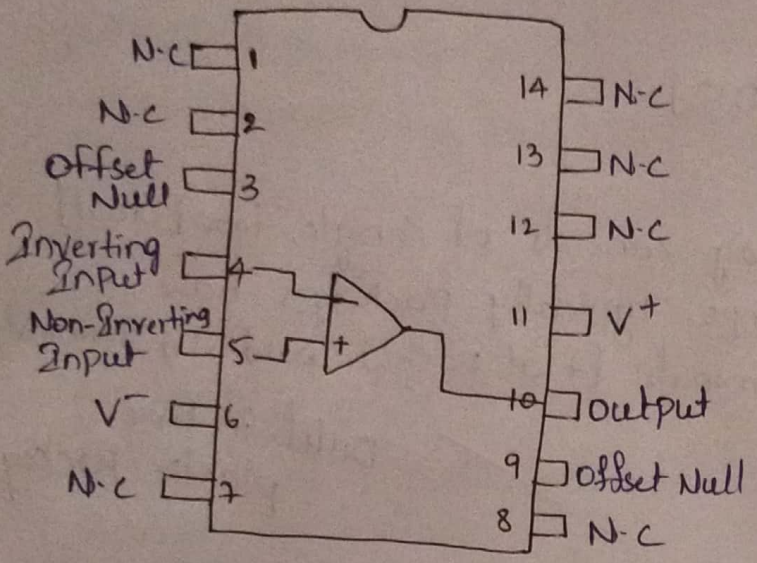
(b) 8-Pin Mini DIP.

Dual-in-line Welded-seal ceramic package.

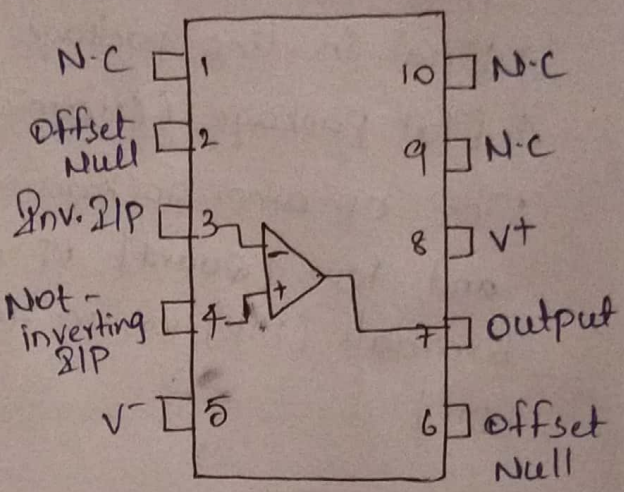


Ceramic flat package.





(c) 14-lead dual-in-line Package



(d) 10-lead flat pack.

* The flat pack comes with 8, 10, 14 or 16 leads. These leads accommatate the power supplies, Inputs, outputs and several special connections required to complete the circuit.

* In metal can the chip is encapsulated in a metal or plastic case the transistor pack is available with 3, 5, 8, 10 (or) 12 pins the power amplifier or audio power amplifiers are usually available in 5-pin package.

* The metal can package is best suited for power Amplifiers because metal is a good heat conductor and consequently has better dissipation capability than the

flat pack or Dual-in-line package. Most of general purpose op-amps come in 8, 10 or 12 pin package.

* In the dual in line package [DIP] the chip is mounted inside a plastic or ceramic case.
* The DIP is most widely used package type because it can be mounted easily. The 8-pin DIP packages are referred to as mini DIPS. DIPS are also available with 12, 14, 16 and 20 pins.
* As the density of components Integrated on the same chip increases the number of pins also goes up.
* In flat pack the chip is enclosed in a rectangular ceramic case with terminal leads extending through the sides and ends.
* Temperature Ranges:-

Ic's are manufactured in three standard temperature ranges.

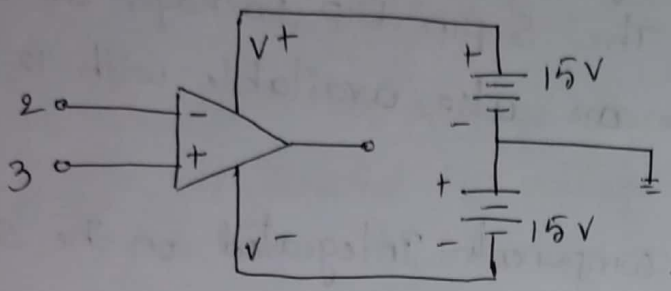
C	: commerial	0°c to 70°c
I	: Industrial	-25°c to +85°c
M	: Military	-55°c to +125°c.

* The very commonly used general purpose op-Amp is Ic 741.
* Power Supply Connections:-

The v^+ and v^- power supply terminals are connected to two dc voltage sources.

* The v^+ pin connected to positive terminal of one source of v^- pin connected to negative terminal of other source where two source are 15v batteries each.

* The power supply voltage ranges from ± 5V to ± 22V. The common terminal of V+ and V- source connected to ground. otherwise twice the supply voltage gets applied and damage the op-Amp.



* The IC will not function properly if power supply connections are not given.

* Advantage of Op-Amp over transistor Amplifier :-
  - Low Power consumption.
  - Low cost.
  - More compact [IC is small or tiny]
  - More reliable.
  - Higher gain can be obtained.
  - Easy design [If to design inverting amplifier only two resistors will be connected.].

* op-Amp is a very high gain amplifier fabricated on IC.
* Combination of many transistors, FETs, resistors in a pin head space.

* Applications:-
  - Audio Amplifier.
  - Signal Generator.
  - signal filters.
  - Biomedical Instrumentation.

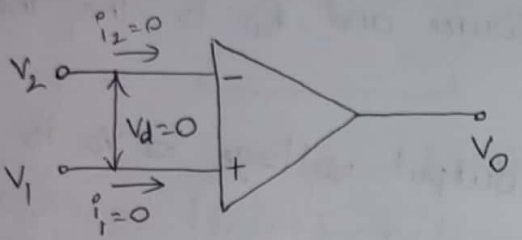
  Etc.

* Ideal Op-Amp :-

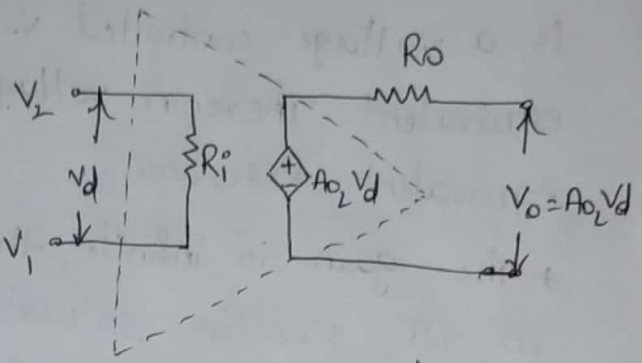
* The Op-Amp has two input terminals and one output terminal.
* The '-' & '+' are the inverting and non inverting input terminals respectively.

$V_1 = 0 \quad V_0 = -V_2$ [out of phase]

$V_2 = 0 \quad V_0 = V_1$ [In phase]



Ideal OP-AMP.



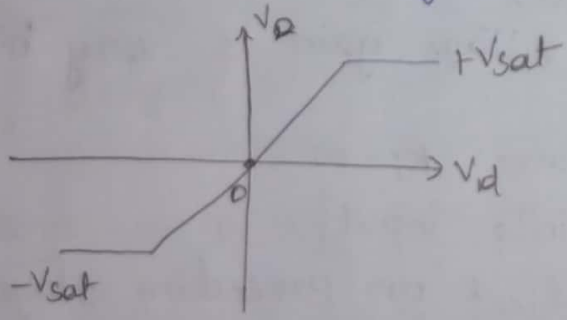
Equivalent circuit of OP-AMP.

* Characteristics of Ideal Op-Amp :-

* open loop voltage gain is infinity $A_{OL} = \infty$.
  open loop due to no feedback and voltage gain is infinite because $V_1 = V_2 = 0$.
* But practically the voltage gain is very high. [i.e 2, 50,000].
* Infinite input impedance $R_i = \infty$.
  - [No current flows into input].
  - To avoid loading effect on preceding stages.
  - But in practical R_i is $10^{12}\Omega$ for FET input Op-Amps.
* Zero output impedance $R_o = 0$.
  [To connect infinite loads]
  - Practically current is maximum.
* The op-amp output will do whatever it can

[within its limitation] to make the voltage difference between the two [$V_d = V_1 - V_2 = 0$] zero.

* Infinite Bandwidth $BW = \infty$ [allows f_{min} to f_{max}]
* Infinite common mode rejection ratio $CMRR = \infty$.
* Infinite slew rate.
* A physical amplifier is not an ideal one. The op-Amp is a voltage controlled voltage source and $A_{OL}V_d$ is an equivalent Thevenin voltage source and R_o is the Thevenin equivalent Resistance.
* The gain is infinite, the output voltage ~~is~~ V_o is either at its positive saturation voltage [$+V_{sat}$] or negative saturation voltage [$-V_{sat}$] as $V_1 > V_2$ or $V_2 > V_1$ resp.
* One of the two possible output states that is $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only.
* This has a limited applications such as voltage comparator, Zero crossing detector etc.



• An ideal op-amp draws no current into both the input terminals i.e $i_1 = i_2 = 0$. Because of infinite input impedance, any signal source can drive it and there is no loading on the preceding driver stage.

* The output voltage is independent of current drawn from the o/p resistance [$R_o = 0$]. Thus op-Amp can drive infinite number of devices.

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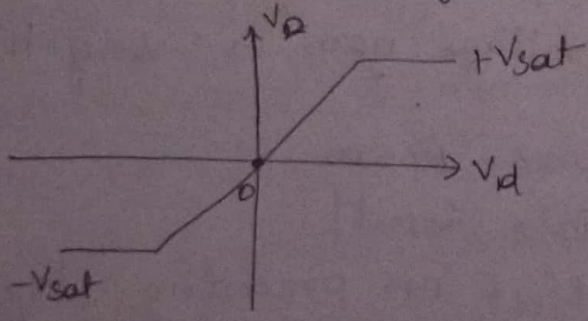

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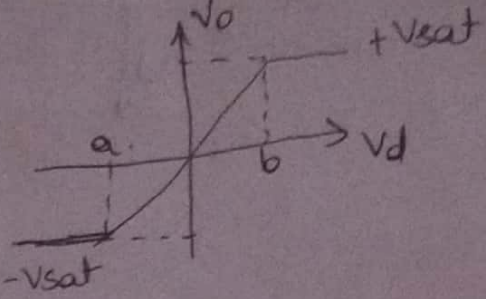
* Practical op-Amp :-

The equivalent ckt of op-Amp comprises of $A V_{id}$ an equivalent Thevenin voltage voltage source and R_o, equivalent thevenin resistance looking into output terminal of op-Amp.



$$V_o = AV_{id} = A[V_1 - V_2]$$

A - open loop voltage gain
V_{id} - differential i/p voltage
V_2 - voltage at inverting i/p terminal
V_1 - voltage at non-inverting i/p terminal.

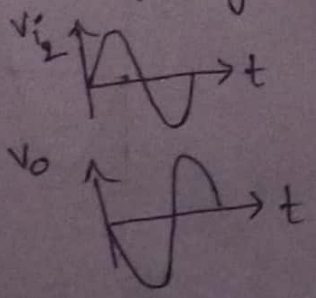
* The o/p voltage V_o is directly proportional to algebraic difference b/w two i/p voltages.
* op-Amp amplifies the difference b/w two i/p voltages.

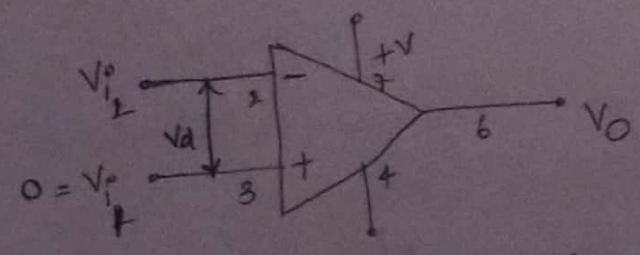
* Open loop Configuration of op-Amp :-

- open loop connection: no direct connection between output and any of the input terminals.

1. Single-Ended input.
2. Double-Ended (differential) input.

* Single-Ended input :- Input voltage is applied one of the input terminals (Inverting or non-Inverting).
* Inverting Mode :- Input is applied to inverting terminal.

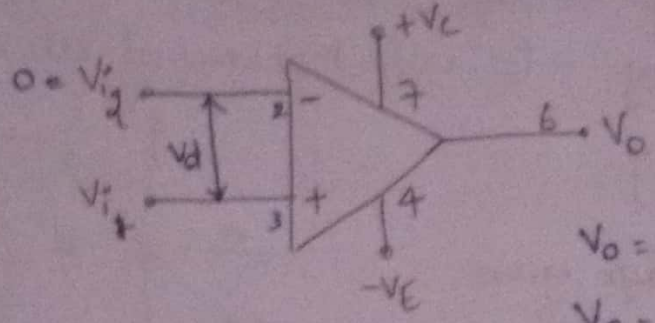


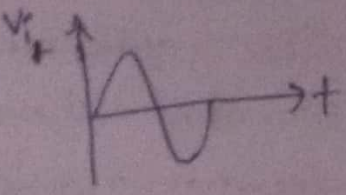


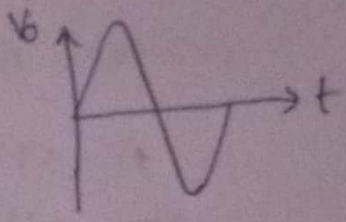
$$V_o = AV_d = A[V_{i_1} - V_{i_2}]$$

$$V_o = A[0 - V_{i_2}] \Rightarrow V_o = -AV_{i_2}$$

* Non-Inverting Mode :- Input is applied to non-Inverting terminal.





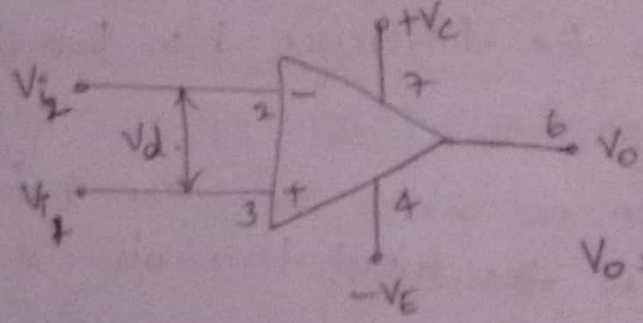


$V_o = AVd$

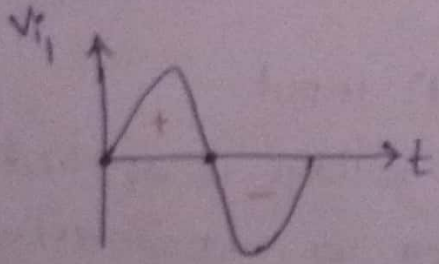
$V_o = A[V_{i_1} - V_{i_2}]$

$V_o = AV_{i_1}$

* Double-Ended or Differential Mode :-
Voltages are applied to both input terminals.



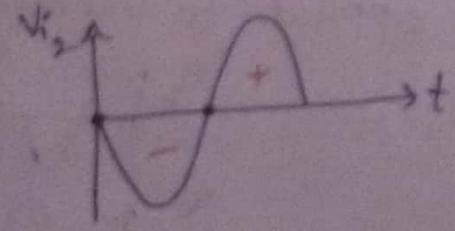
$V_o = AVd = A[V_{i_2} - V_{i_1}]$



(+) - (−)

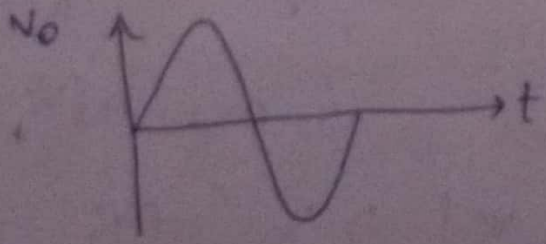
$A[V_{i_2} - V_{i_1}]$

$= +Ve$



$= A[V_{i_2} - V_{i_1}]$

$= -Ve$



* Internal block diagram of Op-Amp :-

* Input stage or differential amplifier stage can amplify difference between two input signals, input resistance is very high. Draws zero current from the input source.
* Intermediate stage uses direct coupling ; provide very high gain
* level shifter stage shifts the dc level of output voltage to zero [can be adjusted manually using two additional terminals]
* output stage is a power amplifier stage ; has very small output resistance, so output voltage is same, no matter what is the value of load resistance connected to the output terminal.

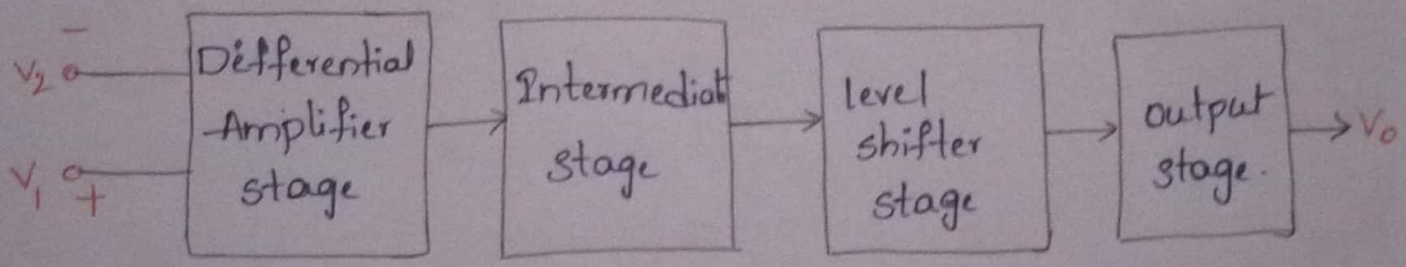


fig: Block schematic of an op-Amp

* The essential building block of modern IC op-amp is differential amplifier.

* Differential Amplifier :-

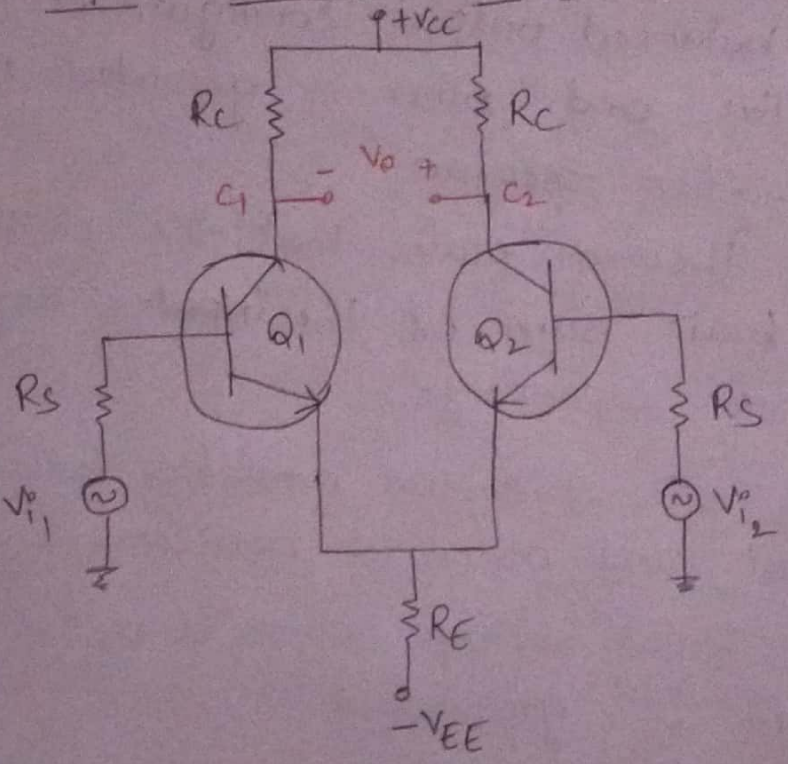
. A circuit that amplifies the difference between two signals is called a difference or differential amplifier. It is able to suppress any undesired noise which is common to both the i/p terminals.

* A differential amplifier can be used in four different configurations depending upon the number of input signals used and the way output is taken.

- The four configurations are.

1. Dual input balanced output (or) Differential Input, differential output.
2. Dual input unbalanced [single ended] output differential amplifier.
3. Single input balanced output differential Amplifier.
4. Single input unbalanced [single ended] output differential amplifier.

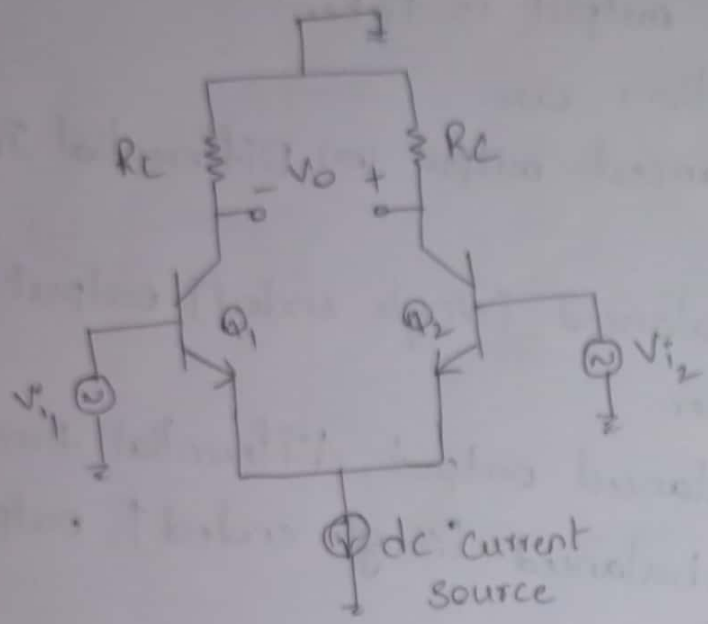
* Dual input balanced output differential Amplifier:-



* The purpose of R_E and dc source $-V_{EE}$ is to supply constant emitter current.

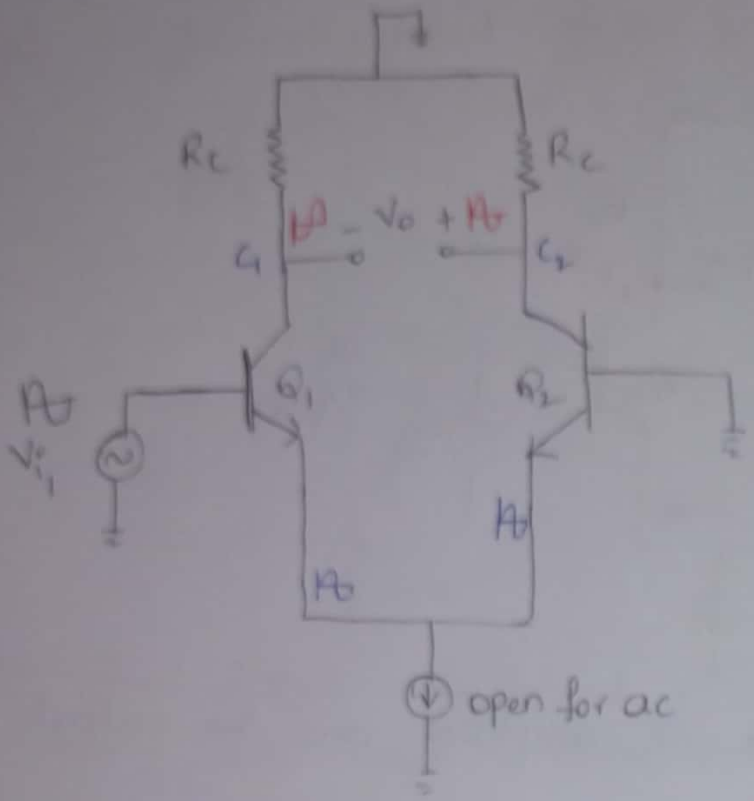
* In ac analysis we can replace R_E & V_{EE} by a constant current source.

* In ac analysis the dc voltage source are grounded and dc current source are opened.

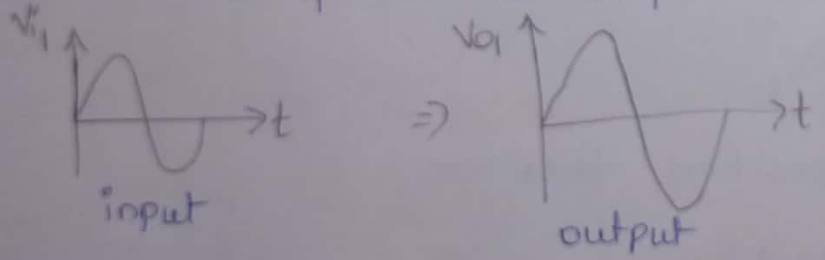


AC ckt.

* The circuit has two input voltages Vi_1 & Vi_2. In dual input balanced output configuration the one input is active and other is grounded. Here we apply Superposition theorem.
* Superposition theorem states that the output is equal to the algebraic sum of the ~~input~~ voltages produced by each source separately.
* Vi_1 and Vi_2 are differential amplifier voltages one is inverting input and other is non-Inverting input.
* one of the input voltage source is active and other input voltage is grounded.
* The output is taken at the collector of the transistors Q_1 and Q_2.



* Here Q_1 forms a CE amplifier. CE Amplifier shows the output inverter of the input. So amplified output will be at the C_1.
* At the Emitter the output is no phase inversion.
* The input for Q_2 is applied at the Emitter and base is grounded. Q_2 forms CB amplifier.
* Because of V_{i_1} the net output voltage is:



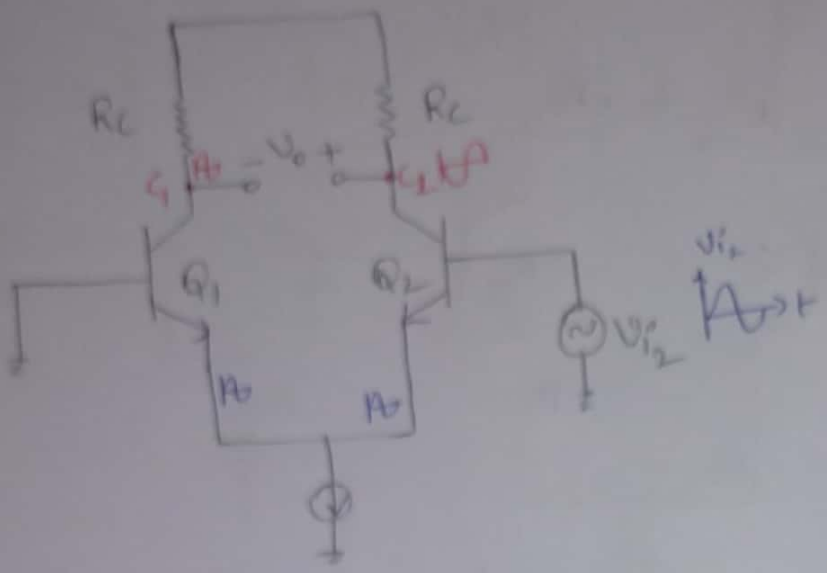
[V_{o_1} is obtained by adding o/p's of C_1 & C_2 i.e C_1-inverted o/p & C_2-non-inverted o/p. Added w.r.to C_2.]

* Q_1 transistor provides non inverting input.

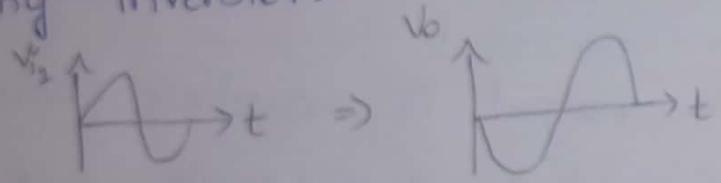
$$V_{o_1} = A \cdot V_{i_1}$$ [where A - Voltage gain]

* Now, consider the input voltage V_{i_2} is active and V_{i_1} is grounded.

*



* the Q_2 forms the CE amplifier and the output is inverted at C_2.
* Q_1 forms the CB amplifier and the output is without any inversion.



Input output

* Q_2 transistor $[V_{i_2}]$ provides Inverted input.

$$V_{o_2} = A V_{i_2}$$

- Apply Superposition theorem

$$V_o = V_{o_1} + V_{o_2}$$

Since V_{o_1} & V_{o_2} differs in phase by π

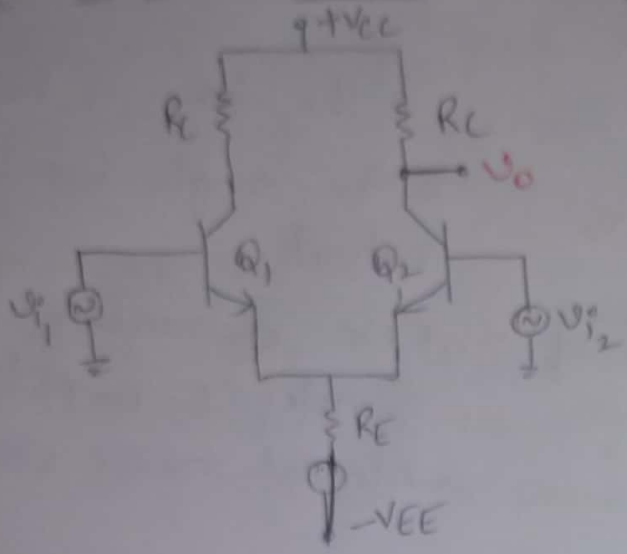
$$V_o = A V_{i_1} - A V_{i_2}$$

$$V_o = A [V_{i_1} - V_{i_2}]$$

$$V_o = A V_{id} \quad [\because V_{id} = V_{i_1} - V_{i_2}]$$

V_{id} - difference voltage.

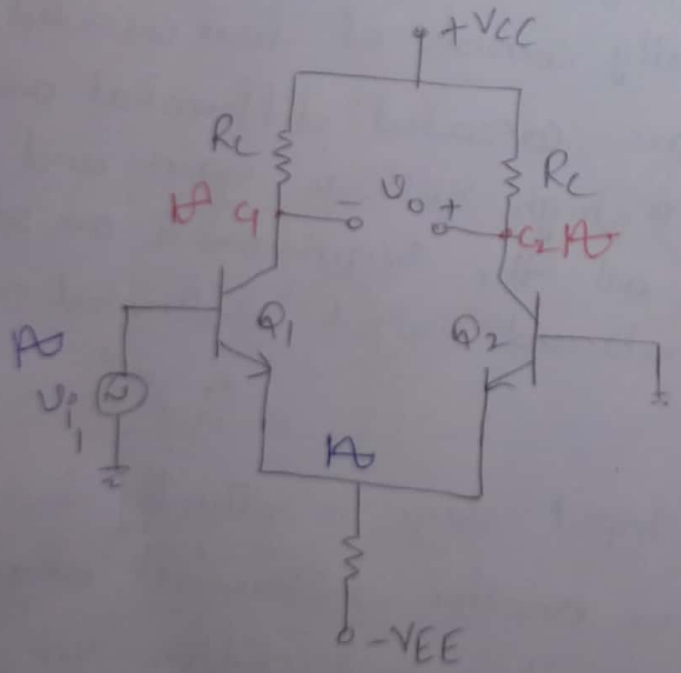
* Dual input unbalanced [single ended] output Differential Amplifier :- (11)

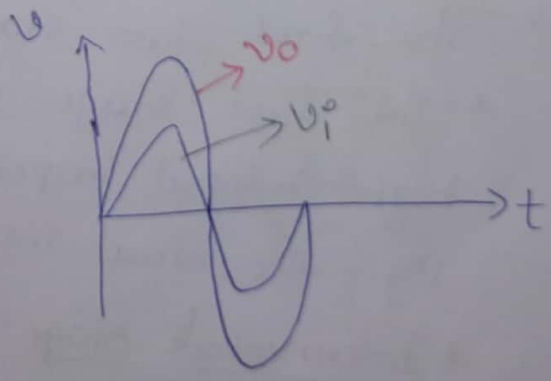


→ In dual input unbalanced output differential amplifier we apply two input voltages and output is taken from the only one collector [C_2].

* The amplification is half compared to the dual input balanced output. [because the output is taken from only one side].

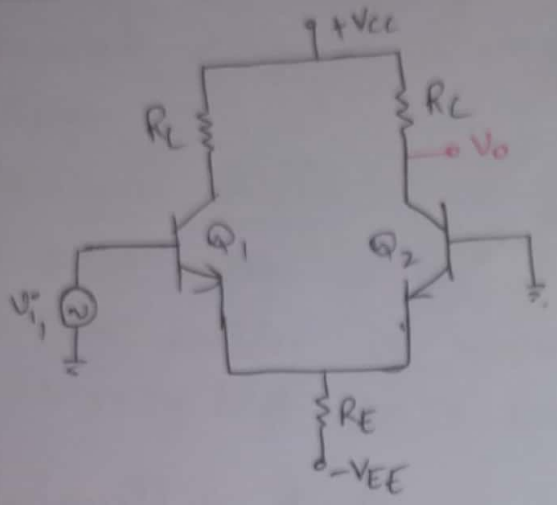
* Single input balanced output differential Amplifier:-



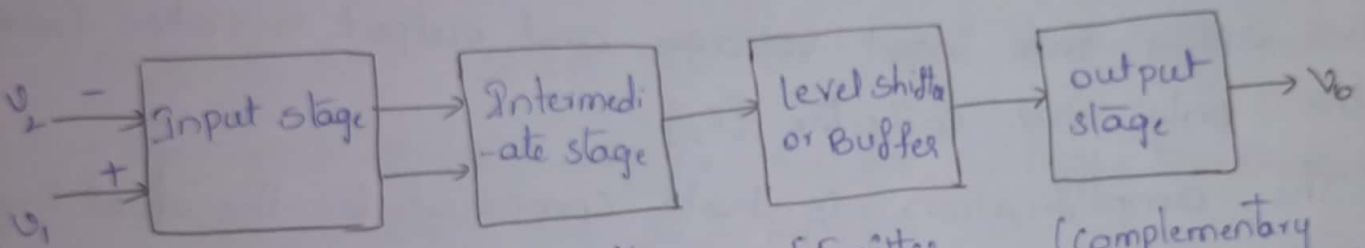


$$V_o = A V_i$$

* Single input unbalanced [single ended] output differential amplifier :-



* The Gain is half of compared to the single input balanced output.
* No advantage over Simple CE amplifier.
- Almost never used.



[Dual input balanced output differential Amplifier] [Dual i/p unbalanced o/p differential Amplifier] [Emitter follower] [complementary symmetry push pull amplifier]

fig: Schematic of op-Amp

* The IC op-amp usually consists of four cascaded block. The first two stages are cascaded differential amplifier.
* The first stage provides high voltage gain and very high i/p input impedance all the requirements are satisfy by the dual input balanced output Differential amplifier.

* Intermediate stage :-

The output of the input stage is directly feed to the Intermediate stage This is another differential amplifier with dual input unbalanced output differential amplifier.

* the main function of the intermediate stage is to provide an additional voltage gain required practically the intermediate stage is a chain of cascaded amplifier called multistage

* Buffer / level shifter :-

The third stage is acts as a buffer as well as a level shifter The buffer is usually an emitter follower. whose input is very high. so it prevents the loading of high gain stage

* Due to unbalanced output they is a dc component in output so it shifts the dc levels and adds power

* The level shifter adjusts the dc voltages so that output voltage is zero for zero inputs

* The increase in dc level tends to shift the operating point of the next stage. This inturn limits the output voltage swing and may even distort the output signal.

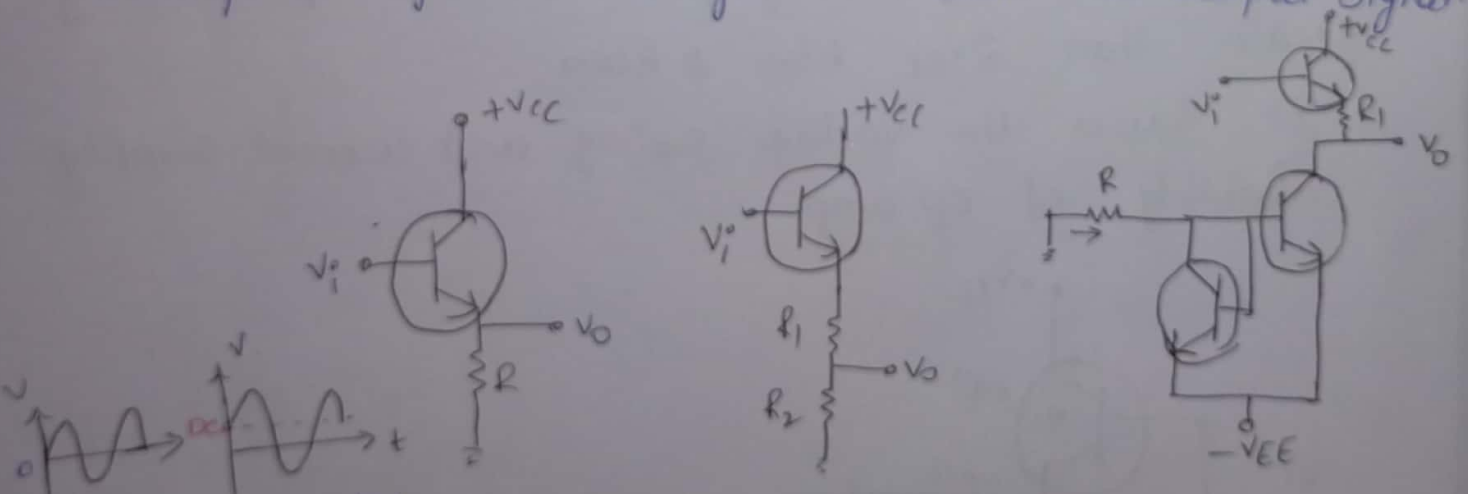


Fig :- level shifter using emitter follower.

* Output stage :-

The function of the output voltage stage in an op-amp is to supply the load current and provide a low impedance output. It should also provide a large output voltage i.e $V_{CC} + V_{EE}$

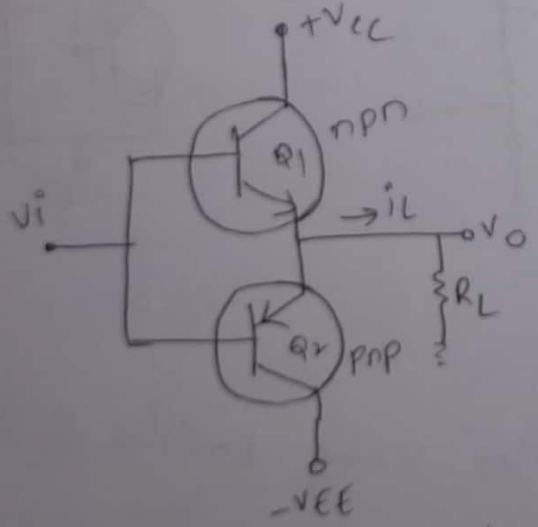
* A simple output stage consists of two complimentary transistors Q_1 [npn] and Q_2 [pnp] connected as a Emitter followers.

* for $V_i \rightarrow +ve$ the transistor Q_1 ON & supplies current to load R_L

* for $V_i \rightarrow -ve$ the transistor Q_1 is off [cut off] and Q_2 acts as a sink to remove current from the load R_L.

* A limitation occurs i.e) output voltage V_o remains zero until the i/p V_i exceeds $V_{BE(cut-in)} = 0.5V$. This is called cross over distortion. The cross over distortion can be eliminated by applying a bias voltage slightly greater than $2V_{BE}$ b/w 2 Bases.

* It raises the voltage swing and current supply capability of op amp.



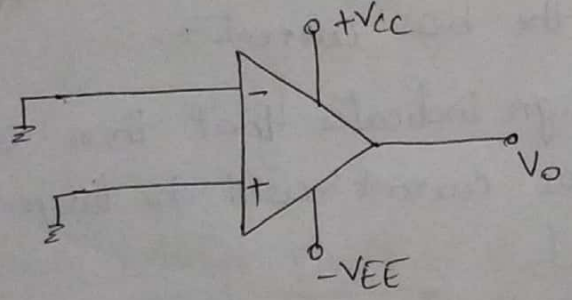
Complementary Emitter follower o/p stage

* Dc characteristics :-

* An ideal op-amp draws no current from the source and its response is also independent of temperature. However, a real op-amp does not work this way.
* Current is taken from the source into the op-amp inputs.

* Input offset voltage (V_{io}) :-

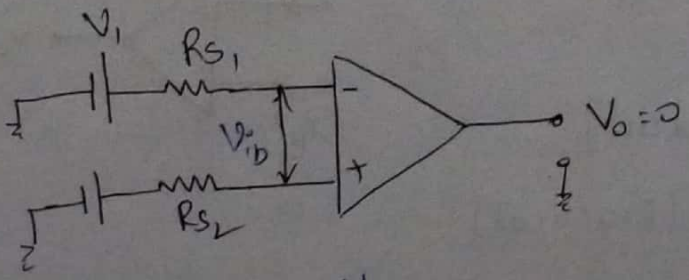
* If the input voltage V_1 & V_2 [Inverting and non-inverting] input is given as zero then the output should be zero



* Assume $V_1 = 0$ & $V_2 = 0$ and if the opamp is ideal then the output should be zero. But due to the biasing voltage the output is offset [small amount of output] This is called as Input offset voltage.
* To nullify the offset voltage that means to make the output voltage as zero. Apply the required voltage at the input terminal of op-Amp.

$V_{io} = 0V$ [Ideal]

$V_{io} = 1000uV$ [Practical]



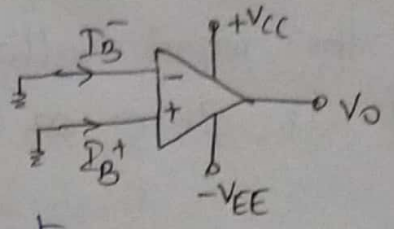
$V_{id} = V_1 - V_2$.

* Input offset current :-

* for ideal op-Amp input impedance $R_i = \infty$ but practically it is not true. The OP-Amp draws current from input dc voltage source.

* The different between the currents entering into the inverting and non-inverting terminals is referred as input offset current.

$$|I_{io}| = |I_B^+ - I_B^-|$$



Here I_B^+ & I_B^- are the bias currents.

* The absolute value sign indicates that there is no way to Predict which of bias current will be larger.

$I_{io} = 0A$ [Ideal]

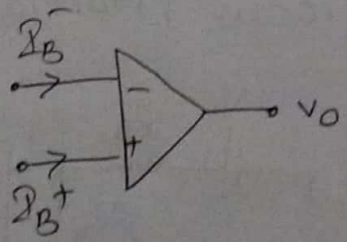
$I_{io} = 100nA$ [practical]

* Input Bias current (I_B) :-

Consider the base currents entering into inverting and non-inverting terminals as I_B^+ & I_B^- respectively. Even though transistors are identical, but I_B^- & I_B^+ are not exactly equal due to internal imbalance blw the two inputs.

* The input bias current is the average value of base current entering into the inverting and non-inverting terminal of the op-amp.

$$I_B = \frac{I_B^+ + I_B^-}{2}$$



$I_B = 0A$ [Ideal]

$I_B = 500nA$ [practical]

* Input Resistance (R_i) :-

* This is the differential input resistance of IC observed at the either the inverting or non-inverting input terminal, with the other terminal connected to ground.

$R_i = 0\ \Omega$ [Ideal] $R_i = 10^{12}\ \Omega$ for FET

$R_i = 2\ k\Omega$ [Practical] for IC 741

* Input capacitance (C_i) :-

* this is the equivalent capacitance of IC measured at either inverting or non-inverting terminal with the other terminal connect to ground.

$C_i = 0pf$ [Ideal]

$C_i = 1.5pf$ [practical]

* Input offset voltage Drift :- V_{io} (drift)

It is defined as rate of input offset voltage V_{io} with temperature (T).

V_{io} (drift) = 0 [ideal]

V_{io} (drift) = 0.2 $\mu V/^\circ C$ [practical]

V_{io} (drift) = $\frac{dV_{io}}{dT}\ \mu V/^\circ C$.

* Input offset current Drift : I_{io} (Drift)

It is defined as rate of input offset current I_{io} with temperature (T)

I_{io} (drift) = $\frac{dI_{io}}{dT}\ \mu A/^\circ C$

I_{io} (drift) = 0 [Ideal]

= 0.1 $nA/^\circ C$ [practical]

* Supply current : I_S

This current drawn by op-amp from power supply.

I_S = 2.8 mA [for 741]

* Common Mode Rejection Ratio :- [CMRR]:

The relative sensitivity of an op-amp to difference signal as compared to common mode signal is called common Mode Rejection Ratio [CMRR] and gives the figure of merit for differential amplifier

* It is defined as Ratio of differential voltage gain (Ad) to common mode voltage gain (Acm)

$$CMRR = \left| \frac{Ad}{Acm} \right|$$

* This parameter indicates capability of OP-Amp to reject noise

* The higher the value of CMRR, the better noise immunity

CMRR expressed in decibels (dB)

CMRR = ∞ [ideal]

CMRR = 10dB [practical]

* Power Supply rejection Ratio [PSRR]:-

The change in an op-Amp input offset voltage (V_{io}) due to variation in power supply voltage $+V_{CC}$ or $-V_{EE}$ is called power supply Rejection Ratio. This is also called as power supply sensitivity

$$PSRR = \frac{\Delta V_{io}}{\Delta V} \quad \mu V/V$$

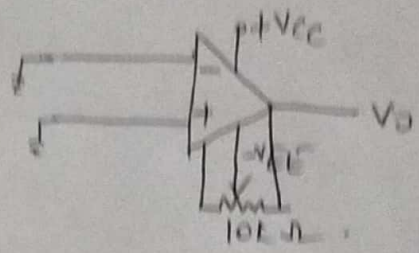
PSRR = 0 [Ideal]

= 150 μV/V [Practical]

* Offset voltage Adjustment :-

* for an op-Amp [IC 741] pin number 1 and 5 are provided for making the offset adjustment
* A 10kΩ potentiometer is connected or wiper of pot is connected to -ve supply. The wiper of pot is adjusted till V_o becomes zero

Range ± 15mV



* Output voltage swing :-

This parameter indicates value of +ve and -ve saturation voltages of an op-Amp and never exceeds the supply voltage V^+ and V^-. The output voltage swing is guaranted b/w +13V and -13V for $R_L \rightarrow 2k\Omega$

* Power Consumption :- (P)

This gives amount of quiscent power that must be consumed by op-Amp so as to operate properly.

P - 85mw.

* Output Resistance : R_o

output resistance R_o is resistance measured b/w output terminal of op-amp and ground.

$R_o = 0\Omega$ [ideal]

$R_o = 75\Omega$ [pratical]

* output short circuit current : I_{sc}

This is current that may flow if an op-amp gets shorted accidentally and is generally high. the op-amp must be provided with short ckt protection

I_{sc} : 25mA [for 741 IC]

*AC characteristics :-

The Dc characteristics such as bias current, input offset current, offset voltage and thermal drift there will effect the steady state (Dc) response of the op-amp only. for small signal sinusoidal (AC) application. The ac characteristics are frequency response, stability of op-Amp and slew rate.

*frequency response :-

Ideally an op-amp has infinite bandwidth. The open loop gain should remain constant throughout audio (low) & radio (high) frequencies.

* But in practical op amp the gain decreases with increase in frequency (or) gain decreases (roll off) at higher frequencies.
* The gain of op amp roll off after certain frequency due to capacitive ~~cap~~acitor- component present in equivalent ckt of op amp.
* The op Amp contains the active elements like BJT & FET. The transistors contains junction capacitor all the capacitor are placed by a single capacitor.
* the capacitance is due to physical characteristics of the device. The high frequency model of an op Amp with signal corner frequency is modified version of low frequency model with capacitor 'c' at o/p.
* There is one pole due to RoC and one -20dB/dec roll-off into effect.

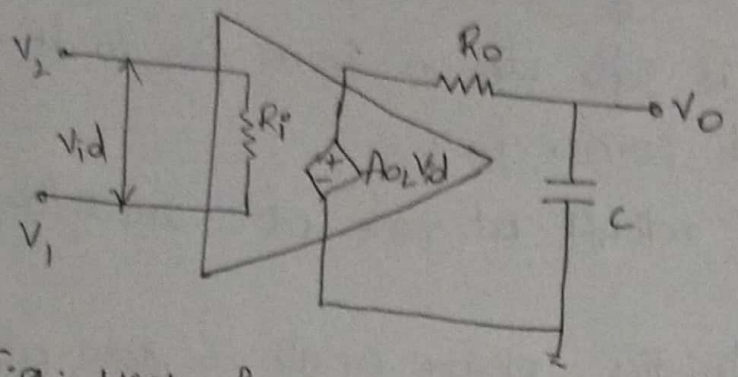


fig:- High frequency model of Op-Amp with single corner frequency.

* Open loop gain of Op-Amp with one corner frequency is given by.

$$V_o = \left[\frac{X_c}{R_o + X_c}\right] A_{OL} V_{id}$$

$$\frac{V_o}{V_{id}} = A_{OL}\left[\frac{1/j\omega c}{R_o + 1/j\omega c}\right]$$

$$A = A_{OL}\left[\frac{1}{1 + j\omega c R_o}\right] \qquad \left[\because \frac{V_o}{V_{id}} = A \;;\; X_c = \frac{1}{j\omega c}\right]$$

$\omega = 2\pi f$.

$$A = A_{OL}\left[\frac{1}{1 + j2\pi f c R_o}\right] \qquad f_1 = \frac{1}{2\pi R_o C}$$

$$\boxed{A = A_{OL}\left[\frac{1}{1 + j[f/f_1]}\right]}$$

Where f_1 is corner frequency (or) 3-dB frequency of Op-Amp (or) break frequency. f is operating frequency.

* The magnitude and the phase angle of the open loop voltage gain are the function of frequency can be written as

$$\boxed{|A| = \frac{A_{OL}}{\sqrt{1 + (f/f_1)^2}}} \;;\; \boxed{\phi = -\tan^{-1}[f/f_1]}$$

* Magnitude and phase characteristics :-

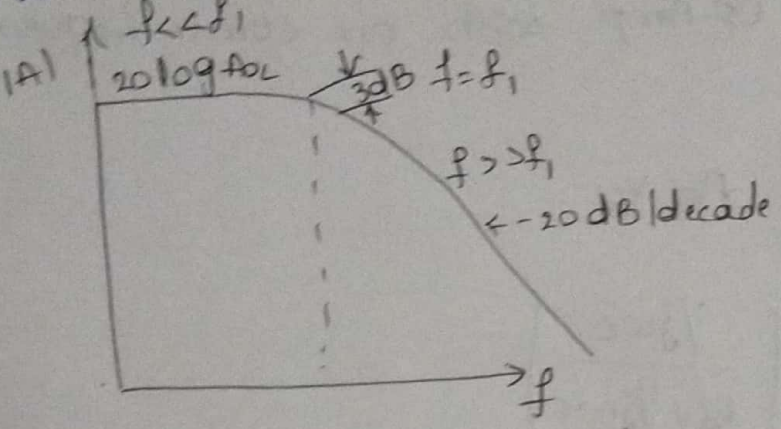
i) for freq $f << f_1$, magnitude of gain is $20\log A_{OL}$ in dB.

ii) for $f = f_1$, gain is 3dB drown from A_{OL} in dB. This freq f_1 is called corner freq.

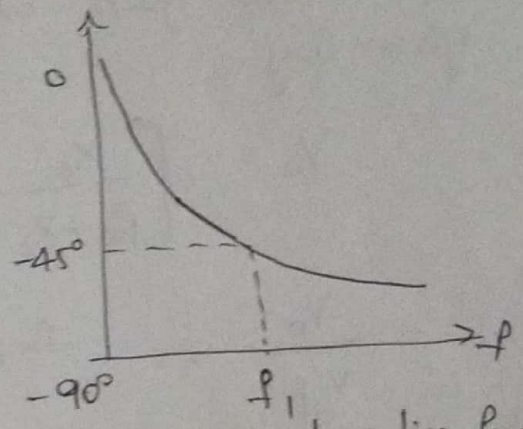
iii) for $f >> f_1$ gain roll off at rate of -20dB/decade or -6dB/octave.

* from phase characteristics, phase angle is zero at $f = 0$

At corner frequency $f = f_1$, $\phi = -45°$, $\phi = -90°$ lagging at $f = \infty$.



Open loop Magnitude characteristics



phase characteristics for an op-Amp with single break frequency.

* The maximum of 90° phase charge can occur in op-Amp with single capacitor.

* Transfer function in s-domain given by [with single break frequency)

$$A = \frac{-A_{OL}}{1 + j(f/f_1)} = \frac{A_{OL}}{1 + j[\omega/\omega_1]} \qquad [\omega = 2\pi f,\ \omega_1 = 2\pi f_1]$$

$$= \frac{A_{OL}\,\omega_1}{\omega_1 + j\omega_1} \Rightarrow \frac{A_{OL}\,\omega_1}{s + \omega_1} \qquad [s = j\omega]$$

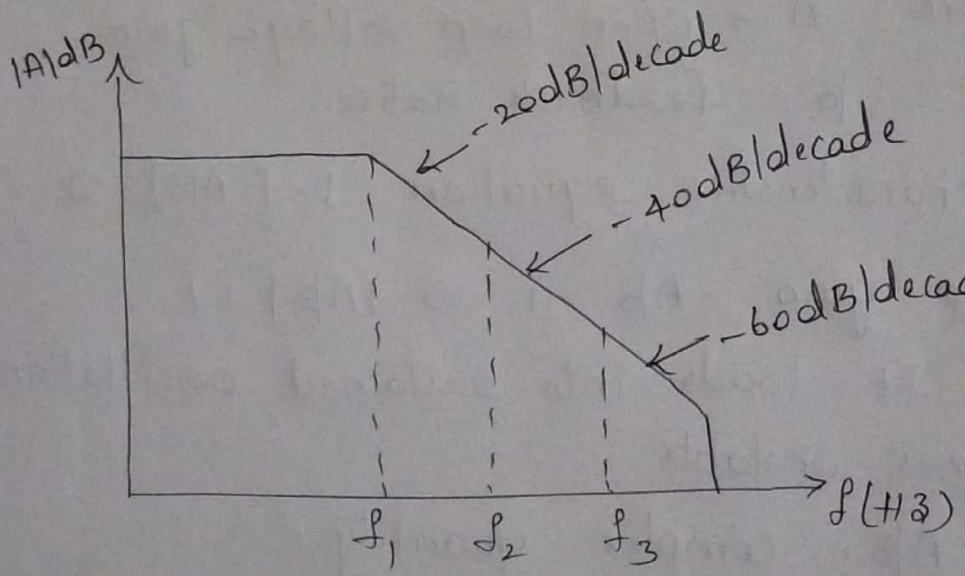
* A practical op amp has number of stages. Each stage produces capacitive component. This is due to number of Rc pole pair. there exist number of break frequency

* Transfer function of an op-Amp (with three break frequencies)

$$A = \frac{A_{OL}}{(1+jf/f_1)(1+j(f/f_2)][1+jf/f_3]} \qquad 0 < f_1 < f_2 < f_3$$

In s-domain

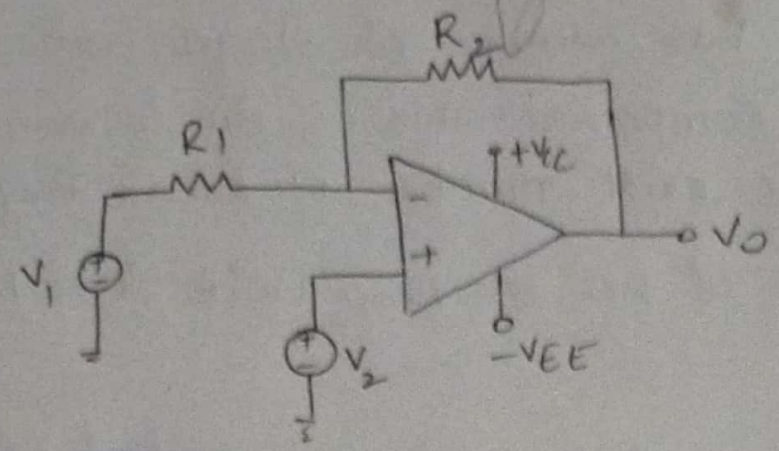
$$A = \frac{A_{OL}\,\omega_1\,\omega_2\,\omega_3}{(s+\omega_1)(s+\omega_2)(s+\omega_3)} \qquad 0 < \omega_1 < \omega_2 < \omega_3$$



* stability of op-Amp :-

op-Amps are rarely used in open-loop configuration due to its high gain.

* Consider an op-amp. It uses resistor feedback network and may be used as inverting amplifier with $V_2 = 0$ and as non-inverting Amplifier with $V_1 = 0$.



$A < 1$
$A\beta \leq 180°$ } stable

$-A > 1$
$-A\beta > 180°$ } unstable

Resistive feedback provided in op-amp

* from the negative feedback the closed loop transfer function is given

$$A_{CL} = \frac{A}{1 + A\beta} \quad -(1)$$

where $A \rightarrow$ open loop voltage gain

β - feedback ratio.

* If characteristics equation $1 - [-A\beta] = 0$

loop gain $-A\beta = 1 \Rightarrow |A\beta| = 1$

* The ckt loads into sustained oscillations and becames unstable

$A\beta$ - complex quantity.

$|A\beta| = 1 \rightarrow$ Magnitude condition

$\angle -A\beta = 0$ or $\angle -A\beta = \pi$.

* In op-Amp, feedback network is resistive n/w and does not provide the any phase shift. Since op-Amp used in Inverting mode, it provides a phase shift of 180° at low frequency.

* At high frequencies due to each number of freq an additional phase shift of max $-90°$ occurs with loop gain A

Thus for two corner freq a max of phase shift associated with gain A is $-180°$

* Thus at high frequencies, for small values of β the magnitude of $A\beta$ becomes unity when A has additional phase shift of $180°$ which makes total phase shift equal to zero.

* Hence the amplifier begins to oscillate as both magnitude and phase conditions are satisfied. Thus oscillation is just starting point of instability.

Instability means unbounded o/p

$\frac{A}{1+A\beta} < 1$

$A\beta < 0$ [negative]

* $A_{CL} < A$ closed loop gain ↓ses and system is stable.

for $A_{CL} > A$ closed loop gain ↑ses and system is unstable.

* At high frequencies, system 'A' bea having 3 corner frequencies (or) 3 RC pole pair there is chance of open loop gain A to contribute max of $-270°$ phase shift.

* $A\beta$ becomes -ve and instability occurs at high frequencies.

* Unstable systems are impractical and need to be made stable. The modification given for stability is used when the system is to be tested practically.

However theoritically analytical or graphical methods are almost used to test system for stability before they are build

Analytical method - Routh Hurzwitt critieria
Graphical method - Bode plot.

* Slew rate :-

The slew rate is define as maximum rate of charge of output voltage with respect to time caused by step input voltage and usually specified in V/μs

$$SR = \left.\frac{dV_o}{dt}\right|_{max}$$

Simple def. : How fast the op-amp will able to respond.

Ex:- 1V/μs → slew rate means that o/p raises or falls by 1V in 1μsec.

* An ideal slew rate is infinite which means op-Amp o/p voltage should change instantaneously in response to i/p step voltage.
* op-amp slew rate is related to its freq. response. Op-Amp with wide bandwidth will have higher slew rate.
* Practical op-Amp slew rate ranges from 0.1V/μs to 1000V/μs
* The slew rate improves with higher closed loop gain and Dc supply voltage. It is also a function of temperature and generally decreases with an increases in temperature.
* Cause of slew rate :-
  * The cause of slew rate is capacitor within (or) outside of op-Amp to prevent oscillation.
  * This internal capacitor which prevents the o/p voltage from responding immediately to fast charging i/p.

* The voltage across the capacitor is given as

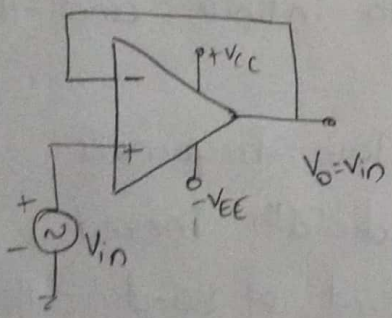
$$V_c = \frac{1}{C}\int i\,dt$$

$$\boxed{\frac{dV_c}{dt} = \frac{I}{C}} \Rightarrow SR = dv$$

* Here I_{max} current drawn by Op-Amp to capacitor C.
* for faster slew rate op-Amp should have higher current (or) small compensating capacitor.
* for 741 the max. internal capacitor charging current is limited to about 15μA. so the slew rate (SR) of 741 is

$$SR = \frac{dv_c}{dt}\Big/_{max} = \frac{I_{max}}{C} = \frac{15\mu A}{30pf} = 0.5\,V/\mu sec.$$

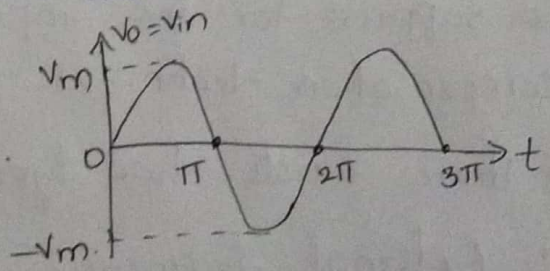
* The SR limits the response speed of all large signal wave shapes for sine wave i/p the effect of slew rate can be calculated as.



* let us consider a voltage follower
* Assume the i/p signal with high voltage (Amplitude) & high freq. sine wave.

If $V_{in} = V_m \sin\omega t$

Then the o/p $V_o = V_m \sin\omega t$.



The rate of change of the o/p is given by

$$\frac{dV_o}{dt} = V_m \omega \cos\omega t$$

and the maximum rate of change of the o/p occurs when $\cos\omega t = 1$ i.e

$$SR = \frac{dv_o}{dt} = \omega V_m$$

$$SR = 2\pi f V_m \; V/s$$

$f \Rightarrow$ i/p freq.
V_m = Peak value of the sine wave.

$$SR = \frac{2\pi f V_m}{10^6} \text{ V/µs}$$

* Thus the max freq f_{max} at which is can obtain an undistorted o/p voltage of peak value V_m is given by

$$f_{max} = \frac{\text{Slew rate}}{2\pi V_m}$$

$$f_{max}(\text{HZ}) = \frac{\text{slew rate}}{6.28 \times V_m}$$

* f_{max} is also called the full power response. It is the max freq of a large amplitude sine wave with which op amp can have without distortion. If either frequency or the amplitude of the i/p signal is increased to exceed the slew rate of the op-Amp the o/p will be distorted.

* Frequency Compensation:-

* Ideal op-Amp has bandwidth infinite and the open loop voltage is infinite.
* the gain is constant at low frequencies.
* At high frequency the bandwidth increases noise components To suppress for the improvement of Bandwidth frequency compensation technique is used.
* There exists two types of compensating techniques.

(i) External frequency compensation
   (a) Dominant pole
   (b) Pole Zero compensation

(ii) Internal compensation.

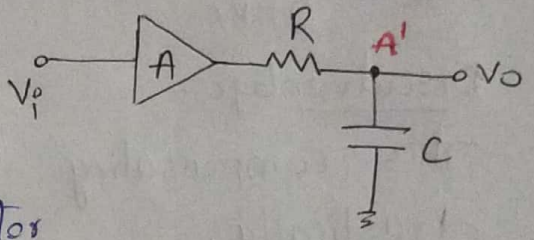
(i) External Frequency compensation:-

Some types of op-Amps are made to be used with externally connected compensating components specially if they are to be used for relatively low closed loop gain.

* Dominant pole compensation:-

Suppose A is the transfer function or Gain of uncompensated network.

* A' is the transfer function or Gain of compensated network.
* Introduce dominant pole by adding RC n/w in series with op-amp (or) by connecting capacitor 'C' from suitable high resistance point to ground.



$$A' = \frac{V_o}{V_i^\circ}$$

$$= \frac{A\left[-j/\omega c\right]}{R - j\omega/c} = \frac{A \cdot 1/j\omega c}{1 + j\omega CR}$$

The o/p voltage V_o

$$V_o = \left(\frac{X_C}{R + X_C}\right) V_i^\circ$$

$$\frac{V_o}{V_i^\circ} = \frac{1/j\omega c}{R + 1/j\omega c}$$

$$A' = \frac{A}{1 + j2\pi fCR} \qquad \text{where } f_d = \frac{1}{2\pi RC}$$

$$\boxed{A' = \frac{A}{(1 + j f/f_d)}}$$

* Compensated transfer function A' with three corner frequencies

$$A' = \frac{A_{OL}}{(1+jf/f_d)(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)}$$

where $f_d < f_1 < f_2 < f_3$

* The frequency found graphically by having A' pass through 0dB at the pole f_1 with slope of -20dB/decade.
* The value of capacitor can be calculated using

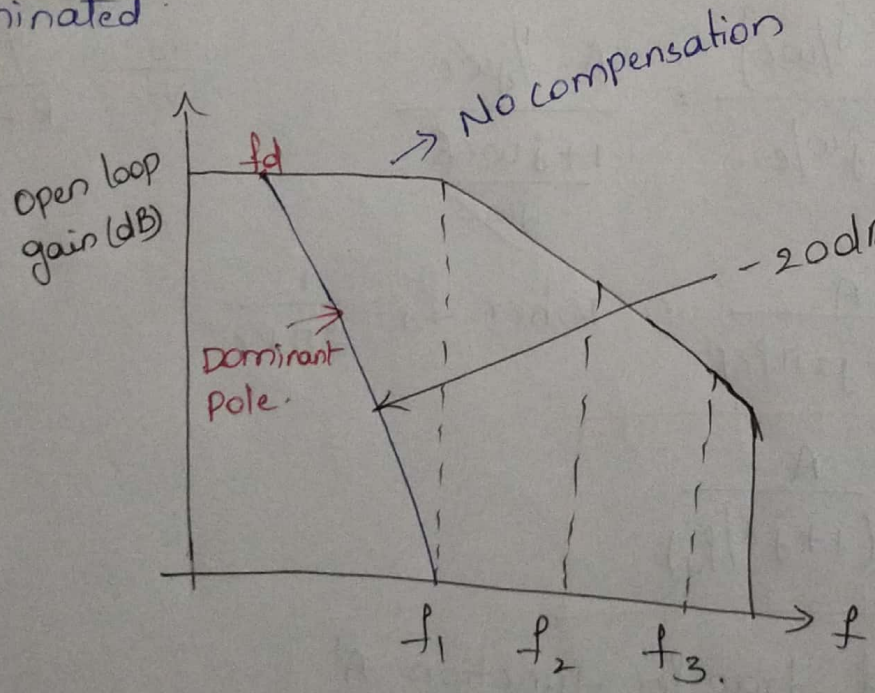
$$f_d = \frac{1}{2\pi RC}$$

Disadvantage:-

This compensating technique reduces open loop bandwidth drastically.

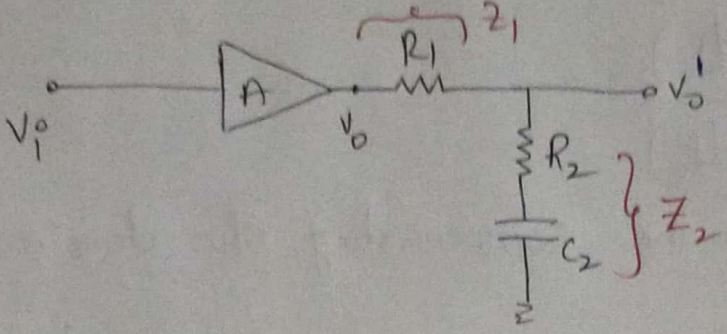
Advantage:-

The noise immunity of system is improved since the noise frequency components outside the bandwidth are eliminated.



* Pole Zero compensation :-

Here the uncompensated transfer function A' is altered by adding both pole and zero.



* The compensating n/w is designed to produce zero at first corner freq. f_1 of uncompensated transfer function A. This zero will cancel the effect of pole at f_1.
* The pole of compensating network f_o is selected such that compensated transfer function A' passes through 0dB at second corner frequency f_2 of uncompensated transfer function A.

$$\frac{V_o'}{V_o} = \frac{Z_2}{Z_1 + Z_2}$$

where $Z_1 = R_1$,

$$Z_2 = R_2 + \frac{1}{j\omega C_2}$$

$$= \frac{R_2 + \frac{1}{j\omega C_2}}{R_1 + R_2 + \frac{1}{j\omega C_2}}$$

$$\frac{V_o'}{V_o} = \frac{1 + j\omega C_2 R_2}{j\omega C_2 R_1 + j\omega C_2 R_2 + 1}$$

$$\frac{V_o'}{V_o} = \frac{1 + j2\pi f R_2 C_2}{j2\pi f R_1 C_1 + j2\pi R_2 C_2 + 1}$$

$$\frac{V_o'}{V_o} = \frac{1 + j 2\pi f R_2 C_2}{j 2\pi f C_2 (R_1 + R_2) + 1}$$

$$f_1 = 2\pi R_2 C_2$$

$$f_0 = 2\pi (R_1 + R_2) C_2$$

$$\frac{V_o'}{V_o} = \frac{1 + j (f/f_1)}{1 + j (f/f_0)}$$

* Assuming that the compensating n/w does not load the amplifier.

$R_2 >> R_1$ then overall transfer function becomes

$$A' = \frac{V_o'}{V_i} = \frac{V_o'}{V_o} \cdot \frac{V_o}{V_i} = A \cdot \frac{R_2}{R_1 + R_2} \left[\frac{1 + j(f/f_1)}{1 + j(f/f_0)} \right]$$

$$A' = \frac{A_{OL}}{(1 + jf/f_1)(1 + jf/f_2)(1 + jf/f_3)} \cdot \frac{R_2}{R_1 + R_2} \left[\frac{1 + j(f/f_1)}{1 + j(f/f_0)} \right]$$

$$A' = \frac{A_{OL}}{(1 + jf/f_0)(1 + jf/f_2)(1 + jf/f_3)} \left[\because R_2 >> R_1, \frac{R_2}{R_1 + R_2} \simeq 1 \right]$$

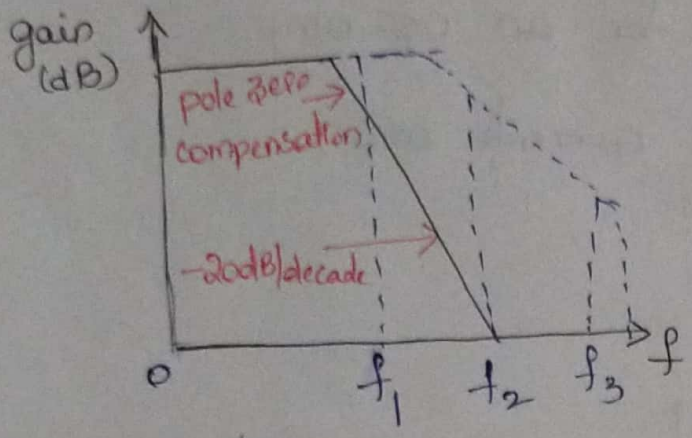
$0 < f_0 < f_1 < f_2 < f_3$

let $R_2 >> R_1$ such that $\frac{R_2}{R_1 + R_2} \simeq 1$

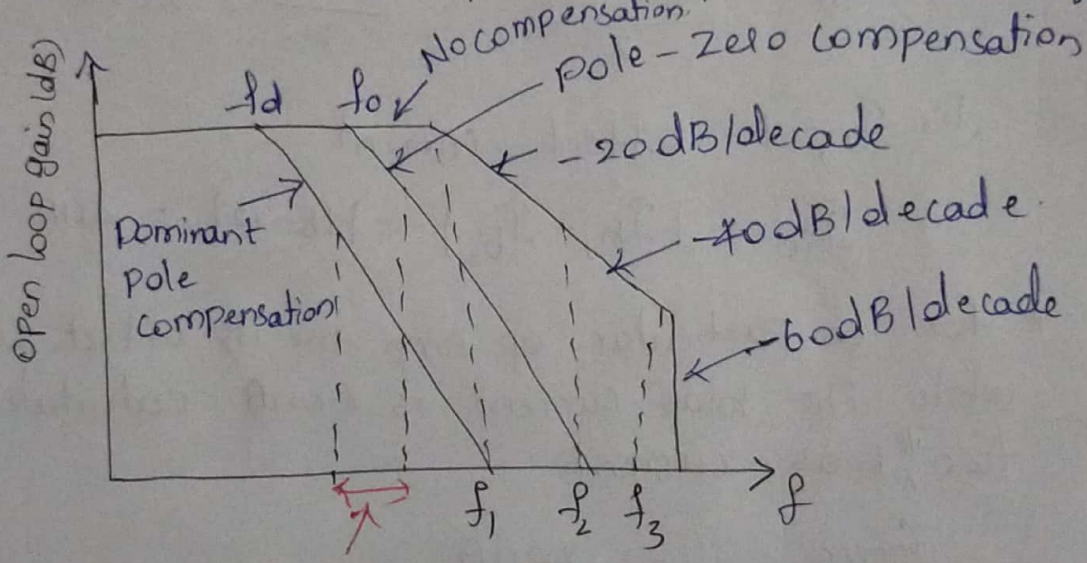
* consider the frequency response for uncompensated op-Amp having three poles at frequencies f_1, f_2, f_3

* Select R_2 & C_2 such that zero of compensating n/w is equal to pole at freq. f_1

*The pole at f_0 should be selected such that -20dB/decade fall should meet the 0dB line at f_2 which is second pole of A.



* Comparison of dominant pole and pole zero technique,



3dB Bandwidth improvement.

*features of op-Amp :-

- High differential voltage gain
- low common mode gain
- High CMRR
- Two i/p terminals
- large B.W
- low offset voltage & currents
- low o/p impedance.

* If the base current for the emitter coupled transistor of differential amp^r are 18μA & 22μA. Determine
(i) Input bias currents.
(ii) Input offset current for an op-amp.

The two input base currents are

$I_{b_1} = 18\mu A$

$I_{b_2} = 22\mu A$

(i) Input bias current

$$I_b = \frac{I_{b_1} + I_{b_2}}{2} = \frac{18+22}{2} = 20\mu A$$

(ii) Input offset current

$$I_{io} = |I_{b_1} - I_{b_2}| = |18-22| = 4\mu A.$$

* for a particular op-Amp the i/p offset current is 20nA while i/p bias current is 60nA. calculate the values of two i/p bias currents

Given $I_{io} = 20nA$

$I_B = 60nA$

$$I_{io} = |I_{b_1} - I_{b_2}| = 20$$

$$I_B = \frac{I_{b_1} + I_{b_2}}{2} = 60 \Rightarrow 120 = I_{b_1} + I_{b_2}$$

$$I_{b_1} - I_{b_2} = 20$$

$$I_{b_1} + I_{b_2} = 120$$

$$2I_{b_1} = 140$$

$$\Rightarrow I_{b_1} = 70nA \quad ; \quad I_{b_2} = 50nA.$$

PROBLEMS

* The i/p signal V_i to an op-amp is $0.04 \sin 1.13 \times 10^5 t$ is to be amplified to the maximum extent. How much maximum gain can be obtained by using op-amp with slew rate of 0.4 V/μsec.

Sol Given input compared with

$V_i = V_m \sin \omega t$

$V_i = 0.04 \sin 1.13 \times 10^5 t$

$\therefore V_m = 0.04$

$\omega = 1.13 \times 10^5$

Also $f_m = \frac{SR}{2\pi V_m}$ — (1)

$\omega = 2\pi f_m \Rightarrow 1.13 \times 10^5 = 2\pi f_m$

$f_m = \frac{1.13 \times 10^5}{2\pi}$ — (2)

Equating Eqn (1) & (2),

$\frac{SR}{2\pi V_m} = \frac{1.13 \times 10^5}{2\pi}$

Given $SR = 0.4 \text{ V/μsec}$

$\frac{0.4}{\frac{10^{-6}}{V_m}} = 1.13 \times 10^5$

$\therefore V_m = \frac{0.4 \times 10^6}{1.13 \times 10^5} = 3.54 \text{ V}$

This is magnitude of o/p voltage

$\text{Gain} = \frac{V_{m(o/p)}}{V_{m(i/p)}}$

$\text{Gain} = \frac{3.54}{0.04} = 88.5$

* In response to square wave i/p the o/p of an op-Amp changed from -3V to +3V over a time period of 0.25 μs. Determine the slew rate of an op-Amp.

Sol change in output voltage -3V to +3V

$$dV_o = 3-(-3) = 6V$$

$$dt = 0.25\mu s$$

$$S = \frac{dv_o}{dt} = \frac{6}{0.25\times10^{-6}} = 24\ V/\mu s.$$

* How fast can the output of op-Amp change by 10V if its slew rate is 1V/μs?

$$S = 1\ V/\mu s = \frac{1}{1\times10^{-6}} = 1\times10^{6}\ V/s$$

$$S = \frac{dv_o}{dt} \Rightarrow \Delta V_o = 10V$$

$$1\times10^{6} = \frac{10}{\Delta t}$$

$$\Delta t = \frac{10}{1\times10^{6}} = 10\ \mu sec$$

∴ Thus 10 μsec is required by an op-amp to change output by 10V.

* for an op-Amp, PSRR = 70dB(min) CMRR = 10^5 & differential mode gain $A_d = 10^5$. The o/p voltage changes by 20V in 4μsec calculate

(i) Numerical value of PSRR

(ii) Common-Mode gain

(iii) Slew Rate.

Sol) PSRR must be as small as possible

(i) $(PSRR)_{dB} = 20 \log_{10} PSRR$

$-70 = 20 \log_{10} PSRR.$

$PSRR = 10^{(-3.5)}$

$= 3.1622 \times 10^{-4}$ V/volts

$= 31.622$ mV/volts

(ii) $\frac{A_d}{A_c} = CMRR$

$10^5 = \frac{10^5}{A_c} \Rightarrow A_c = 1$

(iii) $\Delta V_o = 20V$

$\Delta t = 4 \mu sec$

Slew rate $= \frac{\Delta V_o}{\Delta t} = \frac{20}{4 \times 10^{-6}}$

$= 5 \times 10^6$ V/sec

$= 5$ V/μsec.

* for an op-Amp. $I_{CQ} = 15\mu A$ and $C = 35pf$ The peak value of i/p is 12V. Determine slew rate and maximum possible frequency of i/p voltage that can be applied to get undistorted o/p.

Sol $I_{max} = I_{CQ} = 15\mu A$

$C = 35pf$, $V_m = 12V$

Slew rate $SR = \frac{I_{max}}{C} = \frac{15 \times 10^{-6}}{35 \times 10^{-12}}$

$= 0.4285 \times 10^6 V/sec$

$= 0.43 V/\mu sec$

$f_m = \frac{SR}{2\pi V_m} = \frac{0.4285 \times 10^6}{2\pi \times 12}$

$= 5.684 KHz$

upto this frequency o/p is distorted.

* An op-Amp has a differential gain of 80dB and CMRR of 95dB. If $V_1 = 2\mu V$ & $V_2 = 1.6\mu V$ then calculate the differential and common mode output values.

Given $A_d = 80dB$ & CMRR = 95dB

$V_1 = 2\mu V$ & $V_2 = 1.6\mu V$

$A_d(dB) = 20 \log A_d$

$\therefore 80 = 20 \log A_d$

$\therefore A_d = 10^4$

$CMRR(dB) = 20 \log CMRR$

$95 = 20 \log CMRR$

$\therefore CMRR = 5.62 \times 10^4$

Differential voltage gain

$$A_d = \frac{V_{od}}{V_{id}} = \frac{V_{od}}{(V_1 - V_2)}$$

$$V_{od} = A_d(V_1 - V_2) \Rightarrow V_d = 1 \times 10^4 (2 - 1.6) \times 10^{-6}$$

$V_{od} = 4mV$

Common mode voltage gain

$$A_{cm} = \frac{V_{ocm}}{V_{icm}} = \frac{V_{ocm}}{\left(\frac{V_1 + V_2}{2}\right)}$$

$$V_{ocm} = A_{cm}\left[\frac{V_1 + V_2}{2}\right]$$

Also $CMRR = \frac{A_d}{A_{cm}} \Rightarrow 5.62 \times 10^4 = \frac{10^4}{A_{cm}}$

$A_{cm} = 0.1778$

$\therefore V_{ocm} = 0.1778 \times \left[\frac{2 + 1.6}{2}\right] \times 10^{-6} \Rightarrow V_{ocm} = 0.32\mu V.$

*Modes of operations :-

• Open loop op amp configuration :-

The term open loop indicates that no connection either direct (or) another n/w. Exist b/w the o/p and i/p. i.e the output signal is not fedback to input signal.

*In open loop configuration the op-amp simply function as a high gain amplifier. There are three types of open loop op-Amp configurations.

(i) Differential Amplifier
(ii) Inverting Amplifier.
(iii) Non-Inverting Amplifier.

* These configuration are classified according to the number of inputs used.

*Differential Amplifier :-

In this the input V_{in_1} & V_{in_2} are applied to the +ve & -ve i/p terminals. Since the op-amp amplifiers the difference between the two i/p signals. This configuration is called as the Differential amplifier.

*The op-amp is a versatile device because it amplifies both ac & dc input signals. That means the V_{in_1} & V_{in_2} could be either ac or dc voltages.

*The source resistances R_{in_1} & R_{in_2} are normally ~~negligible~~ negligible compared to the i/p resistance R_i.

∴ The voltage drop across the resistors can be assumed to be zero which then implies that

$$V_1 = V_{in_1} \quad \& \quad V_2 = V_{in_2}$$

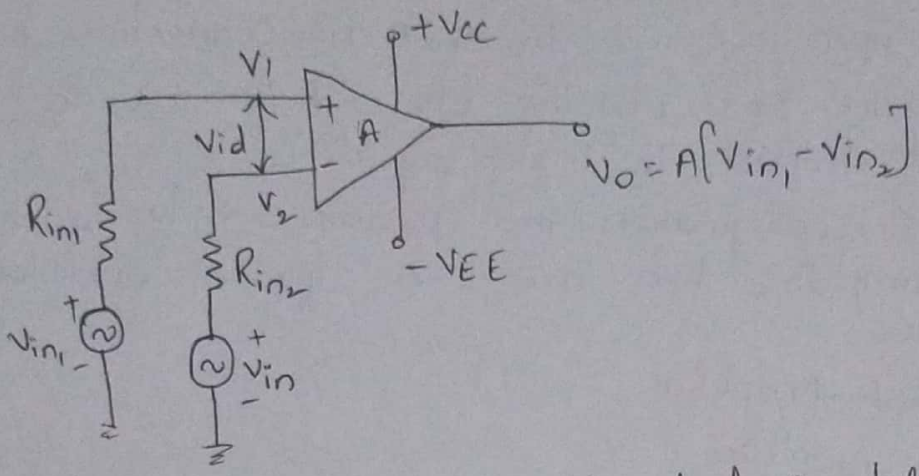
then $V_o = A V_{id}$

$$= A[V_1 - V_2] \Rightarrow A[V_{in_1} - V_{in_2}] = V_o$$

*The o/p voltage is equal to the voltage gain A times the difference b/w two i/p voltages. And the polarity of the o/p voltage is dependent on the polarity of the

the O/P switches b/w

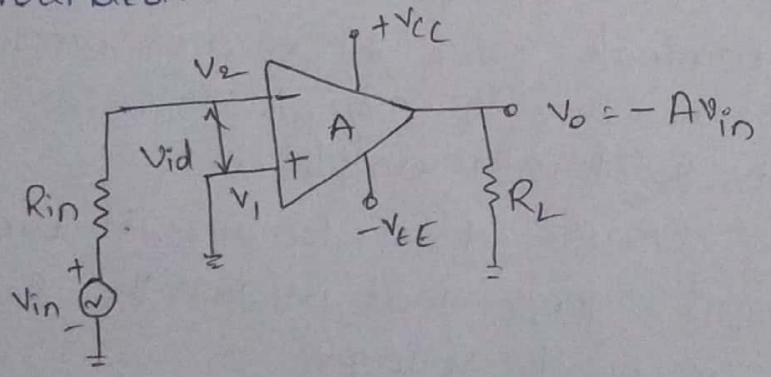
difference V_d. $[V_{in_1} - V_{in_2}]$ In open loop configuration, gain A is commonly referred as open loop gain.



open loop Differential Amplifier.

(ii) Inverting Amplifier :-

In the inverting Amplifier only one i/p is applied and that is to the inverting i/p. The non inverting i/p terminal is grounded.



Since $V_1 = 0$

$V_2 = V_{in}$

$V_o = A[V_{in_1} - V_{in_2}]$

$= A[0 - V_{in_2}]$

$V_o = -AV_{in}$.

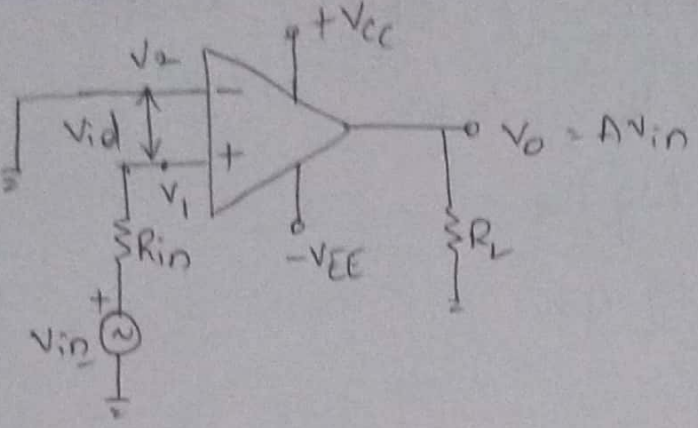
Inverting Amplifier.

* The -ve sign indicates that the o/p ~~volat~~ voltage is out of phase w.r.to i/p by 180° or is of opposite polarity.

* Thus in inverting Amplifier the input signal is amplified by gain A and is also inverted at the output.

* Non-Inverting Amplifier:-

In this the i/p is applied to the non-inverting i/p terminal and the inverting terminal is connected to ground.



$V_1 = V_{in}$, $V_2 = 0V$

$V_o = A[V_{in_1} - V_{in_2}]$

$V_o = A[V_{in} - 0]$

$\boxed{V_o = AV_{in}} \Rightarrow A = \frac{V_o}{V_{in}}$

* The o/p voltage is larger than the i/p voltage by gain 'A' i.e is in-phase with the i/p signal.
* In all three open loop configuration any i/p signal i.e only slightly greater than zero drives the o/p to saturation level. This results from the very high gain (A) of the op-Amp thus when operated open loop the o/p of the op-Amp is either +ve or -ve saturation (or) switches b/w +ve & -ve saturation levels.
* for this reason open loop op-Amp configuration are not used in linear applications But used in the voltage comparator, zero crossing detector.

open loop configuration of op-amp may increase the distortion as well as clipping of o/p signal. Due to this reasons the o/p switches b/w +ve & -ve saturation levels

* Closed loop op-Amp :-

Closed loop means there is a blw the o/p and the i/p terminals through the devices In this we have +ve feedback and -ve feedback.

* The gain of the op-Amp is very high in many application Due to that gain the opamp becomes unstable. Gain may be reduced to any desired value through the use of negative feedback.

* If the signal is fed back to opposite polarity (or) out of phase by 180° w.r.t the i/p signal, the feedback is called negative feedback.

* An op.amp with -ve f/b has a self correcting ability against any change in o/p voltage caused by change in environmental conditions.

* Negative f/b is also called as degenerative f/b because when used it reduces the o/p voltage amplitude and in turn reduces the voltage gain.

* If the signal fedback in phase with the i/p signal the f/b is called +ve f/b. It is called as regenerative (or) f/b.

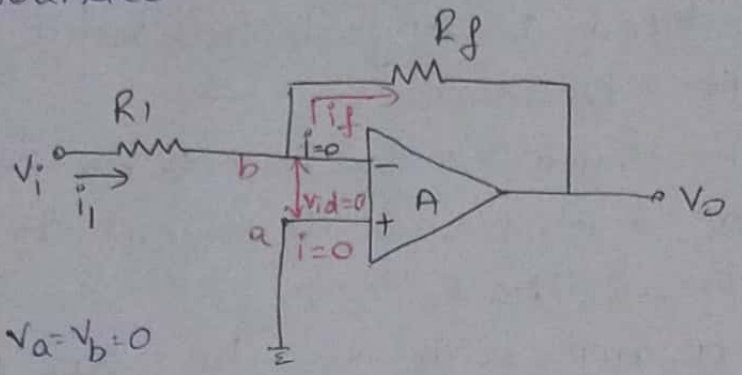
* When -ve f/b is used in Amplifier then it stabilizes (or) reduces the gain, increases the B.W and changes the i/p and o/p resistances.

- It decreases the distortion.
- It reduces the offset of i
- It reduces the effect of i/p offset voltage at the o/p.

* Inverting Amplifier :-

The o/p voltage is fed back to inverting i/p terminal through R_f feedback resistance.

* The i/p signal V_i is applied to the inverting i/p terminal through R_1, i/p resistance & non-inverting i/p terminal of op-amp is grounded.



Analysis:-

Assume ideal op-Amp $V_d = 0$

from virtual Ground $V_a = V_b = 0$

Apply KVL at node a, we have

$$\frac{V_i - V_a}{R_1} = \frac{V_a - V_o}{R_f}$$

V_a voltage at node 'a' is zero

$$V_a = 0$$

$$\frac{V_i}{R_1} = \frac{-V_o}{R_f}$$

$$\boxed{V_o = -\frac{R_f}{R_1} \cdot V_i}$$

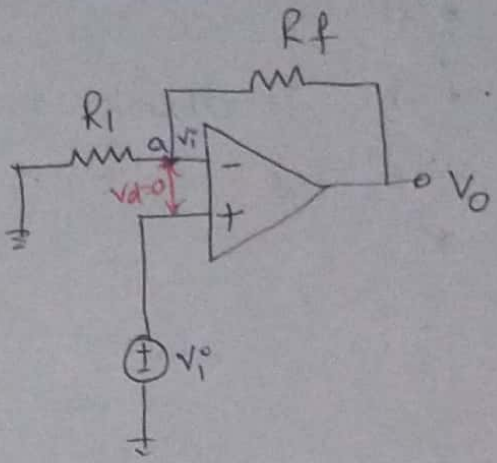
* The -ve sign indicates a phase shift of 180° blw V_i & V_o. the value of R_1 should be large to avoid loading effect.

A load resistor R_L is connected at o/p to avoid loading effect

* Non-Inverting Amplifier :-

If a signal applied to non-inverting i/p terminal & feedback given through the feedback resistance, the ckt amplifies without inverting the i/p signal such ckt is called non-inverting Amplifier.

* This is also called as negative feedback system as o/p is being feedback to inverting i/p terminal.



• As differential voltage $V_d = 0$ at i/p terminal voltage at node 'a' is $V_a = V_i$ (By virtual ground)

R_f & R_1 from potential divider.

Voltage at node a.

$$V_a = V_i = \frac{R_1}{R_1 + R_f} \cdot V_o$$

$$\frac{V_o}{V_i} = \frac{R_1 + R_f}{R_1} \Rightarrow \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

Gain of non-inverting amplifier.

$$A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_1}$$

* The gain to be adjusted to unity by proper selection of resistors R_f & R_1. As compared to inverting amplifier the i/p resistance of non inverting op amp is large as op-Amp draws negligible current from signal source.

* Voltage follower :- (or) Buffer Amplifier.

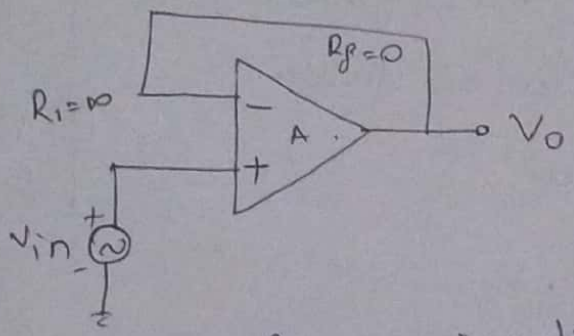
* In voltage follower the o/p voltage follows the i/p voltage i.e $V_{out} = V_{in}$. The o/p voltage is same as i/p voltage both in magnitude & phase.

* This offers the unity gain because of its high i/p impedance and low o/p impedance.

* It is a special case of non-inverting amplifier.

* The feedback resistance $R_f = 0$ and $R_i = \infty$ we get voltage follower ckt.

*



* feedback gain of non inverting Amplifier is

$$A_f = 1 + \frac{R_f}{R_1}$$

But in voltage follower $R_1 = \infty$, $R_f = 0$.

$$A_f = 1 + \frac{0}{\infty} \Rightarrow \boxed{A_f = 1} \Rightarrow A_f = \frac{V_o}{V_{in}} = 1$$

* Thus voltage follower used as buffer for impedance matching (i.e) to connect high impedance source to low impedance load.

UNIT-II

* An Op-Amp forms the basic building blocks of linear & non-linear analog systems.

* Linear ckts: output signal varies with the input signal in linear manner.

Ex: Adder, subtractor, voltage-to-current converter, current to voltage converter, power amplifier etc.,

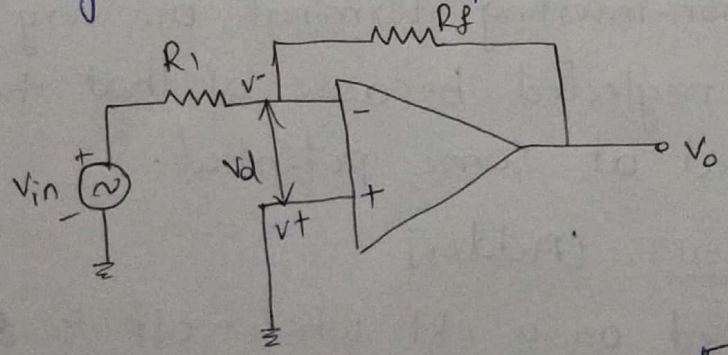
* Non-Linear ckts:- output signal varies with the input signal in non linear manner.

Ex:- Rectifier, peak detector, clipper, clamper, sample & hold ckt, log & anti log amplifier, Multiplier and divider etc.

* Concept of virtual ground:-

* Op-Amp of open loop gain is very large 10^5 to 10^6.

* Consider inverting amplifier, the input is given to the inverting terminal of op-amp. The -ve f/b is considered.



Assume open loop gain $A_{OL} = 10^5$

Consider $V_o = 10$ [Because due to -ve f/b the o/p voltage is less saturates]

$$V_{out} = A V_d$$

$$10 = 10^5 V_d$$

$$V_d = 10\ \mu V$$

The V_d is less it can be similar to zero.

$$V_d = 0V$$

$V^+ - V^- = 10\mu V$

$V^+ - V^- = 0\,V$

$\boxed{V^+ = V^-}$

∴ It means that the inverting and non-inverting input terminal are at same potential or it is called as virtual short blw the inverting and non-inverting terminal

* That means the two terminals are not actually short circuited but they are virtually short circuited. The voltage at one terminal appears exactly same at the other terminal.

$V^+ = 0$ & $V^- = 0$.

V^- is not actually grounded but it will acts as virtual ground.

* This -ve f/b will ensure that the difference b/w inverting and non-inverting terminal are very small and it can be neglected because of that two terminals can be considered at same potential.

* Summing Amplifier :- [Adder].

• Op-Amp designed as a ckt whose o/p is sum of several i/p signals such ckt is called as summing Amplifier.

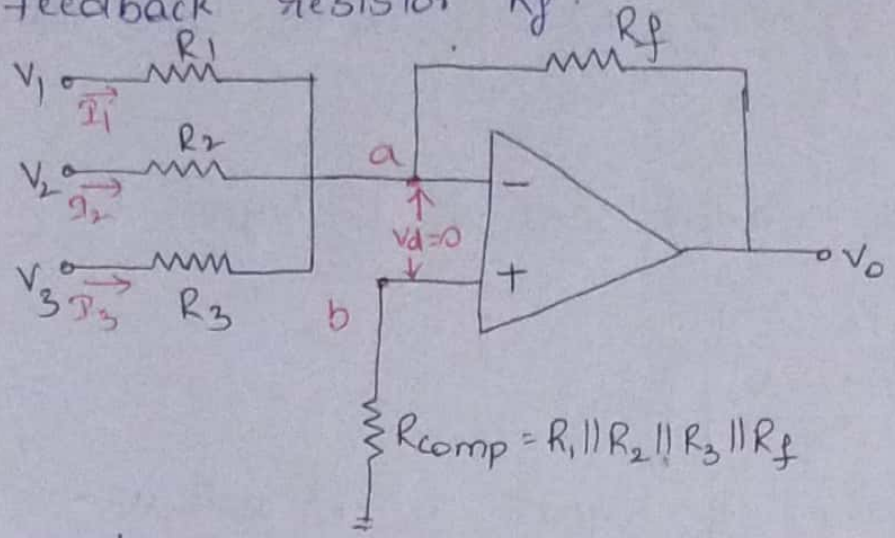
* Based on the i/p's applied it can be classified in two types.

i) Inverting summer

ii) Non-Inverting summer.

* Inverting Summer :-

- A Summing amplifier comprise of three input voltages V_1, V_2 & V_3. Three i/p resistance R_1, R_2 & R_3 and feedback resistor R_f.



* voltage at node a is zero as non-inverting i/p terminal is grounded.

from virtual ground concept $V_b = V_a = 0$.

Apply KCL at node 'a'

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = \frac{V_a - V_o}{R_f}.$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_o}{R_f} \quad [\because V_a = 0]$$

$$\boxed{V_o = -\left[\frac{R_f}{R_1} V_1 + \frac{R_f}{R_2} V_2 + \frac{R_f}{R_3} V_3\right].}$$

Thus the o/p is an inverted, weighted sum of i/p's

for $R_1 = R_2 = R_3 = R_f$.

$$\boxed{V_o = -[V_1 + V_2 + V_3]}$$

Suppose $R_1 \neq R_2 \neq R_3$ then $\frac{R_f}{R_1} \neq \frac{R_f}{R_2} \neq \frac{R_f}{R_3}$

* In this case along with addition we can also perform scaling operation.

$$V_{out} = -[AV_1 + BV_2 + CV_3]$$

$A = \frac{R_f}{R_1}$, $B = \frac{R_f}{R_2}$, $C = \frac{R_f}{R_3}$ ∴ A, B, C are scaling factor.

* The o/p V_o is inverted sum of i/p signals for

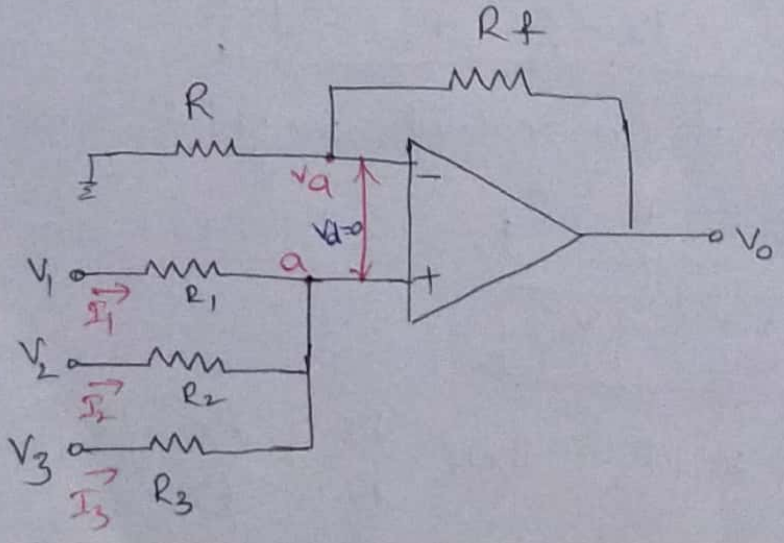
$$R_1 = R_2 = R_3 = 3R_f.$$

$$V_o = -\left[\frac{V_1 + V_2 + V_3}{3}\right]$$

o/p is average of i/p signals. So ckt acts as an average.

* Applications
  - Summing, Scaling, Averaging
  - Providing Dc offset.
  - Digital to Analog converters.

* Non-Inverting Summing Amplifier: (Adder)
  - A summer that gives non-inverting sum is called non-inverting summing amplifier. The i/p are applied to the non-inverting terminal of the op-amp:



* Voltage at non-inverting terminal is V_a.
From virtual ground concept voltage at inverting terminal is V_a.

Apply KCL at node a

$$\frac{V_1 - V_a}{R_1} + \frac{V_2 - V_a}{R_2} + \frac{V_3 - V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} - \frac{V_a}{R_1} + \frac{V_2}{R_2} - \frac{V_a}{R_2} + \frac{V_3}{R_3} - \frac{V_a}{R_3} = 0$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = V_a\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right]$$

$$V_a = \frac{\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}}{\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}}$$

* Gain of non-inverting amplifier with R_f & R given as

$$A_{CL} = \frac{V_o}{V_a} = \left[1 + \frac{R_f}{R}\right]$$

$$V_o = \left[1 + \frac{R_f}{R}\right] V_a$$

Sub. value of V_o, we get

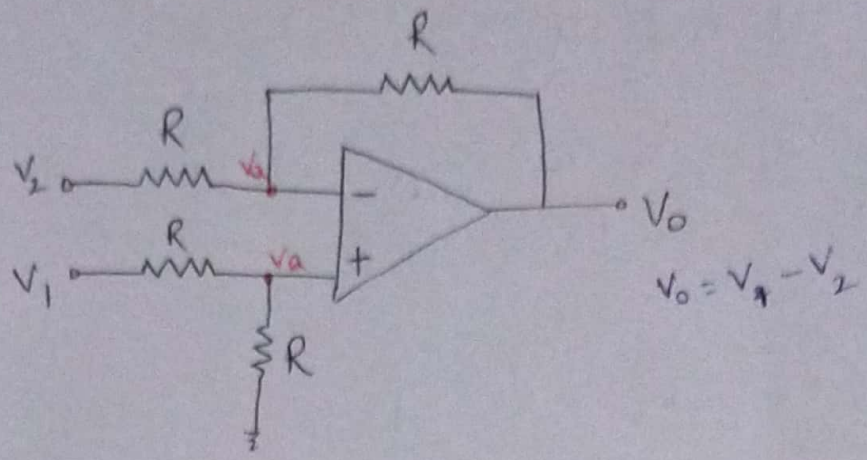
$$V_o = \left[1 + \frac{R_f}{R_1}\right] \frac{\left[\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3}\right]}{\left[\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3}\right]}$$

The o/p is the ~~non~~ weighted sum non-inverted weighted sum of i/p's ∴ for $R_1 = R_2 = R_3 = R = \frac{R_f}{2}$ then

$$V_o = V_1 + V_2 + V_3.$$

* Subtractor :-

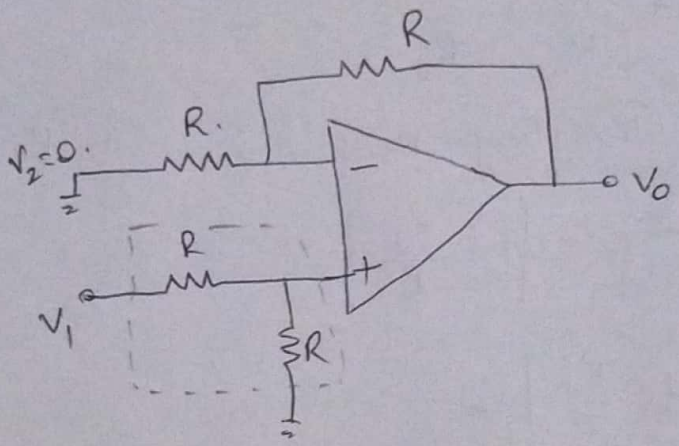
The basic differential amplifier used as subtractor, Producing difference of two input signals.



Subtractor.

If all the resistors are equal in value, then o/p voltage derived by using superposition principle.

- V_{o_1} - output due to V_1 alone with $V_2 = 0$.



~~At V_1 Apply~~ voltage divider is formed $V_1 \times \frac{R_2}{R_1+R}$

$$V_1 \times \frac{R}{2R} \Rightarrow \frac{V_1}{2}$$

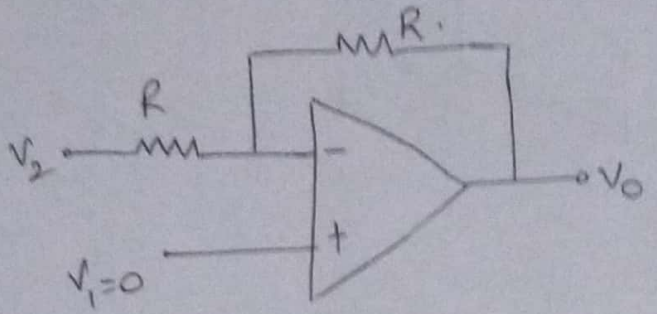
The ckt turns into non-inverting amplifier with i/p voltage $V_i = V_1/2$ applied at non-inverting terminal.

∴ output voltage $V_{o_1} = \frac{V_1}{2}\left[1 + \frac{R}{R}\right]$

$$\boxed{V_{o_1} = V_1}$$

Gain of non-inv is
$A_{CL} = \frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right]$
$V_o = V_i\left[1 + \frac{R_f}{R_1}\right]$

* V_{o_2} - o/p due to V_2 alone with $V_1 = 0$.



The ckt turns into inverting amplifier with i/p voltage $V_2 = V_i$ applied at inverting terminal.

∴ output voltage

$$V_{o_2} = -V_2.$$

Gain of inverting amp is
$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1}$
$V_o = -\frac{R_f}{R_1} V_i$
$V_o = -\frac{R}{R} \cdot V_2$

* The output voltage due to the both inputs

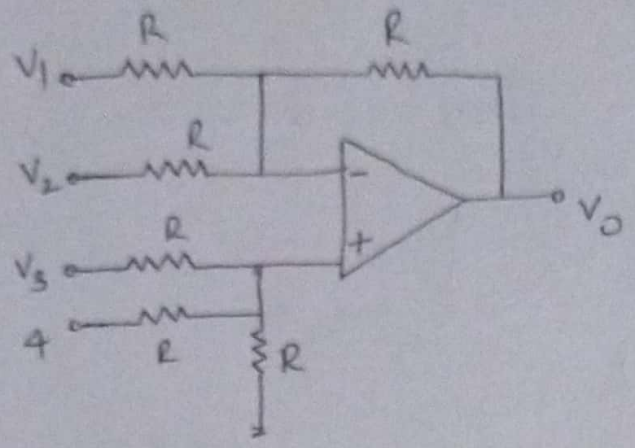
$$V_o = V_{o_1} + V_{o_2}.$$

∴ $V_{o_1} = V_1$; $V_{o_2} = -V_2$

$$\boxed{V_o = V_1 - V_2.}$$

* Adder - Subtractor :-

A single op-amp ckt can be used to perform addition and subtraction simulation



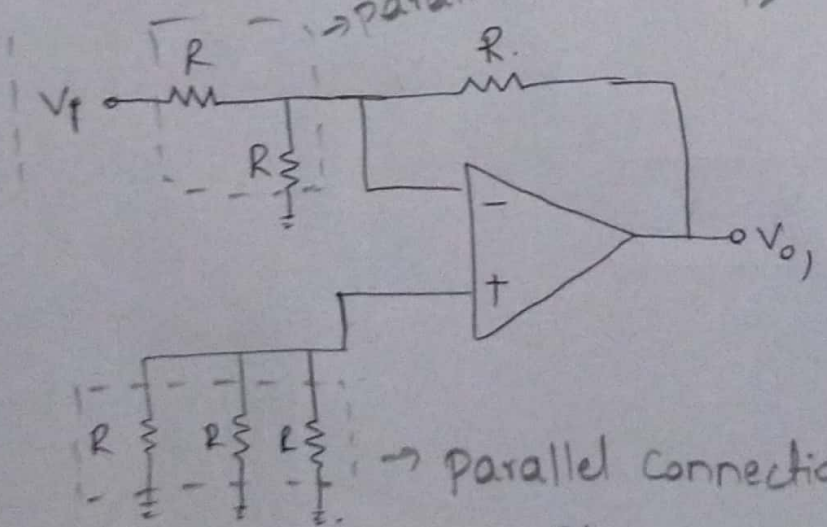
* The o/p voltage V_o can be obtained by using superposition principle.

V_{o_1} - o/p voltage due to V_1 alone with $V_2 = V_3 = V_4 = 0$.

V_{o_2} - o/p voltage due to V_2 alone with $V_1 = V_3 = V_4 = 0$.

V_{o_3} - o/p voltage due to V_3 alone with $V_1 = V_2 = V_4 = 0$

V_{o_4} - o/p voltage due to V_4 alone with $V_1 = V_2 = V_3 = 0$



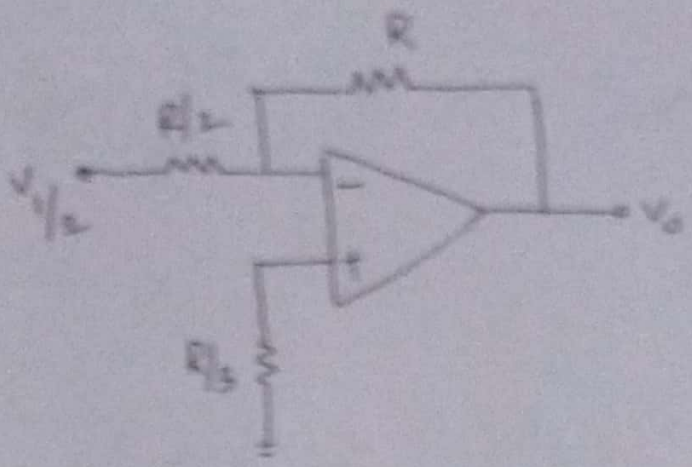
single voltage V_1 is shared by 2 resistors R & R

The voltage divider is forming

$V_1 \times \frac{R}{R+R}$

$= V_1 \times \frac{R}{2R}$

$= V_1/2$



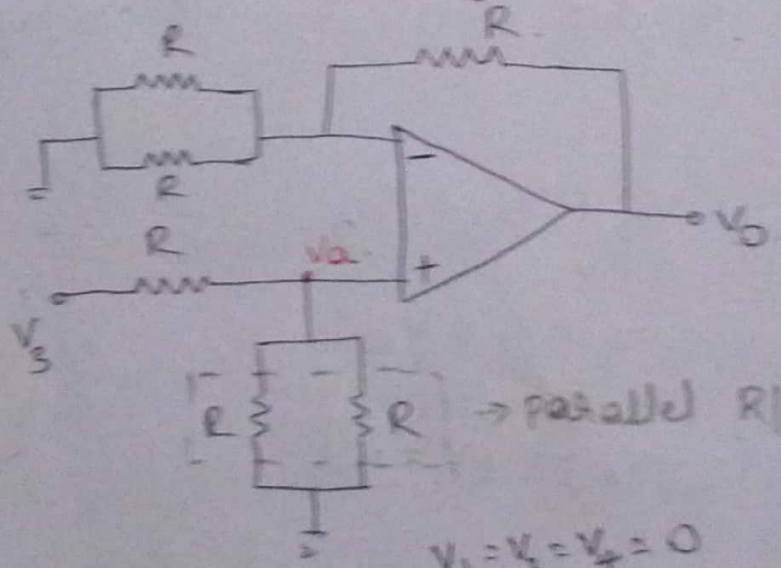
the ckt is forming Inverting amplifier with i/p voltage $V_{o_1} = -\frac{R}{R/2} \cdot \frac{V_1}{2} = -V_1$

$$\boxed{V_{o_1} = -V_1}$$

Similarly the output voltage V_{o_2} due to V_2 alone is

$$\boxed{V_{o_2} = -V_2}$$

- Now the o/p voltage V_{o_3} due to the i/p voltage signal V_3 alone supplied to the non-inverting terminal can be found by setting V_1, V_2 & V_4 equal to zero.



→ parallel $R/2$

$V_1 = V_2 = V_4 = 0$

$V_{o_3} = V_3$.

Single voltage V_3 is applied

Voltage divider is formed

$V_a = \frac{R/2}{R + R/2} \cdot V_3$

$V_a = V_3/2$

$$V_a = \left(\frac{R||2}{R+R||2}\right) V_3 \Rightarrow V_a = \left(\frac{R||1}{3R||1}\right) V_3$$

$$V_a = \frac{V_3}{3}$$

The o/p voltage V_{o3} due to V_3 alone is

The ckt forms non-inv amp^r $A = \frac{V_o}{V_i} = \left[1 + \frac{R_f}{R}\right]$

$$V_o = \left[1 + \frac{R_f}{R}\right] V_i$$

$$V_{o3} = \left[1 + \frac{R}{R||2}\right] V_a$$

$$V_{o3} = \left[1 + \frac{R}{R||2}\right] \cdot \frac{V_3}{3} \Rightarrow V_{o3} = 3\left[\frac{V_3}{3}\right]$$

$$\boxed{V_{o3} = V_3}$$

Similarly $V_{o4} = \left[1 + \frac{R}{R||2}\right] V_a = 3\left[\frac{V_4}{3}\right]$

$$V_{o4} = V_4$$

o/p voltage V_o due to all four i/p voltages given by

$$V_o = V_{o1} + V_{o2} + V_{o3} + V_{o4}$$

$$= -V_1 - V_2 + V_3 + V_4$$

$$V_o = [V_3 + V_4] - [V_1 + V_2]$$

Thus ckt form adder - subtractor

* Instrumentation Amplifier:-

* The purpose of Instrumentation Amplifier is to amplify very low voltage signal.
* Basically the instrumentation uses transducers. The transducers converts one form of energy into another form of energy may be in the form of electrical signals or non-electrical.
* To measure temperature, humidity etc the transducers converts their physical quantity into electrical form.
* Instrumentation amplifier is one kind of differential Amplifier with very high gain and high CMRR.
* These amplifiers are used in industrial and consumer applications, one is required to measure and control physical quantities.

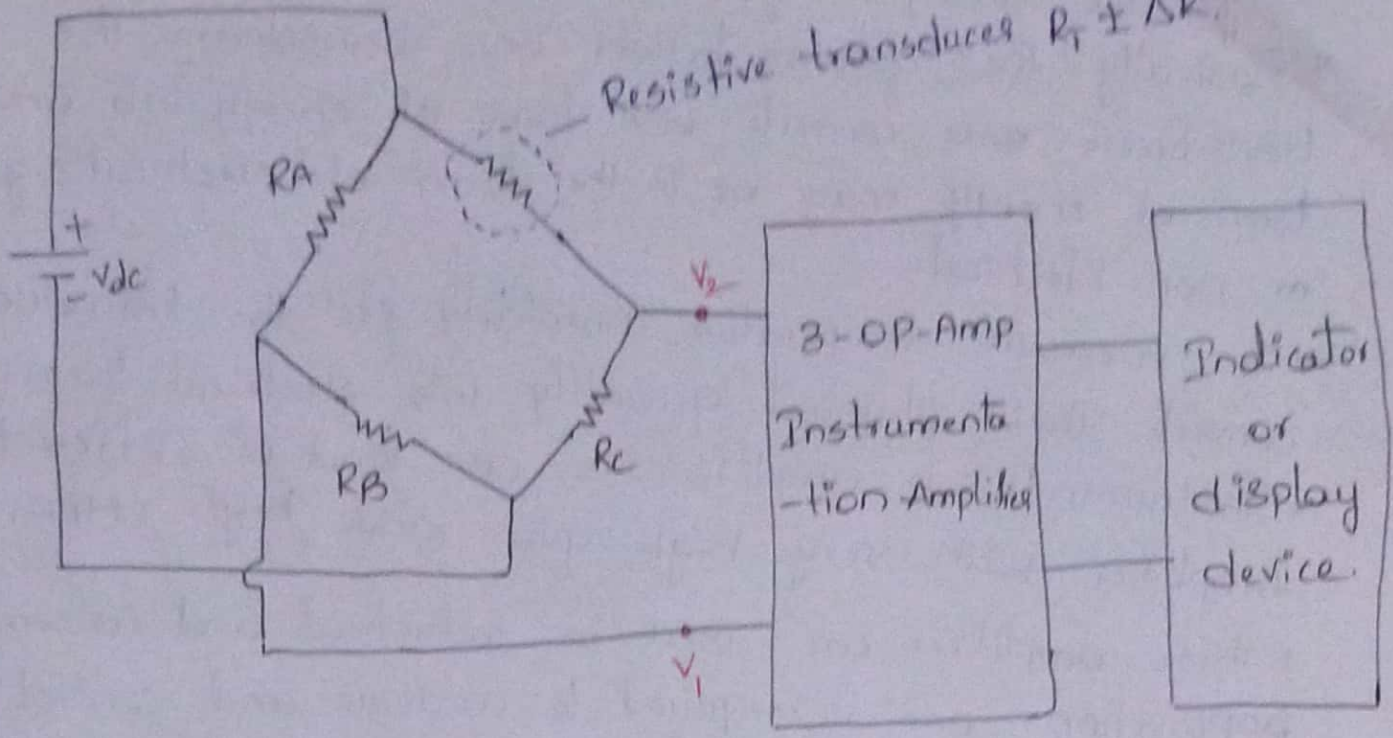
Ex:- Control of temperature, humidity, light intensity, water flow etc.

* These physical quantities are usually measured with the help of transducers.
* The output of transducers has to be amplified so that it can drive the indicator or display characteristics.

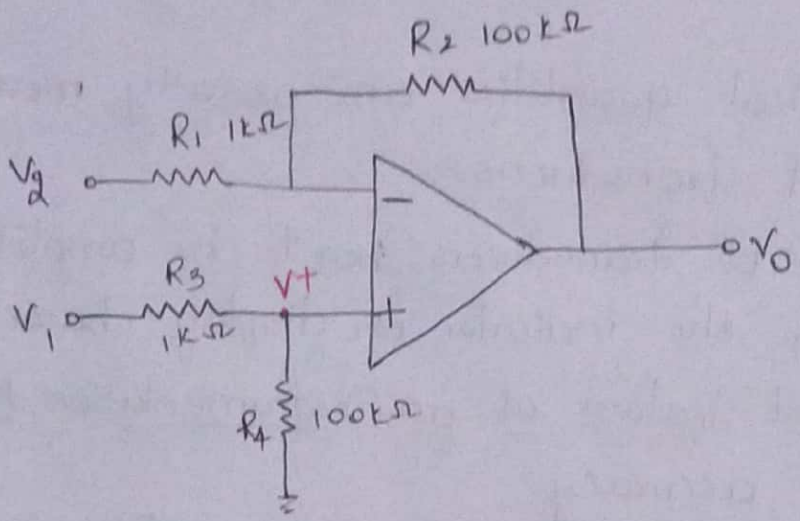
* The important features of an Instrumentation Amplifier:-

- High gain accuracy.
- High gain stability at low temperature coefficients.
- High CMRR.
- High slew rate.
- low Dc offset.
- High i/p impedance.
- low o/p impedance.

* Monolithic (single chip) instrumentation amplifiers are also available commercially such as AD521, AD524, AD620, AD624 by Analog devices.



Instrumentation Amplifier using transducer bridge



Differential Amplifier using single op Amp.

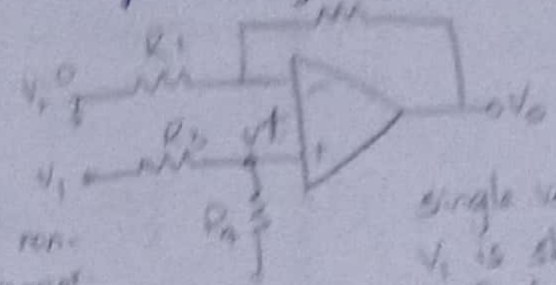
- for basic differential amplifier the o/p voltage V_o is given by

$$V_o = V_{o_1} + V_{o_2}$$ [By superposition theorem].

V_{o_1} → output for V_1 alone connected with V_2 is grounded.

V_{o_2} → output for V_2 alone connected with V_1 is grounded.

$$V^+ = \left[\frac{R_4}{R_3+R_4}\right] V_1 \quad \text{[from voltage divider]}$$



single voltage V_1 is shared to R_3 & R_4 it forms voltage divider

$$V_{o_1} = \left[1 + \frac{R_2}{R_1}\right] V^+ \quad \left\{\text{Gain of non-inverting amp}^r = \frac{V_o}{V_i} = \left[1+\frac{R_f}{R_1}\right] \Rightarrow V_o = \left(1+\frac{R_f}{R_1}\right) V_i\right\}$$

$$V_{o_1} = \left(1 + \frac{R_2}{R_1}\right)\left[\frac{R_4}{R_3+R_4}\right] V_1$$

$$V_{o_1} = \left[1 + \frac{R_2}{R_1}\right]\left[\frac{1}{1+\frac{R_3}{R_4}}\right] V_1 \quad -(1)$$

$$V_{o_2} = -\frac{R_2}{R_1} V_2 \quad -(2) \left[\because \text{Gain of inverting amp}^r = \frac{V_o}{V_i} = -\frac{R_f}{R_1} \Rightarrow V_o = -\frac{R_f}{R_1} V_i\right]$$

$$V_o = V_{o_1} + V_{o_2}$$

$$V_o = \left[1 + \frac{R_2}{R_1}\right]\left[\frac{1}{1+\frac{R_3}{R_4}}\right] V_1 - \left[\frac{R_2}{R_1}\right] V_2$$

$R_3 = R_1$

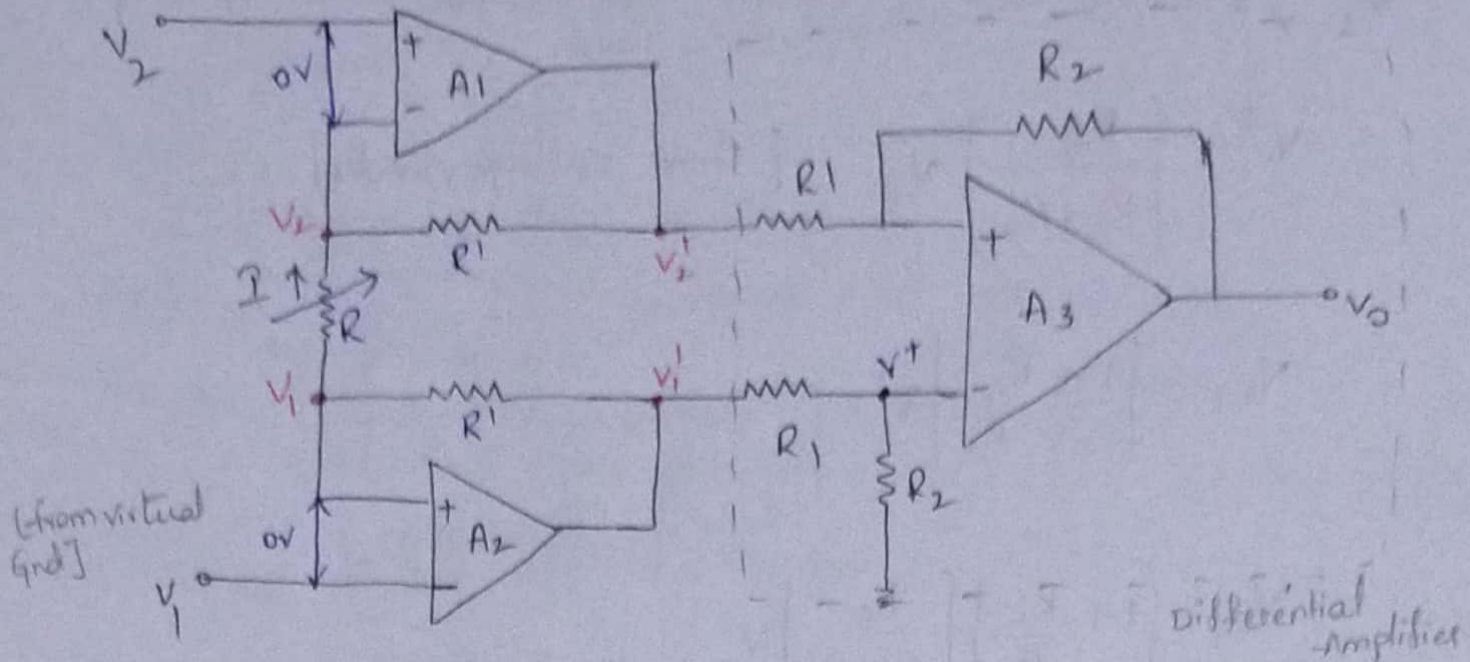
$R_4 = R_2$

$$= \left(\frac{R_1+R_2}{R_1}\right)\left[\frac{R_2}{R_2+R_1}\right] V_1 - \left(\frac{R_2}{R_1}\right) V_2$$

$$= \frac{R_2}{R_1} V_1 - \frac{R_2}{R_1} V_2$$

$$\boxed{V_o = \frac{R_2}{R_1}\left[V_1 - V_2\right]}$$

output voltage of a differential amplifier.



An Improved Instrumentation Amplifier (or) Triple Op-Amp Instrumentation Amplifier.

*In the basic differential Amplifier, source V_1 offers an i/p impedance $R_i = (R_3 + R_4)$ [$\because 100+1 = 101 k\Omega$] and impedance offered by V_2 is $1 k\Omega$.

* The low i/p impedance loads signal source heavily. Hence high resistance buffer is used proceding each i/p to avoid the loading effect.

*The op-Amps A_1 & A_2 have differential i/p voltage $V_d = 0$ for $V_1 = V_2$. Under Common-mode condition, voltage across R. i.e zero $V_R = 0$ $\left[\because V_R = IR = \left(\frac{V_1 - V_2}{R}\right) R\right]$

*As no current flows through R & R' the non-Inverting amplifier A_1 acts as voltage follower so its o/p $\boxed{V_2 = V_2'}$

*Similarly op-Amp A_2 acts as voltage follower with o/p $\boxed{V_1' = V_1}$

* But if $V_1 \neq V_2$, current flows through R & R' and $(V_2' - V_1) > [V_2 - V_1']$ thus ckt offers high gain & CMRR when compared to single op-Amp.

Analysis :-

calculation of o/p voltage

Voltage at (+) terminal of op-Amp as

$$V^+ = \left[\frac{R_2}{R_1 + R_2}\right] V_1' \quad ; \quad V_{o_1} = \left[1 + \frac{R_2}{R_1}\right] V^+$$

(for non-Inverting Amp)

Using super position theorem

$$V_o = V_{o_1} + V_{o_2}$$

$$V_{o_2} = -\frac{R_2}{R_1} V_2' \quad \text{(for Inverting Amp)}$$

$$V_o = \left[1 + \frac{R_2}{R_1}\right] V^+ - \frac{R_2}{R_1} V_2'$$

$$= \left(1 + \frac{R_2}{R_1}\right)\left[\frac{R_2}{R_1 + R_2}\right] V_1' - \frac{R_2}{R_1} V_2'$$

$$= \left(\frac{R_1 + R_2}{R_1}\right)\left(\frac{R_2}{R_1 + R_2}\right) V_1' - \frac{R_2}{R_1} V_2'$$

$$V_o = \frac{R_2}{R_1} V_1' - \frac{R_2}{R_1} V_2' \Rightarrow \boxed{V_o = \frac{R_2}{R_1}\left[V_1' - V_2'\right]}$$

* Since no current flows at i/p side of op-Amp. Current I flowing through R is $I = \left[\frac{V_1 - V_2}{R}\right]$ and passes through R'

$$V_1' = IR' + V_1 \Rightarrow \frac{R'}{R}\left[V_1 - V_2\right] + V_1$$

$V_3' = -IR' + V_3 \Rightarrow -\frac{R'}{R}(V_1 - V_3) + V_3$

Sub the values of V_1' and V_2' in V_0 the o/p voltage

$$V_0 = \frac{R_2}{R_1}\left[\frac{R'}{R}(V_1 - V_2) + V_1 + \frac{R'}{R}(V_1 - V_2) - V_2\right]$$

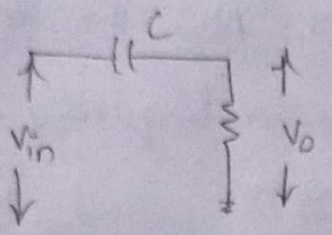
$$V_0 = \frac{R_2}{R_1}\left[\frac{2R'}{R}(V_1 - V_2) + (V_1 - V_2)\right]$$

$$\boxed{V_0 = \frac{R_2}{R_1}(V_1 - V_2)\left[1 + \frac{2R'}{R}\right]}$$

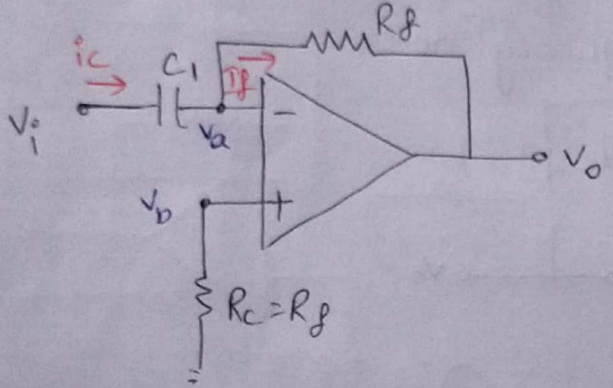
* The difference gain of instrumentational amplifier can be varied by replacing the resistance R by potentiometer.
* The differential instrumentation amplifier using transducer bridge the ckt uses resistive transducers whose resistance changes as function of physical quantity to be measured.
* The bridge is initially balanced by dc supply voltage Vdc such that $V_1 = V_2$.
As the physical quantity changes the resistance R_T of transducers also changes causing an unbalance in bridge $V_1 \neq V_2$
* This differential voltage now gets amplified by three OP-Amp differential instrumentation amplifier with
* The applications of instrumentation amplifier with transducer include temperature indicator, temperature controller, light intensity meter etc.

*Differentiator [HPF] :-

- The differentiator circuit performs the mathematical operation of differentiation i.e output waveform is derivative of input waveform. This operation is very useful to find the rate at which the signal varies with time.
- The differentiator circuit which doesnot use any active device is called active differentiator.



*The differentiator ckt at which active devices like op-amp -transistor is called active differentiator.



Apply KCL

$$I_c = I_f \Rightarrow C\frac{dv_c}{dt} = \frac{0 - V_o}{R_f}$$ [∵ from virtual gnd Concept $V_a = 0$V].

$$\boxed{V_o = -R_f C \frac{dv_{in}}{dt}}$$

$$V_o = \frac{-R_f}{X_c} \cdot V_{in}$$ [X_c - reactance ; $X_c = \frac{1}{2\pi f_c}$]

$$\frac{V_o}{V_{in}} = -R_f 2\pi f \cdot C$$

$$\left|\frac{V_o}{V_i}\right| = 2\pi f \cdot C R_f$$

$f_a = \frac{1}{2\pi R_f C}$.

$|A| = \frac{f}{f_a}$. [At f_a the gain is 0dB].

At $f = f_a$, $|A| = 1$, i.e 0d.B & gain increases at rate of +20 dB/dec.

* Thus at high frequencies, differentiator ~~becomes~~ becomes unstable & breaks into oscillations. Also the impedance [$X_C = \frac{1}{j2\pi f C_1}$] decreases with increases in frequency and makes ckt sensitive to high frequency noise.

* Frequency response of ideal Differentiator :-

Let us consider o/p expression

$$V_o(t) = -R_f C_1 \frac{d}{dt} V_i(t)$$

Apply L.T on both sides we get.

$$V_o(s) = -sR_f C_1 V_i(s)$$

$$\frac{V_o(s)}{V_i(s)} = -sR_f C_1$$

To get freq response $s = j\omega$.

$$\frac{V_o(j\omega)}{V_i(j\omega)} = -j\omega R_f C_1$$

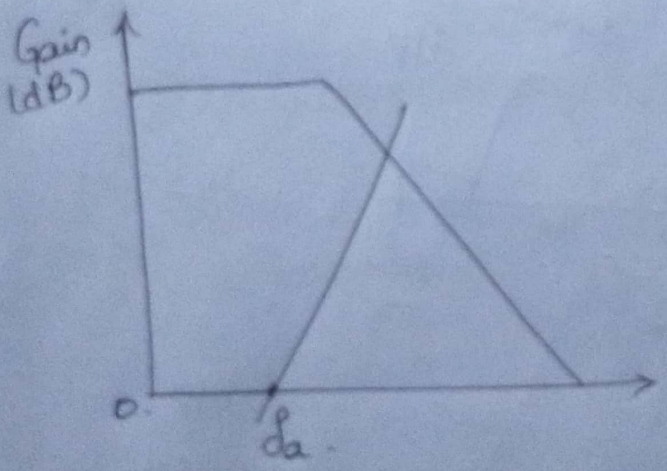
ω is angular frequency $= 2\pi f$

$$|A| = \frac{V_o(j\omega)}{V_i(j\omega)} = |-j\omega R_f C_1| = \sqrt{0^2 + (\omega R_f C_1)^2} = \omega R_f C_1$$

$$|A| = 2\pi f R_f C_1$$

let $f_a = \frac{1}{2\pi R_f C_1}$

$V_o(s) = -R$

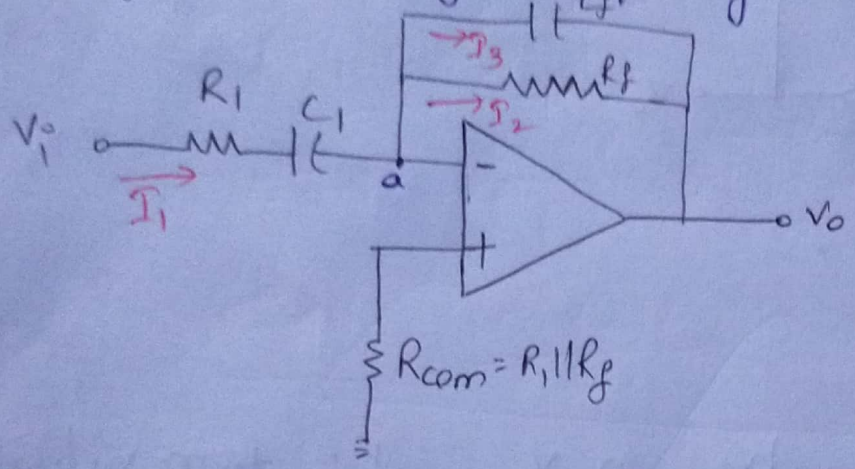


* As freq ↑ses the gain of differentiator also increases
* But the gain of differentiator cannot ↑sey indefinitely & the gain is restricted by the open loop gain of op-Amp.

* So the max. gain attainted by the differentiator is the intersection point of differentiator and the open loop gain of op-amp.

* Practical Differentiator :-

The practical differentiator eliminates the problem of stability and high frequency noise.



* By the feedback capacitance Cf we can improve the stability at the output of op-amp.

* Apply KCL at node 'a'

$$I_1 = I_2 + I_3$$

$$\frac{V_{in} - V_a}{R + \frac{1}{sC_1}} = \frac{V_a - V_o}{R_f} + C_f \frac{d}{dt}(V_a - V_o)$$

$\therefore V_a = 0$ [from virtual ground concept]

$$\frac{V_{in}(t)}{R_1 + \frac{1}{sC_1}} = \frac{-V_o(t)}{R_f} - C_f \frac{d}{dt} V_o(t) \quad (2)$$

Apply laplace Transform on both sides.

$$\frac{V_{in}(s)}{R_1 + \frac{1}{sC_1}} = \frac{-V_o(s)}{R_f} - sC_f V_o(s)$$

$$\frac{V_{in}(s)(sC_1)}{R_1 sC_1 + 1} = -V_o(s)\left[\frac{1 + sC_f R_f}{R_f}\right]$$

$$V_o(s) = \frac{-R_f sC_1}{(1+R_1 sC_1)(1+sC_f R_f)} \cdot V_{in}(s)$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_f sC_1}{(1+sR_f C_f)(1+sC_1 R_1)}$$

* Frequency Response of Practical differentiator:-

$$\frac{V_o(s)}{V_i(s)} = \frac{-sR_f C_1}{(1+sR_f C_f)(1+sC_1 R_1)}$$

i) for $R_f C_f = R_1 C_1$ we get.

$$\frac{V_o(s)}{V_i(s)} = \frac{-sR_f C_1}{(1+sR_1 C_1)^2}$$

$s = j\omega$.

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j\omega R_f C_1}{(1+j\omega R_1 C_1)^2} \quad [\because \omega = 2\pi f]$$

Differentiator :-

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j2\pi f R_f C_1}{(1+j2\pi f R_1 C_1)^2}$$

$$f_a = \frac{1}{2\pi R_f C_1}, \quad f_b = \frac{1}{2\pi R_1 C_1}$$

$$\frac{V_o(j\omega)}{V_i(j\omega)} = \frac{-j(f/f_a)}{(1+jf/f_b)^2}$$

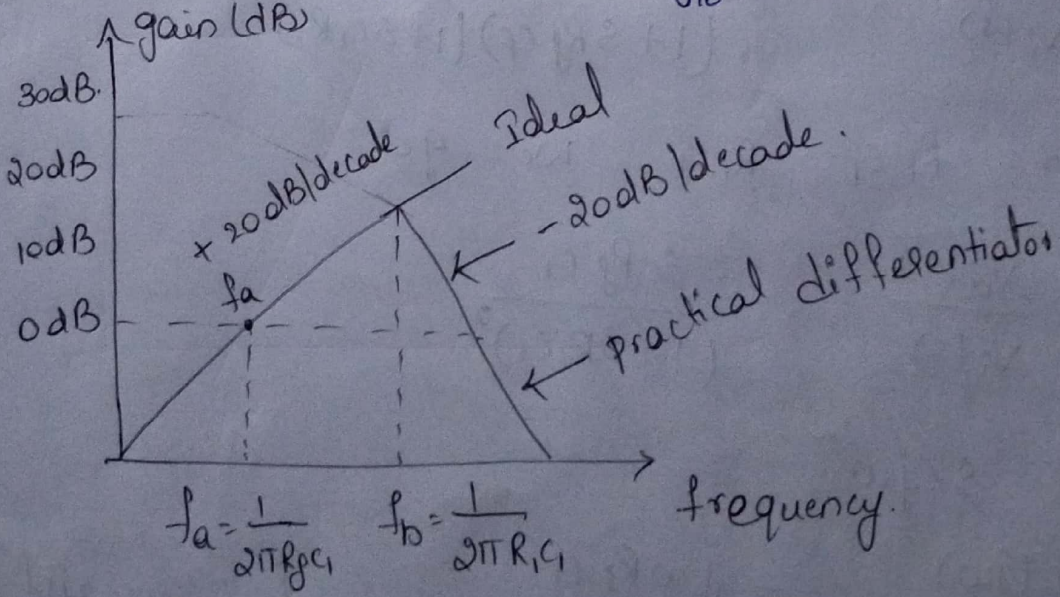
Magnitude

$$|A| = \left|\frac{V_o(j\omega)}{V_i(j\omega)}\right| = \frac{f/f_a}{\sqrt{1+(f/f_b)^2}}$$

i, Consider $f_a = 10f$, $f_b = 100f$, $f = 10f$

$$|A| = \frac{10f/10f}{\sqrt{1+(10f/100f)^2}} = \frac{1}{\sqrt{1+\frac{1}{100}}} = 1$$

Gain in dB $= 20\log_{10}(A) = 20\log_{10}(1) = 0$ dB.



ii,

ii, $R_f C_f >> R_1 C_1$ & $(R_f C_f)$

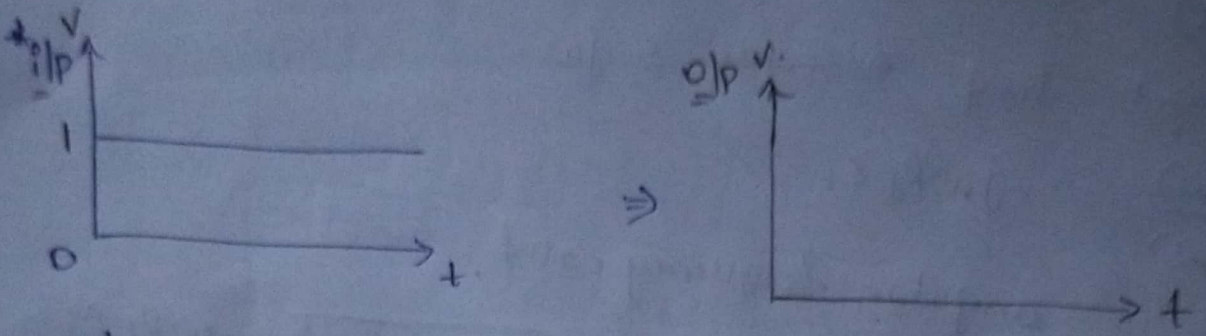
$$\frac{V_o(s)}{V_i(s)} = -s C_1 R_f$$

$$V_o(s) = -R_f C_1 s V_i(s)$$

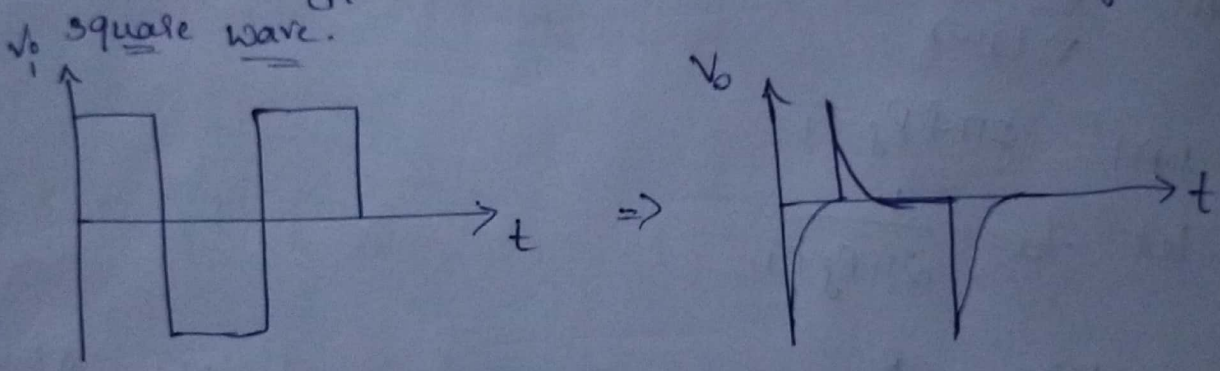
$$V_o(t) = -R_f C_1 \frac{d}{dt} V_i(t)$$

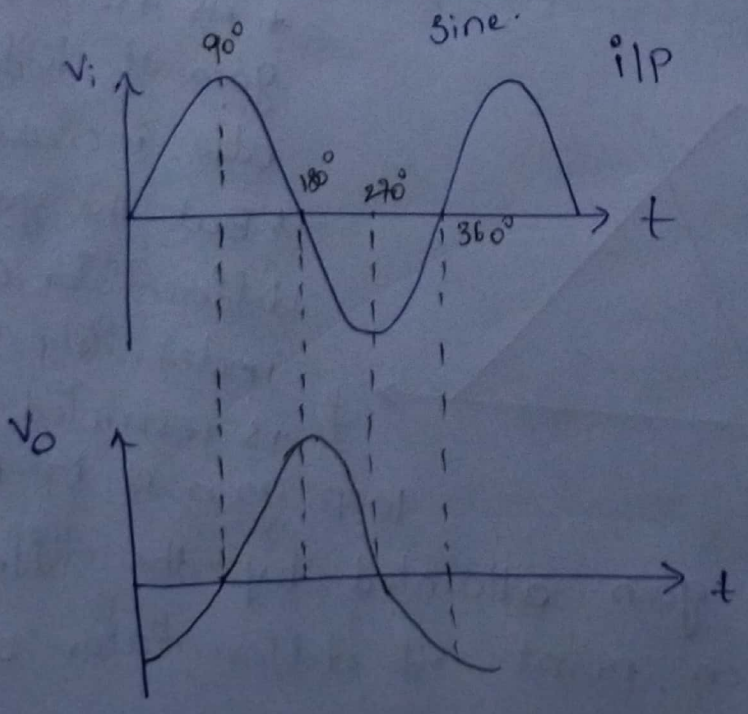
* As the frequency increases, gain increases till $f = f_b$ at rate of 20dB/decade.
After $f = f_b$ the gain decreases at the rate of -20dB/decade.

* The gain decreases as frequency increases $> f_b$.
Hence the problem of instability at high frequency get eliminated.



$\frac{d}{dt}(V_{in}) = \frac{d}{dt}(1) = 0$. The o/p of dc i/p signal.





Steps to design practical differentiator :-

i) choose f_a as the highest freq. of i/p signal $\left[f_a = \frac{1}{2\pi R_f C_1}\right]$

ii) choose C_1 to be $\leq 1\mu f$ & calculate value of R_f.

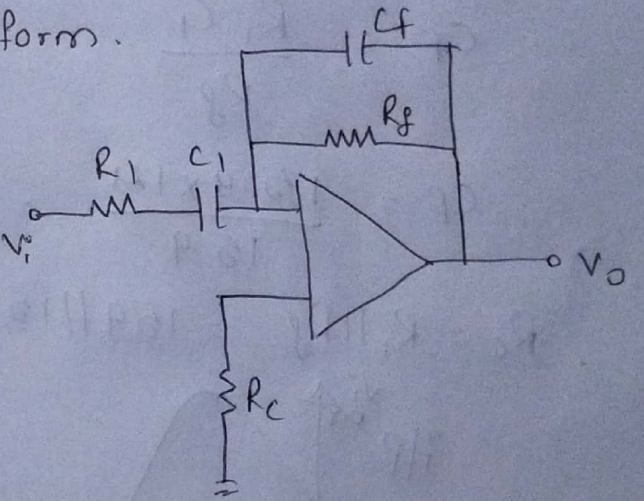
iii) choose f_b as 10 times f_a $[f_b = 10 f_a]$ $\left[f_b = \frac{1}{2\pi R_1 C_1}\right]$

iv) calculate the values of R_1 & C_f from the expression

$$R_1 C_1 = R_f C_f .$$

v) $R_{comp} = R_1 \| R_f$.

* Design a differentiator an input signal that varies in freq. from 10Hz to 1KHz If a sine wave of 1V Peak at 1kHz is applied to this differentiator. Draw its output waveform.



Given freq : 10Hz - 1kHz

$\therefore f_{max} = f_a = 1kHz$

$C_1 = 1\mu f.$

$$f_a = \frac{1}{2\pi R_f C_1}$$

$$R_f = \frac{1}{2\pi f_a C_1} \Rightarrow R_f = \frac{1}{2\pi \times 1 \times 10^3 \times 1 \times 10^{-6}}$$

$$\boxed{R_f = 159\,\Omega}$$

$$f_b = 10 f_a \Rightarrow f_b = 10 \times 1kHz.$$

$$\boxed{f_b = 10kHz.}$$

$$f_b = \frac{1}{2\pi R_1 C_1}$$

$R_1 = \frac{1}{2\pi \times 10k \times 1\mu} = 15.9\,\Omega \Rightarrow \boxed{R_1 = 15.9\,\Omega}$

$R_1 C_1 = R_f C_f$

$R_f = \frac{1}{2\pi \times 10k \times 1\mu} = 15.9\,\Omega$

$\frac{R_1 C_1}{R_f} = C_f \Rightarrow R_f = \frac{R_1 C_1}{C_f}$

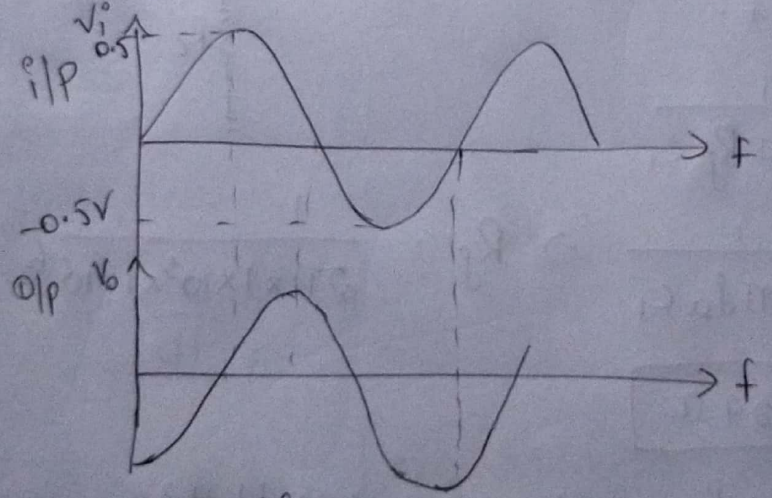
$R_f = \frac{15.9 \times 1\mu}{159}$

$R_1 C_1 = R_f C_f$

$C_f = \frac{R_1 C_1}{R_f}$

$C_f = \frac{15.9 \times 1\mu}{159} = 0.1\mu f \quad \therefore C_f = 0.1\mu f$

$R_c = R_1 \| R_f = 159 \| 15.9 = 14.45\,\Omega \quad \therefore R_c = 14.45\,\Omega$



* Application of Differentiator:-

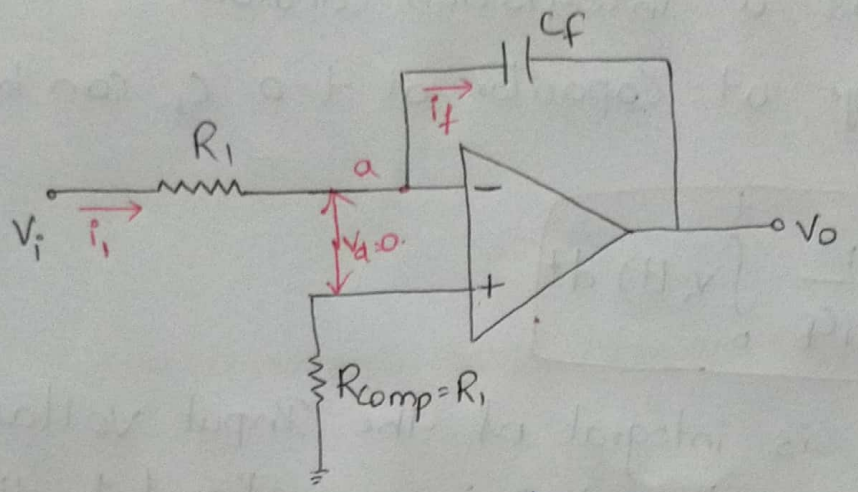
→ It can be used as wave shaping ckt

* Edge detection in FM demodulators

* Analog computers.

* Integrator :-

- It is also called Integration Amplifier.
- The output voltage is integral of input voltage then the circuit is called Integrator.
- The interchange of the resistor and capacitor of the differentiator is the integration.



*from the basic capacitor theory
The voltage developed across the capacitor and the charging current have relationship.

$$i = C\frac{dv}{dt}$$

Apply KCL at node 'a'

$$i_1 = i_f$$

$$\frac{V_i - V_a}{R_1} = C_f \frac{d}{dt}(V_a - V_o)$$

$V_a = 0$ as it is virtual ground.

$$\frac{V_i}{R_1} = C_f \frac{d}{dt}(-V_o)$$

$$\frac{d}{dt}V_o = -\frac{1}{R_1 C_f}V_i$$

Apply Integration on both side w.r.t we get

$$\int_0^t dV_o = -\frac{1}{R_1 C_f}\int_0^t V_i(t)$$

$$V_o(t) = -\frac{1}{R_1 C_f}\int_0^t V_i(t)\,dt + C_1 \qquad [C_1 = V_o(0)]$$

Where C_1 is a integration constant.

* Initial voltage at capacitor at $t=0$ C_1 can be set to zero.

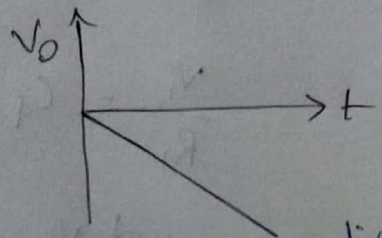
$$V_o(t) = -\frac{1}{R_1 C_f}\int_0^t V_i(t)\,dt$$

* output voltage is integral of the Input voltage.
* Thus the output voltage (V_o) is proportional to the integral of input voltage with $R_1 C_f$ as time constant of integrator.
* As negative sign indicates inverting Integrator.
* A resistance $R_{comp} = R_1$ is connected to (+) i/p terminal to minimize the effect of i/p bais current.
* A simple low pass RC circuit act as integrator when time constant is large ($\tau >> RC$). This requires large value of R and C.
* If the input voltage is constant $V_i = V$.

$$V_o = -\frac{1}{RC}\int V\,dt.$$

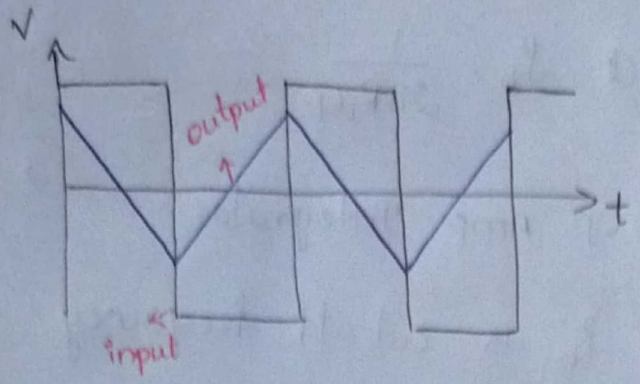
$$V_o = -\frac{Vt}{RC}.$$

i.e The output is a ramp.



output is negative going ramp for a constant i/p.

* for a square wave input we get output as triangular wave.

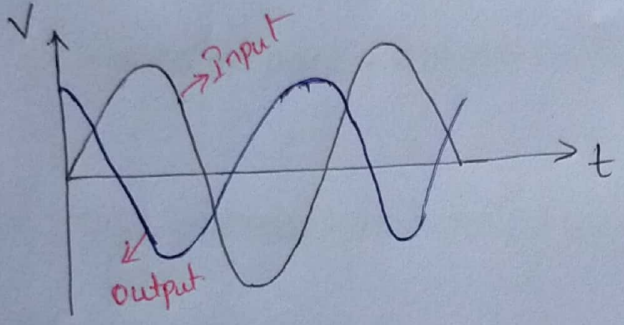


* If input is a sinusoidal signal.

$V_i = a_0 \sin \omega t$

$$V_0 = -\frac{1}{RC} \int a_0 \sin \omega t \, dt$$

$$V_0 = \frac{a_0}{\omega RC} \cos \omega t$$



* Frequency Response :-

$$V_0(t) = -\frac{1}{R_1 C_f} \int V_i(t) \, dt$$

Apply laplace Transform on both side.

$$V_0(s) = -\frac{1}{sR_1C_f} V_i(s)$$

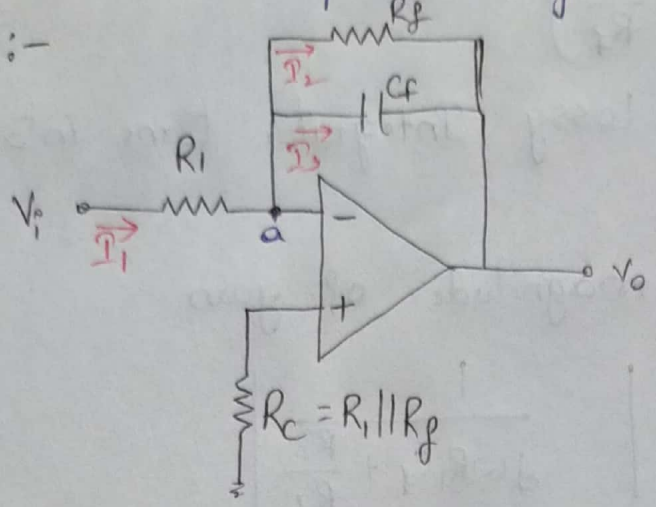
Put $s = j\omega$

$$V_0(j\omega) = -\frac{1}{j\omega R_1 C_f} V_i(j\omega)$$

$$|A| = \left| \frac{V_0(j\omega)}{V_i(j\omega)} \right| = \left| -\frac{1}{j\omega R_1 C_f} \right|$$

to $-R_f/R_1$ [$R_f = 10R_1$] providing stability and minimizing the variations in output voltage.

*Analysis :-



Apply KCL at node 'a'

$$I_1 = I_2 + I_3$$

$$\frac{V_i - V_a}{R_1} = C_f \frac{d}{dt}(V_a - V_o) + \frac{V_a - V_o}{R_f}$$

But $V_a = 0$ as it is virtual ground.

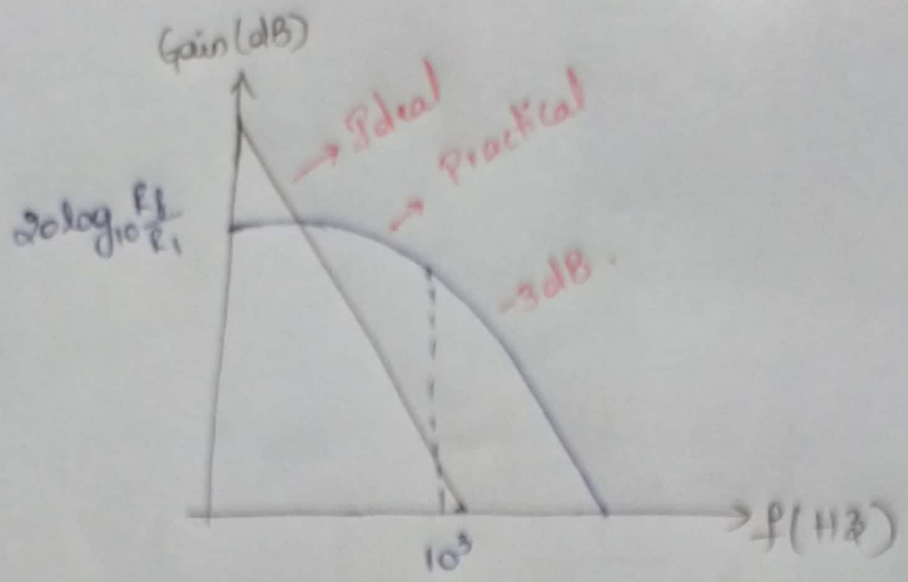
$$\frac{V_i(t)}{R_1} = -C_f \frac{dV_o(t)}{dt} - \frac{V_o(t)}{R_f}$$

Taking laplace Transform on both sides

$$\frac{V_i(s)}{R_1} = -sC_f V_o(s) - \frac{V_o(s)}{R_f}$$

$$\frac{V_i(s)}{R_1} = -V_o(s)\left[sC_f + \frac{1}{R_f}\right]$$

$$\frac{V_o(s)}{V_i(s)} = -\frac{1}{R_1}\left[\frac{1}{sC_f + \frac{1}{R_f}}\right]$$



for freq $f > f_a$ gain R_f/R_1 is constant, gain decreases at rate of -20dB/decade values of f_a, R_1C_f, R_fC_f should be chosen.

*Applications :-

The integrator is used in analog computer & analog-to-digital (ADC) and wave shaping circuit.

*Design a lossy integrator using op-Amp so that peak gain is 20dB & gain is 3dB down from its peak value for $\omega = 10,000$ rad/sec use $C = 0.01\mu f$.

Sol Magnitude of gain for lossy integrator given by

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{R_f/R_1}{\sqrt{1+(\omega R_f C_f)^2}}$$

$$|A|_{dB} = 20\log_{10}\left[\frac{R_f/R_1}{\sqrt{1+(2\pi f R_f C_f)^2}}\right]$$

Gain is at its peak when $\omega = f = 0$

Peak value in dB given by

$$(A)_{dB} = 20\log_{10}\frac{(R_f/R_1)}{\sqrt{1+0}} = 20 \text{ [Given]}$$

$$20\log_{10}(R_f/R_1) = 20$$

$$\frac{R_f}{R_1} = 10 \Rightarrow \boxed{R_f = 10R_1}$$

*Ac Amplifier :-

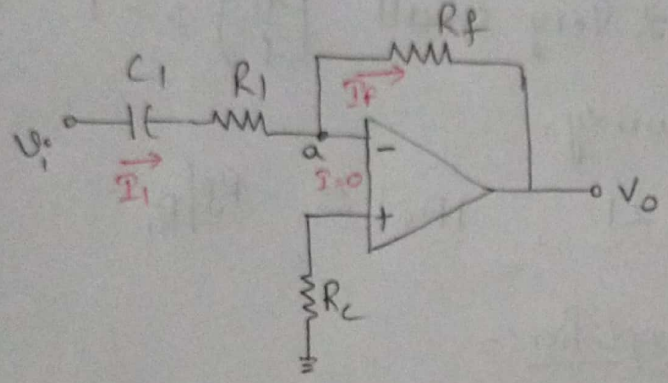
The op-Amp can amplifies both the types of signals Dc and Ac the op-Amp respond to ac signal is called Ac Amplifier

* Ac amplifier are of two types:
- Inverting Ac amplifier
- Non-Inverting Ac Amplifier

* Inverting Ac Amplifier :-

*The input is provided across the inverting terminal of the op-Amp.

*The capacitor is used to block the dc components.



Apply KCL at node 'a'

$$I_1 = I_f$$

$$\frac{V_i - V_a}{R_1 + \frac{1}{sC_1}} = \frac{V_a - V_o}{R_f}$$

[$\because V_a = 0$ [from virtual GND

$$\frac{V_i}{R_1 + \frac{1}{j\omega C_1}} = \frac{-V_o}{R_f}$$

$$V_o = -R_f \times \frac{V_i}{R_1 + \frac{1}{j\omega C_1}}$$

$$V_o = -\frac{R_f}{R_1} \times \frac{V_i}{1 + \frac{1}{j\omega R_1 C_1}}$$

$$\frac{V_o}{V_i} = -\frac{R_f}{R_1} \times \frac{1}{1 + \frac{1}{j\omega R_1 C_1}}$$

$$A_v = \frac{V_o}{V_i} = -\frac{R_f}{R_1} \times \frac{1}{1 - j f_L/f} \qquad \left[f_L = \frac{1}{2\pi R_1 C_1} \right]$$

$$|A_v| = \left| \frac{V_o}{V_i} \right| = \frac{1}{\sqrt{1 + (f_L/f)^2}}$$

- If $f < f_L$, $|A_v| \simeq$ Very small $\left(\frac{f_L}{f}\right)^2 >> 1$

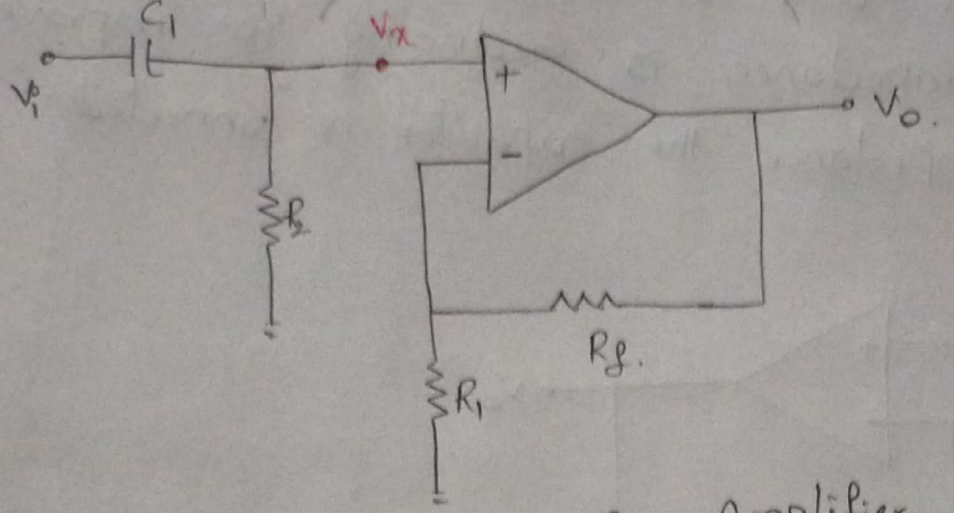
f - Input signal frequency.

- If $f > f_L$ $(f_L/f)^2 << 1$, $|A_v| \simeq -R_f/R_1$.

* Non-Inverting Ac Amplifier :-

* The input is provided across the non-Inverting terminal.
* Here a resistor R_2 is added to provide path for dc signal to ground. This reduces the overall input impedance of the amplifier.
* V_x is the output voltage of the high pass filter connected to the non-Inverting terminal.

Non-Inverting mode operation



Non-Inverting Ac Amplifier.

output voltage expression for non-Inverting.

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_a$$

$$V_a = V_i \times \frac{R_2}{R_2 + \frac{1}{j\omega C_2}}$$

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_i \times \frac{R_2}{R_2 + \frac{1}{j\omega C_2}}$$

$$\frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right] \left[\frac{1}{1 - j f_L/f}\right] \qquad \left[\because f_L = \frac{1}{2\pi R_2 C_1}\right]$$

- If $f < f_L$ $|A_V| \simeq$ very small $(f_L/f)^2 >> 1$
- If $f > f_L$ $|A_V| \simeq \left[1 + R_f/R_1\right]$ $(f_L/f)^2 << 1$

* Disadvantages :-

- R_i if non-Inverting OP-Amp is infinite.

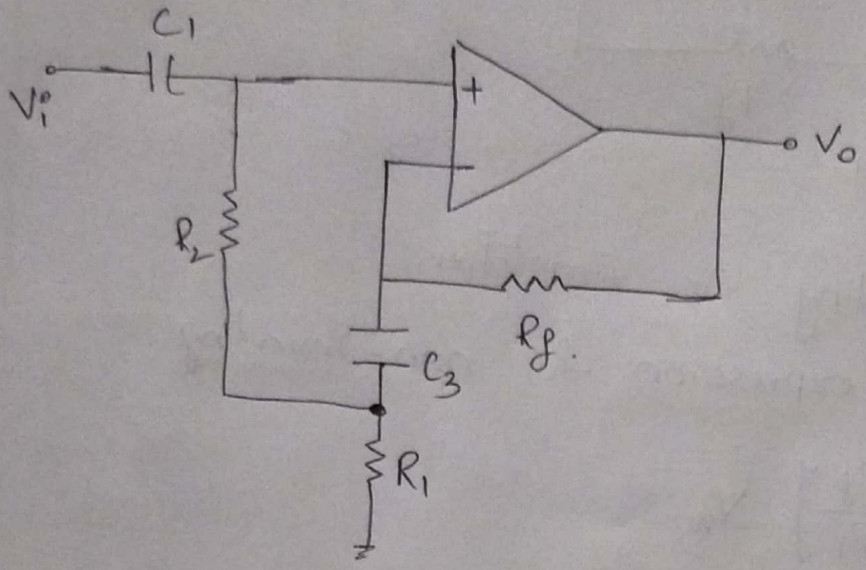
In this ckt.

$R_i = X_{C_1} + R_2$ [if $f < f_1$]

• $R_i = R_2$ $[f > f_L]$

The capacitor acts as short circuit.

*The input impedance is reducing. To improve the input impedance the capacitor is connected.



• for $f < f_L$. The capacitor C_1 & C_3 acts as open circuit.

• If C_1 is open circuit that means no input is transmitted at the non-Inverting terminal.

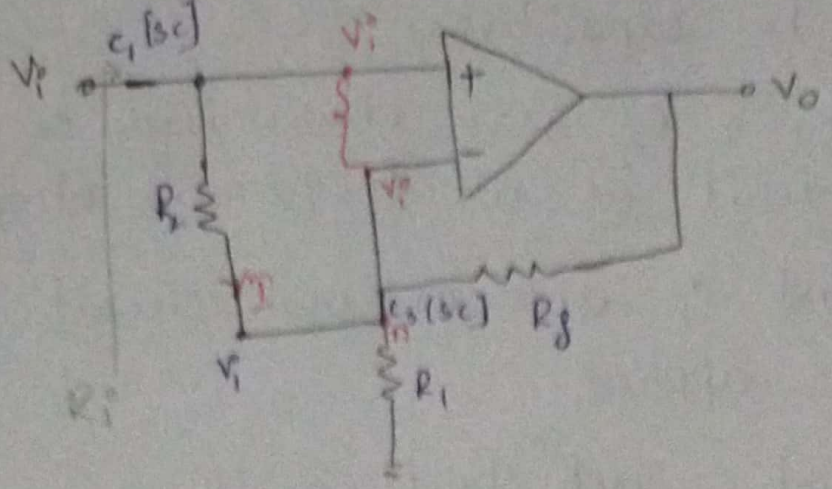
• output is independent of input $V_o = 0$ Even if V_{in} is applied. It is blocking the dc components V_{in}.

* for $f > f_L$. The capacitors ~~acts~~ C_1 and C_3 acts as short circuit.

*The both ends of R_2 are of V_i.

* voltage drop across $R_2 = 0$.

$$V_{R_2} = IR_2. \Rightarrow I = 0.$$



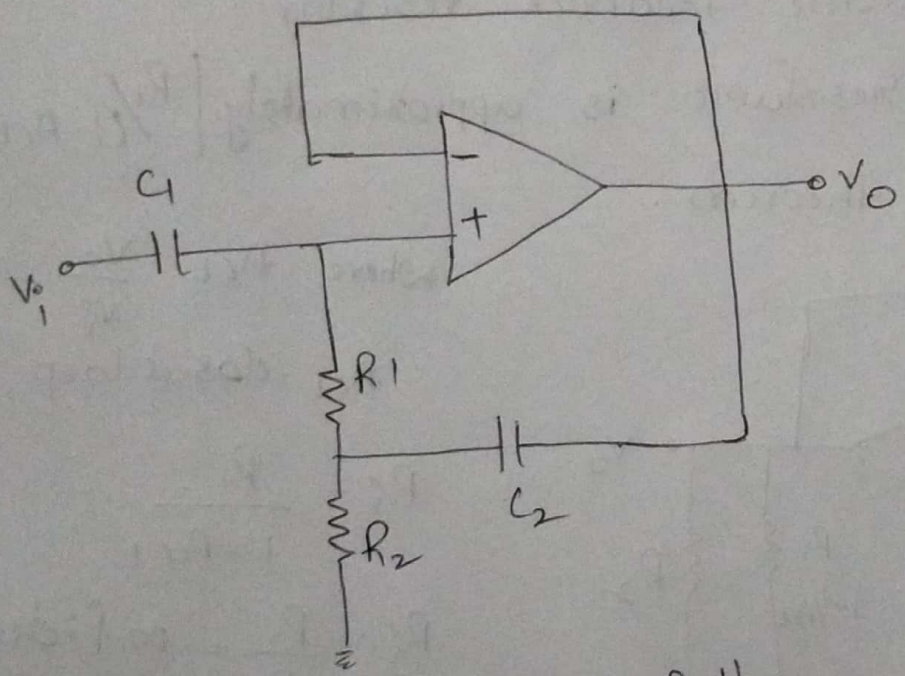
$$R_i = \frac{V_i}{I} = \frac{V_i}{0} = \infty \quad [\text{Ideal}]$$

*Ac voltage follower :- Ac Amplifier with unity gain

- characteristics :-

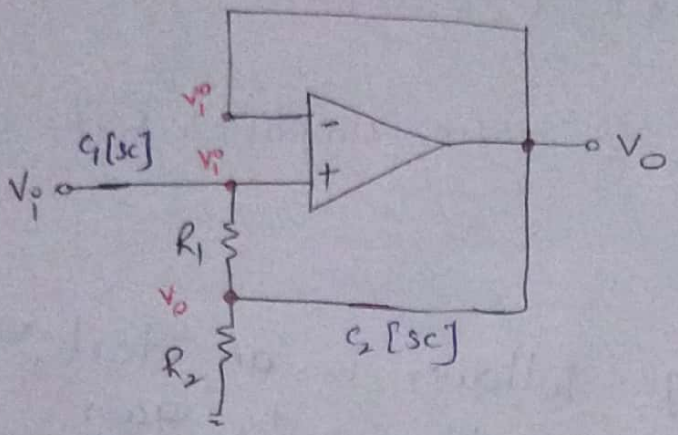
- $A_v = 1$
- $R_i = \infty$
- $R_o = 0$

} voltage follower is an ideal voltage amplifier with unity gain.



Ac voltage follower.

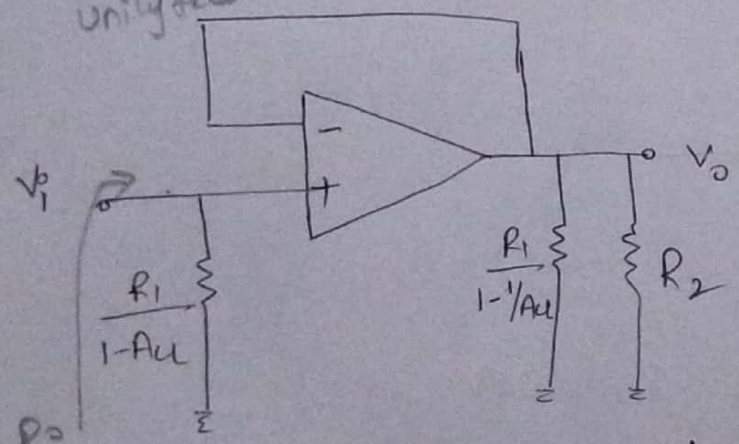
* The circuit is used as a buffer to connect a high impedance signal source to a low impedance load which may even be capacitive.
* The capacitor C_1 & C_2 are chosen high so that they are short circuit at all frequencies of operation
* for $f < f_L$. C_1 and C_2 acts as open circuit
$V_o = 0$ Even V_i is applied.
* for $f > f_L$, C_1 and C_2 acts as short circuit



Because of virtual short
$V_o = V_i'$ [Now the circuit is acting as voltage follower].

* Since C_2 is short circuit
* Since C_2 is acting as short circuit that makes R_1 to ~~fee~~ become feedback resistor.
* The input resistance is approximately $\left[R_1 / (1 - A_{CL}) \right]$ from miller's theorem.

unity feedback



where $A_{CL} = \frac{V_o}{V_i'} = 1$

A_{CL} = closed loop gain

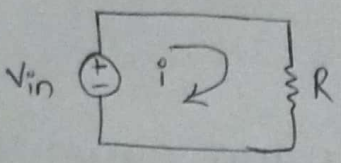
$$R_i' = \frac{R_1}{1 - A_{CL}}$$

$$R_i' = \frac{R_1}{0} = \infty \text{ [ideal]}$$

* Thus very high i/p impedance is obtained.

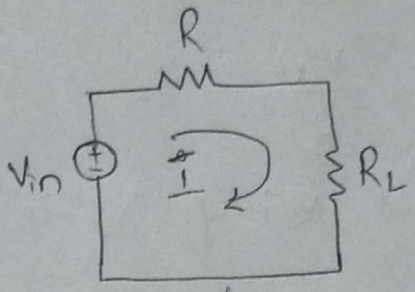
* Voltage to current Converter [Transconductance Amplifier]:-

* The circuit converts an input voltage signal to proportional output current.
* This circuits are used in Industrial applications and Instrumentation.
* consider passive circuit.



$$i = \frac{V_{in}}{R}$$

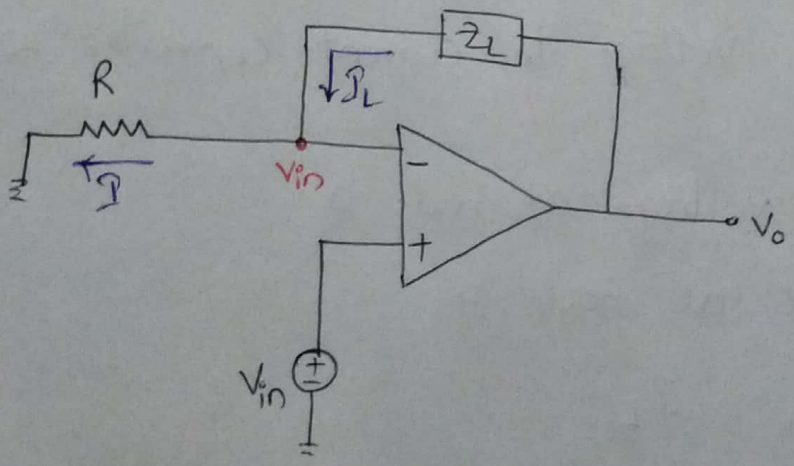
. The current is proportional to input voltage.



$$I = \frac{V_{in}}{R+R_L}$$

*The current dependents on the load resistance also.

* By using the active component i.e Op-amp. There are two types of circuits possible.
(i) Voltage to current Converter with floating load.
(ii) Voltage to current Converter with grounded load.



floating load.

*The ckt shows voltage to current converter in which load Z_L is floating.

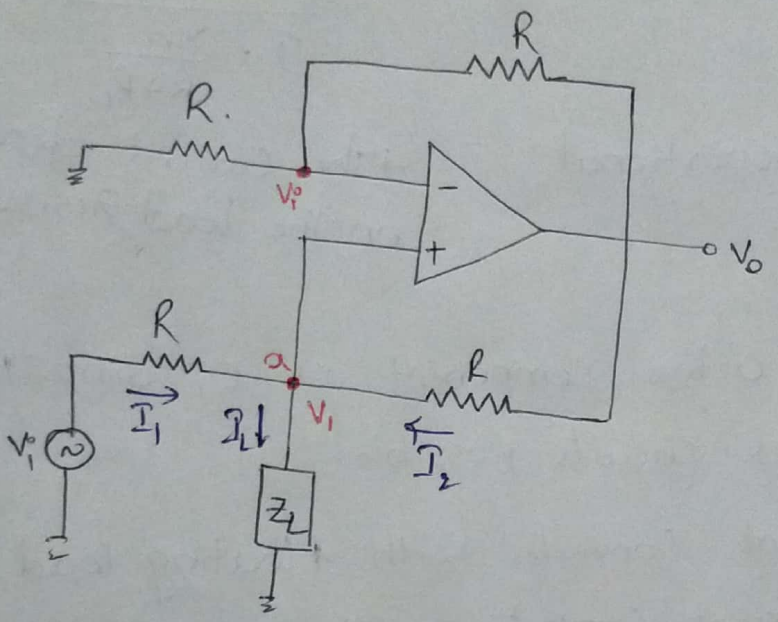
let V_i be voltage at node 'a' [virtual ground].

Apply KCL

$$I = I_L$$

$$\frac{V_{in}}{R} = I_L \qquad \therefore I_L = \frac{V_{in}}{R}$$

Input voltage V_i is converted into an output current of $\frac{V_i}{R}$



Grounded load.

*The ckt shows voltage to current converter with grounded load.

let V_1 be voltage at node 'a'

Apply KCL at node 'a'

$$I_1 + I_2 = I_L$$

$$\frac{V_{in} - V_1}{R} + \frac{V_o - V_1}{R} = I_L$$

$V_i - V_1 + V_o - V_1 = I_L R$

$V_i + V_o - 2V_1 = I_L R$ — (1)

Since op-amp is used in non-Inverting mode gain of non-Inverting amplifier.

$$A = \frac{V_o}{V_i} = \left(1 + \frac{R_f}{R_1}\right)$$

$$V_o = \left(1 + \frac{R}{R}\right) V_1 \Rightarrow V_o = 2V_1$$

Sub. $V_o = 2V_1$ in Eqn (1)

$V_i + 2V_1 - 2V_1 = I_L R$

$$I_L = \frac{V_i}{R}$$

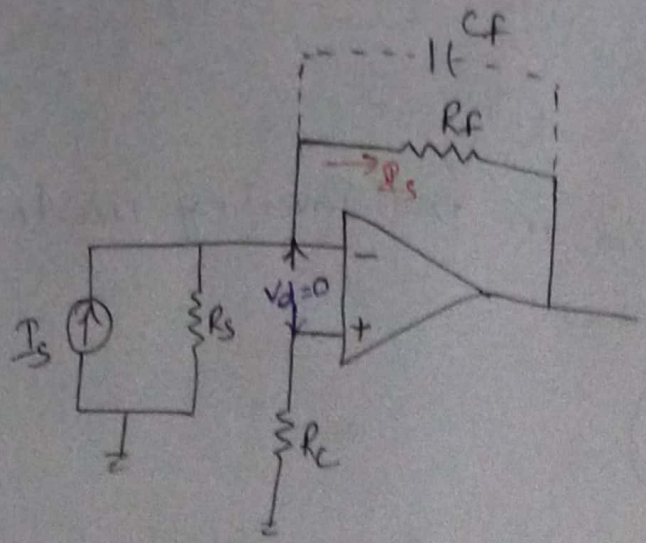
It is independent of the load resistance.

* The application include low voltage dc & ac voltmeter, LED and Zener diode tester.

* Current to voltage Converter [Transresistance Amplifier]:-

* The devices like photocell, photo diode and photo voltaic cell gives an output current proportional to incident radiation energy or light.

* The current through these devices can be converted to voltage by using current to voltage converter and hence amount of light or incident radiant energy measured.



* The figure shows Op-Amp used as current to voltage converter with inverting (-) input terminal at virtual ground.

* Thus no current flows through R_s & current flows through feedback resistance R_f.

Hence output voltage $V_o = -I_s R_f$.

* The resistor R_f is shunted with capacitor C_f to reduce high frequency noise and possibility of oscillation.

* Sample and Hold circuit :-

* A sample and Hold circuit samples an input signal and holds on its last sampled value until the input is sampled again.

* This type of circuit is useful in digital interfacing and analog to digital and pulse code modulation systems.

* The n-channel E-MOSFET works as switch and controlled by control voltage V_c and capacitor 'C' stores the charge.

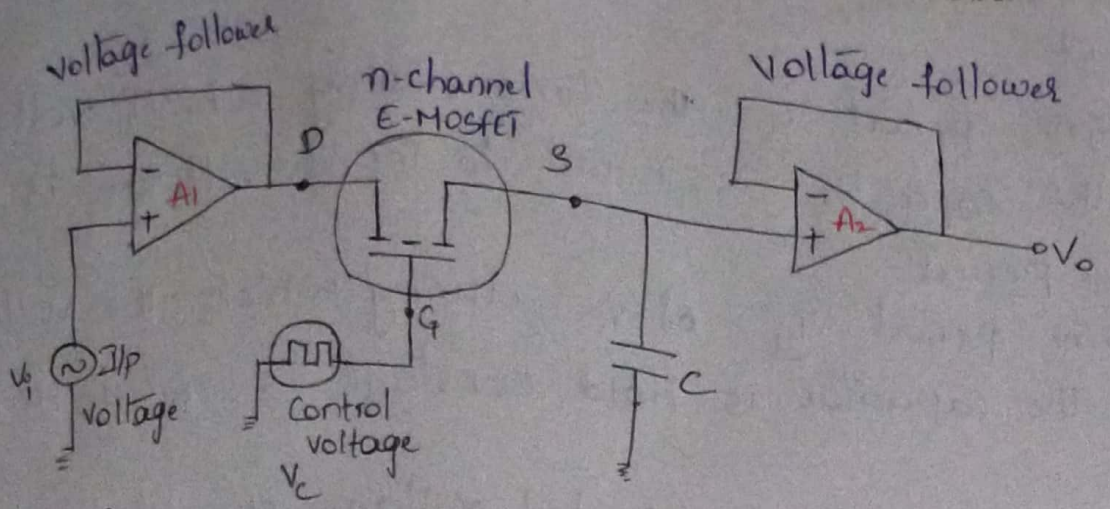


fig: Sample and Hold circuit.

* The analog signal V_i to be sampled is applied to drain of MOSFET and control voltage V_c is applied to its gate.

* Operation :-

* When V_c is positive the E-MOSFET turns ON and capacitor 'C' charges to instantaneous value of input V_i with time constant

$$\tau = [(R_o + r_{DS})_{(ON)}]C.$$

Where R_o is output resistance of the voltage follower A_1.

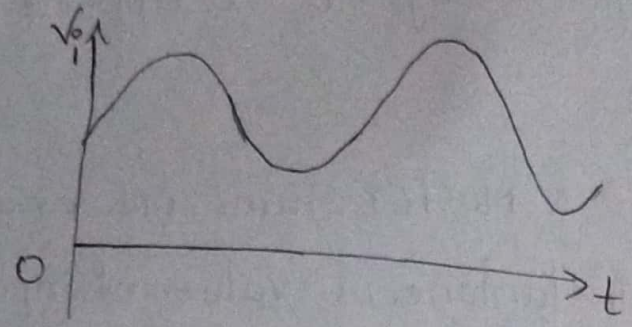
$r_{DS(ON)}$ - Resistance of MOSFET b/w drain and source when MOSFET is turned ON.

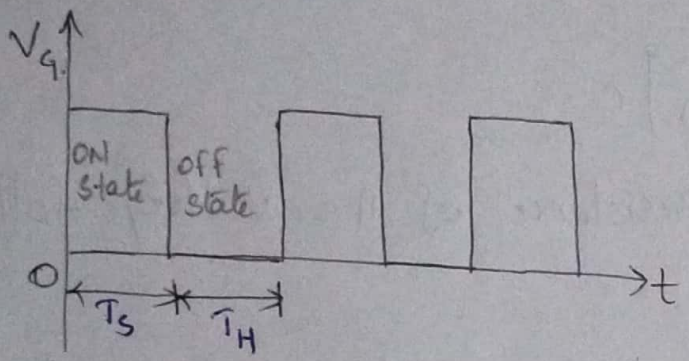
* Thus the input voltage V_i appears across the capacitor 'C' and then at the output through the voltage follower A_2.

* During the time when control voltage V_c is zero the MOSFET turns off. The capacitor 'C' Now connected to high input impedance of voltage follower A_2 and hence cannot discharges. The capacitor holds the voltage

across it.

* The time period 'T_s' the time during which voltage across the capacitor is equal to input voltage is called sample period.
* The Time period 'T_H' of V_c during which the voltage across the capacitor is held constant is called Hold Period.
* The frequency of the control voltage should be kept higher than the input so as to retrive the input from output waveform.





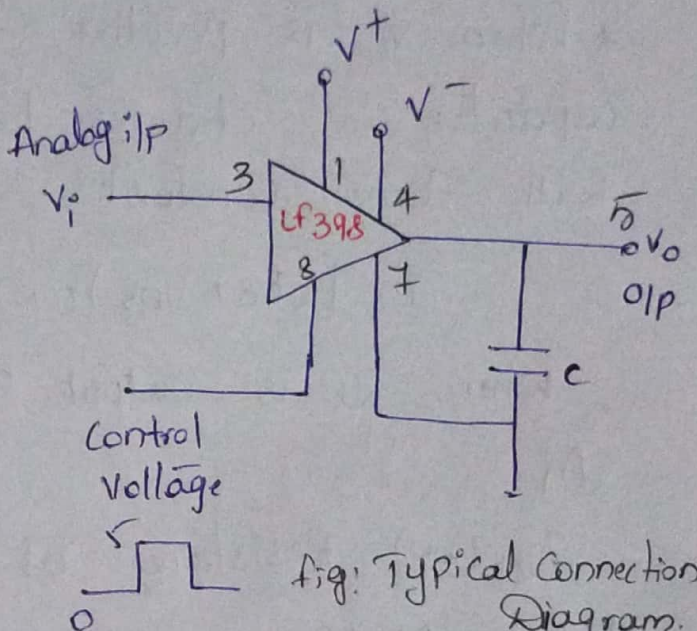
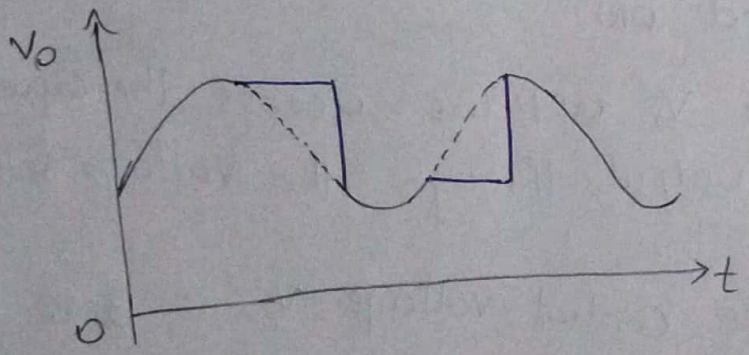


fig: Typical Connection Diagram.

* A typical connection diagram of the Lf398. It may be noted that the storage capacitor C is connected externally.



Input and output waveforms.

During ON:-
Switch-ON, C-charges, ckt Works on Track mode [sample]

During off:-
Switch-off, ckt Works on Holding mode

* Comparator :-

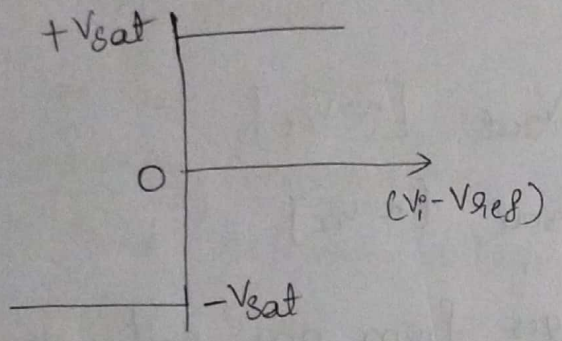
* The non-linear applications of op-Amp include comparator, detector, limiters, Digital Interfacing etc.

* A Comparator is a circuit which Compares input signal voltage at one input of an op-Amp. with known reference voltage at other input.

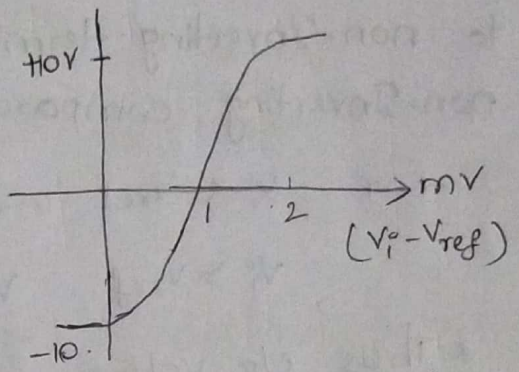
* It is basically an open-loop op-Amp with two analog input and digital output varies $\pm V_{sat}$.

* These are used in circuits such as digital Interfacing, Schmitt trigger, descriminators, voltage-level detectors and oscillators.

Transfer characteristics



(a) Ideal Comparator



(b) Practical comparator.

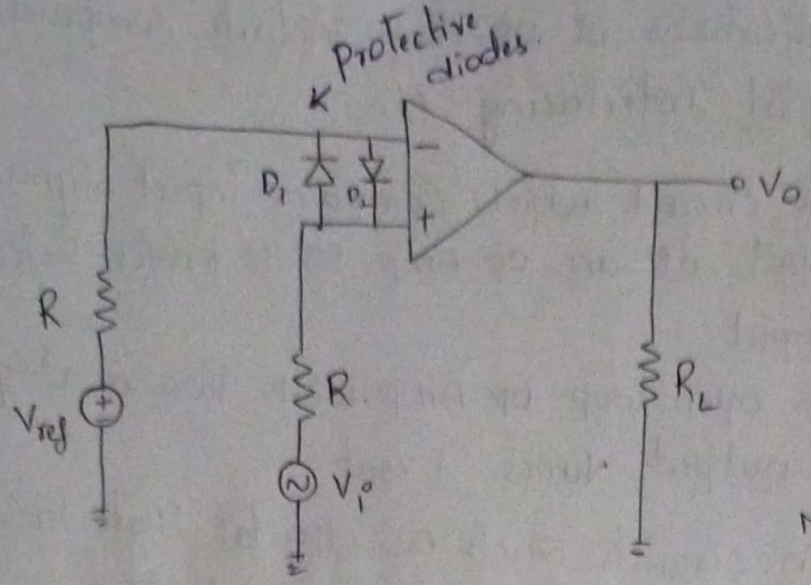
* There are two types of comparators

(i) Non-Inverting Comparator $\begin{cases} V_i > V_{ref} \rightarrow V_o \text{ switches from } -V_{sat} \text{ to } +V_{sat} \\ V_i < V_{ref} \rightarrow V_o \text{ switches from } +V_{sat} \text{ to } -V_{sat} \end{cases}$

(ii) Inverting Comparator.

$\begin{cases} V_i > V_{ref} \rightarrow V_o \text{ switches } +V_{sat} \text{ to } -V_{sat} \\ V_i < V_{ref} \rightarrow V_o \text{ switches } -V_{sat} \text{ to } +V_{sat} \end{cases}$

* Non-Inverting Comparator :-



Non-Inverting Comparator.

* A fixed ref voltage V_{ref} (1V) is applied to Inverting (-) i/p and time varying signal voltage V_i is applied to non-Inverting terminal this circuit is called as non-Inverting comparator.

for $V_i < V_{ref}$, $V_o = -V_{sat}$ $[\sim V_{EE}]$

$V_i > V_{ref}$, $V_o = +V_{sat}$ $[\sim V_{cc}]$

* Thus o/p voltage V_o changes from one saturation level to another saturation level. A sinusoidal input wave converts into square wave input.

* The comparator is of analog-to-digital converter.

* The diodes D_1 & D_2 protects the op-Amp from damage due to excess input voltage V_i. Due to these diodes, the difference i/p voltage V_{id} of op-Amp is clamped to ± 0.7 V. Hence diodes are called clamp diodes.

* In Practical Comparator V_{ref} obtained by using 10kΩ Potentiometer which forms voltage divider with

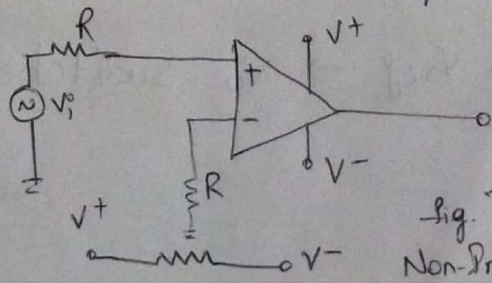
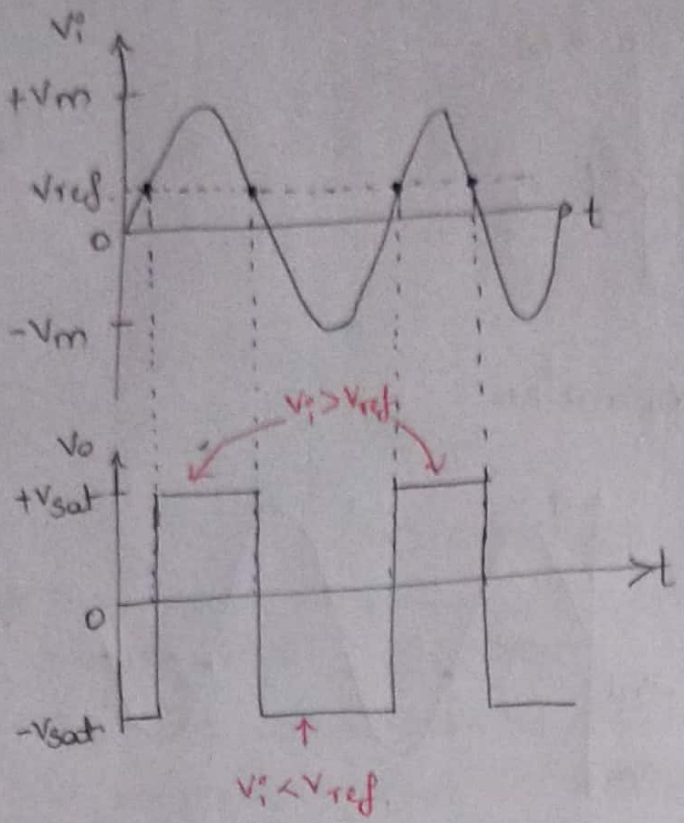
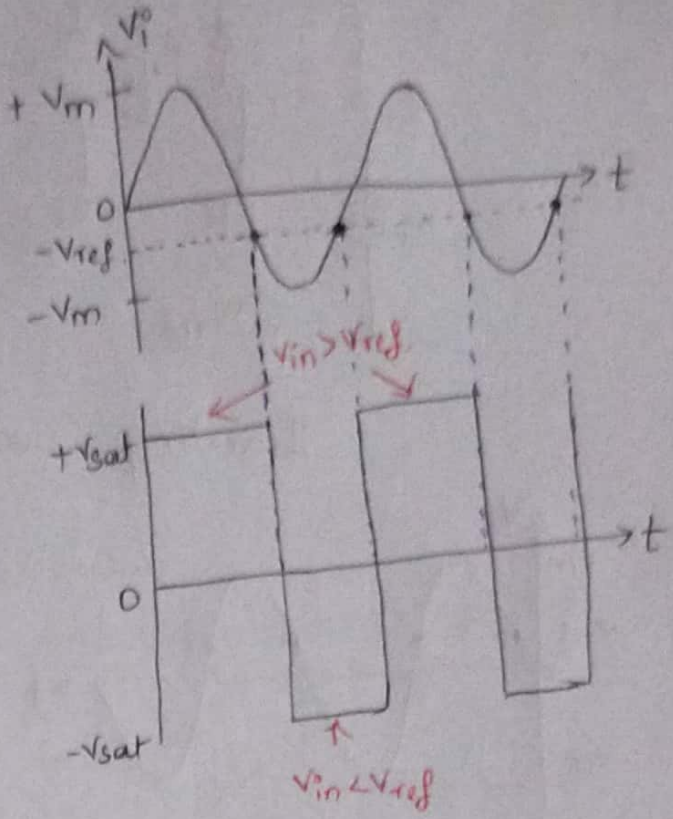


fig. Practical Non-Inverting Comparator.

Supply voltage V^+ & V^- with wiper connected to (-) i/p terminal.



(a) V_{ref} → positive.



(b) V_{ref} → Negative.

Input and output waveforms.

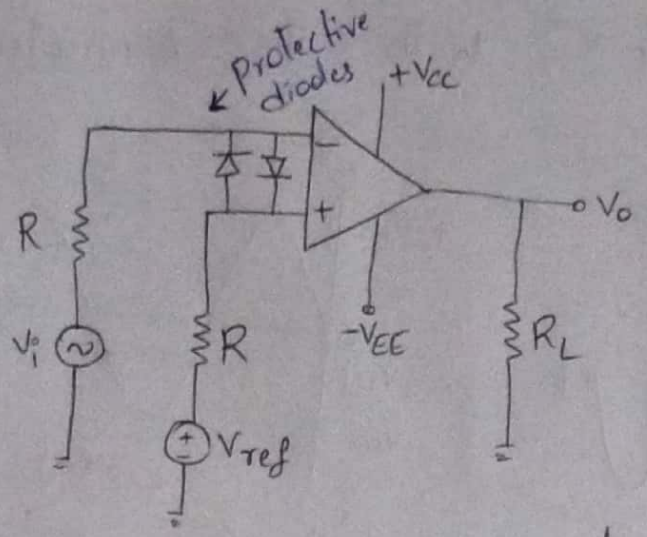
*Inverting Comparator :-

- A fixed reference voltage V_{ref} (1V) is applied to non-Inverting input and time varying signal voltage V_i is applied to Inverting (-) input. This circuit is known as Inverting comparator.

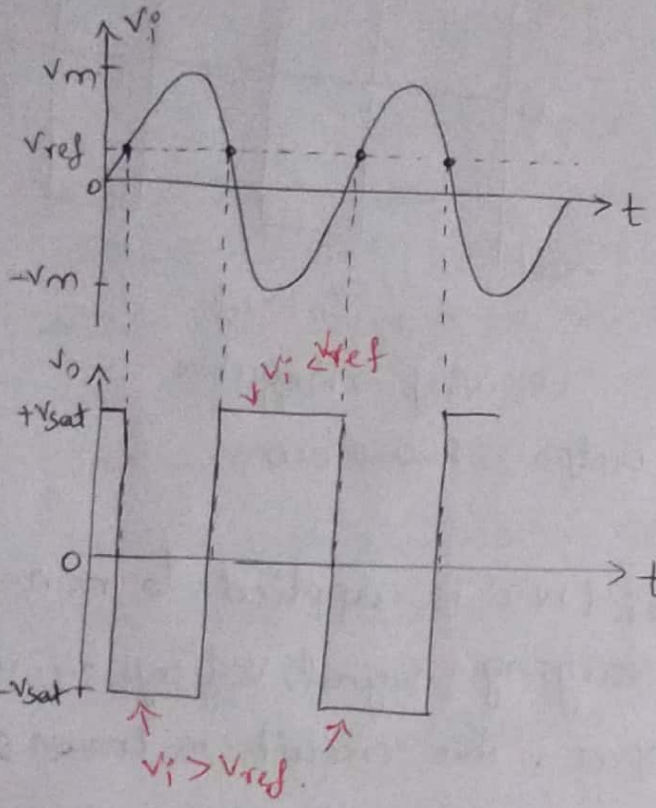
for $V_i < V_{ref}$, $V_o = +V_{sat}$ $[\sim V_{cc}]$

$V_i > V_{ref}$, $V_o = -V_{sat}$ $[\sim V_{EE}]$

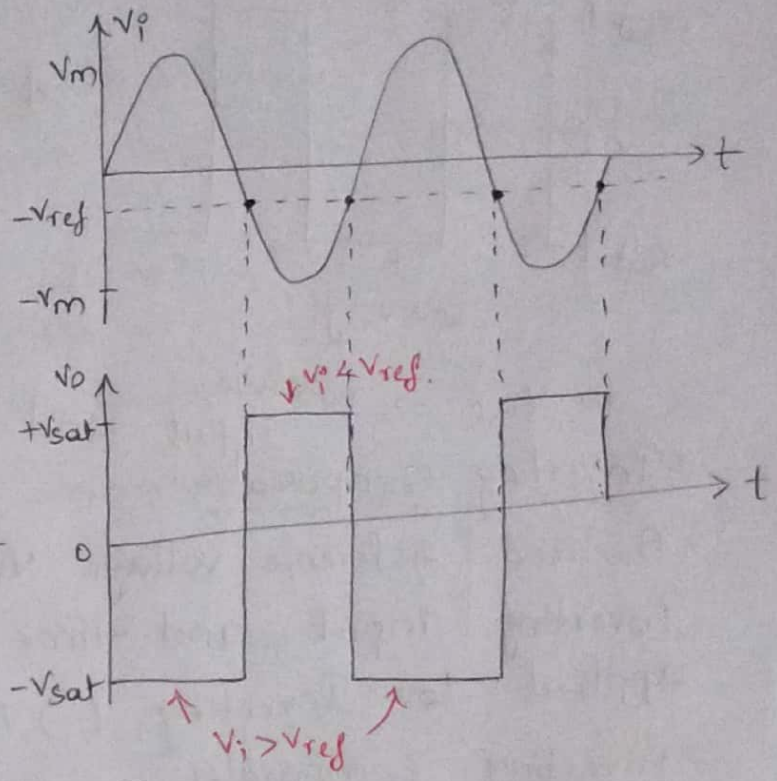
*Thus output voltage V_o changes from one saturation to other level. In Practical Comparator V_{ref} is obtained by using 10 kΩ potentiometer which forms voltage divider with supply voltage V^+ & V^- with wiper connected to (+) input terminal.



Inverting Comparator



(a) Vref is positive



(b) Vref is Negative

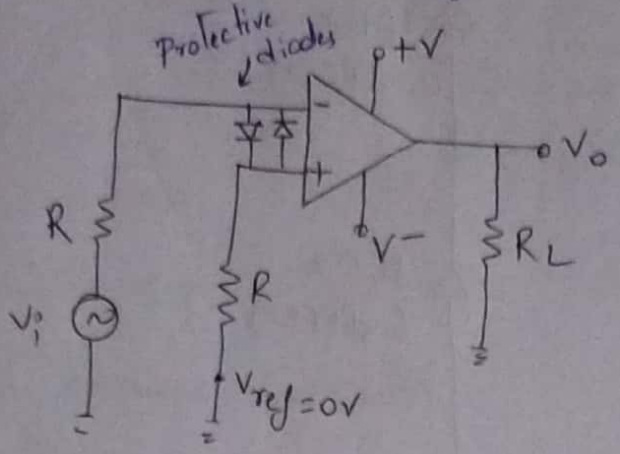
Input and output Waveforms.

* Applications of Comparator :-

- Zero crossing detector
- Window detector
- Time Marker Generator
- Phase detector

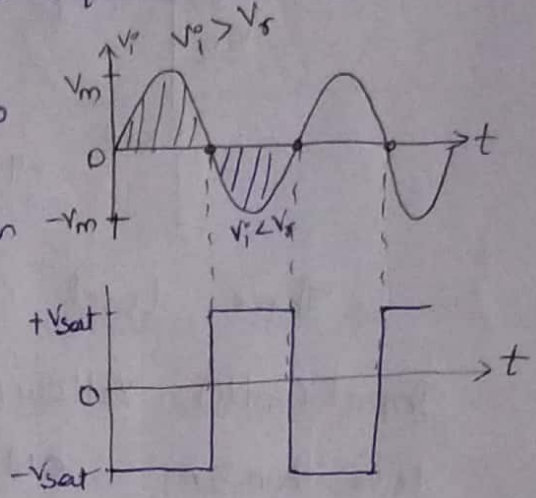
* Zero Crossing Detector :-

- The basic comparator can be used as zero crossing detector provided $V_{ref} = 0V$.



Zero crossing Detector.

* This ckt converts sine wave into square wave called square wave generator.
* The o/p wave form, V_o driven into -ve saturation. when i/p voltage V_i passes through zero in +ve direction
* Also o/p waveform (V_o) driven into +ve saturation when i/p voltage V_i passes through zero in -ve direction.



$V_i > V_r$, $V_o = -V_{sat}$

$V_i < V_r$, $V_o = +V_{sat}$

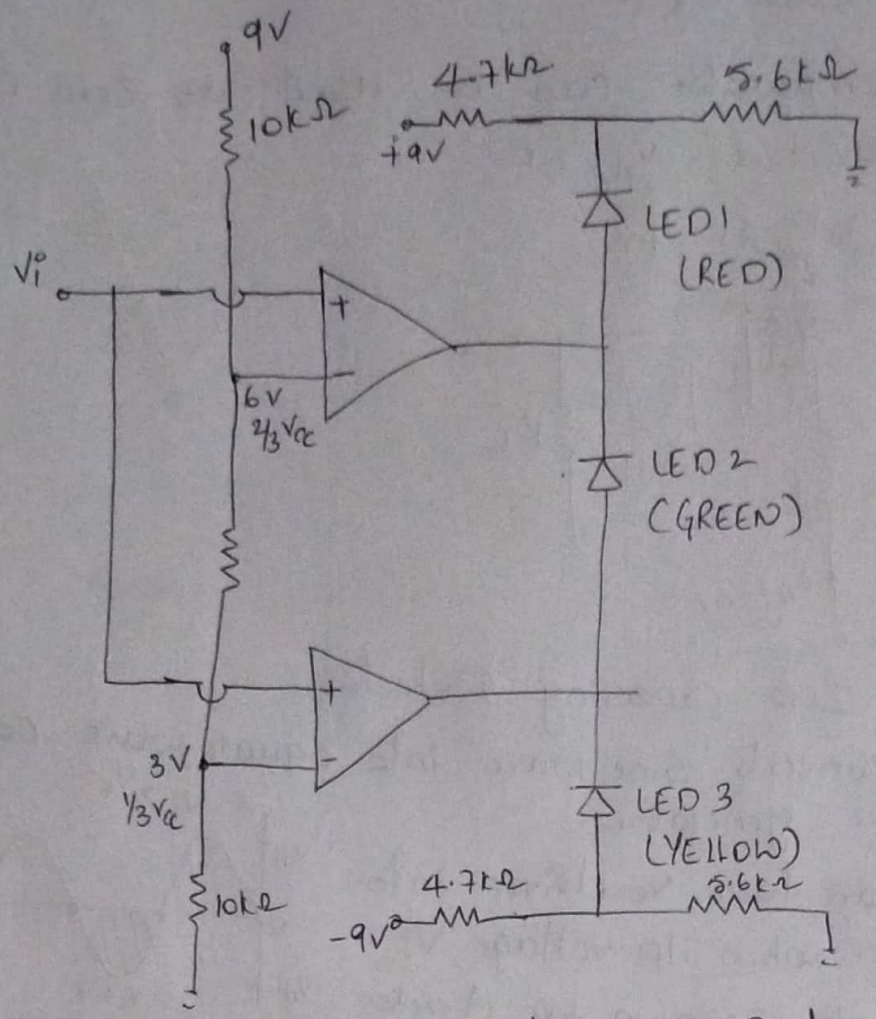
* Window detector :-

* The window detector is circuit which is used to mark the instant at which an unknown i/p is blw two threshold levels.
* A three level detector with three indicator circuit
* There are three indicator

Yellow (LED 3) - i/p too low (< 3V)

Green [LED 2] - safe i/p (3-6V)

Red [LED 1] - high i/p (> 6V)



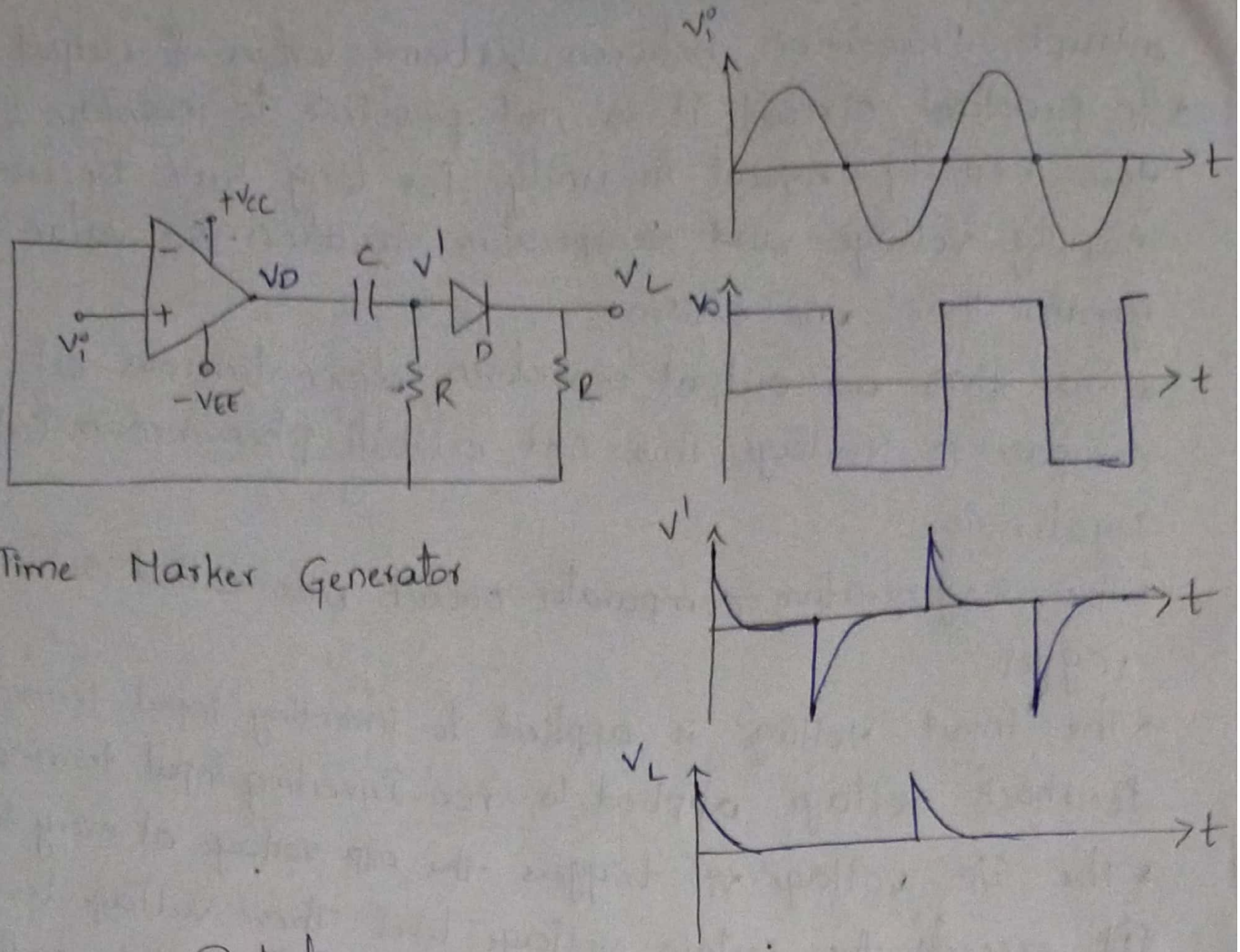
Three level comparator with Indicator.

Input (volts)	Yellow (LED3)	Green (LED 2)	Red (LED1)
less than 3V	ON	off	off
B/w 3V & 6V	off	ON	off
Greater than 6V	off	off	ON

*Time Marker Generator :-

* The o/p of the Zero crossing detector is differentiated by an RC ckt (RC << T) such that V' is in series of positive negative spikes

* The negative portion is clipped off after passing through the diode (D). This ckt converts sinusoidal into train of pulses of spacing (T) and used for triggering monostable, SCR, sweep voltage of CRT etc.



Time Marker Generator

*Phase Detector :-

*The phase angle blw two voltages can be measured using time marker generator. Both voltages are converted into spikes and time interval blw pulse spikes of one i/p and that of other is measured.

*A time interval is proportional to phase difference One can measure phase angles from 0° to 360° with such circuit.

*Schmitt Trigger :- [Regenerative comparator] :-

*If positive feedback is added to the comparator circuit the gain can be increased greatly. Thus transfer curve of comparator becomes closed to Ideal-curve.

*If loop gain is adjusted to unity then gain with feedback A_{Vf} becomes infinite. This results in an

adrupt transition between extreme values of output voltage

* In practical circuit, it is not possible to maintain loop-gain exactly equal to unity for long time because of supply voltage and temperature variation. so value greater than one chosen.
* this gives an output waveform discontinuous at comparison voltage. This ckt exhibits phenomenon called Hysterisis.
* The regenerative comparator circuit also called schmitt Trigger.
* The input voltage is applied to inverting input terminal and feedback voltage applied to non-inverting input terminal.
* The i/p voltage V_i triggers the o/p voltage at every time. It exceeds the certain voltage level. These voltage levels are called upper threshold voltage (V_{UTP}) and lower threshold voltage [V_{LTP}].
* the Hysterisis width is the difference blw two threshold voltages. $V_H = V_{UT} - V_{LT}$

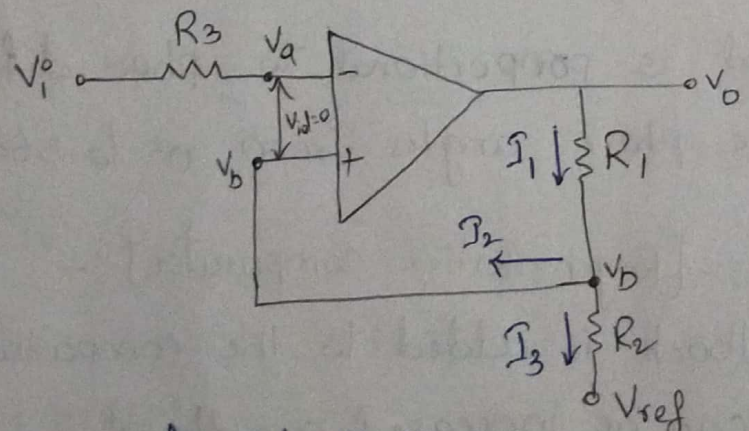


fig. schmitt Trigger.

Apply KCL at node b

$I_1 = I_2 + I_3$.

As per ideal characteristics $R_{in} = \infty$

$\frac{V_{in}}{I_{in}} = \frac{1}{0}$.

$I_{in} = I_2 = 0$.

$I_1 = 0 + I_3 \Rightarrow I_1 = I_3$

$\frac{V_b - V_o}{R_1} = \frac{V_{ref} - V_b}{R_2}$

$$V_b\left[\frac{1}{R_1}+\frac{1}{R_2}\right] = \frac{V_{ref}}{R_2}+\frac{V_o}{R_1}$$

$$V_b\left[\frac{R_1+R_2}{R_1R_2}\right] = \frac{V_{ref}R_1+V_oR_2}{R_1R_2}$$

$$V_b = \frac{V_{ref}R_1+V_oR_2}{R_1+R_2}.$$

As per Ideal characteristics $V_{id}=0 \Rightarrow V_a=V_b$.

$V_a = V_{in}$, $V_a = V_b = V_{in}$

$$V_{in} = \frac{V_{ref}R_1+V_oR_2}{R_1+R_2} \Rightarrow$$

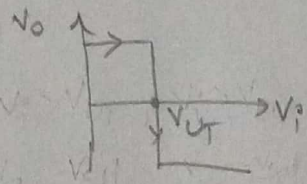
If $V_{ref}=0$ then

$$V_{in} = \frac{R_2}{R_1+R_2}V_o.$$

* Upper Threshold voltage:-

$V_{in} = V_{UT}$, $V_o = +V_{sat}$.

$$\boxed{V_{UT} = \frac{R_2}{R_1+R_2}(+V_{sat})}$$

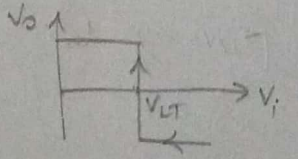


$V_i \le V_{UT}$ o/p $+V_{sat}$

* lower Threshold voltage:-

$V_{in} = V_{LT}$, $V_o = -V_{sat}$.

$$\boxed{V_{LT} = \frac{R_2}{R_1+R_2}(-V_{sat})}$$



$V_i \le V_{LT}$ o/p $-V_{sat}$

$$A_f = \frac{A_{OL}}{1+\beta A_{OL}} = \frac{A_{OL}}{1-[-\beta A_{OL}]} = \frac{A_{OL}}{0} = \infty$$

($-\beta A_{OL}=1$)

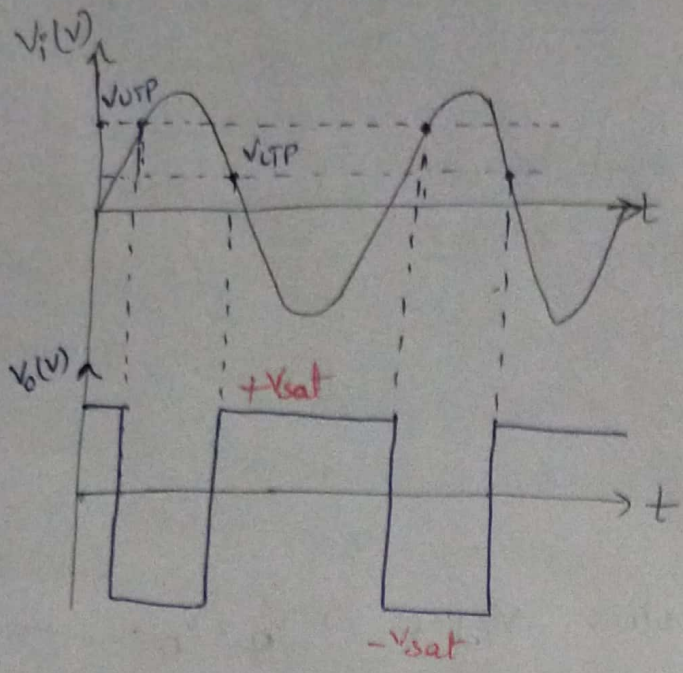
o/p $V_o = \pm V_{sat}$

$-\beta A_{OL}$ is loop gain

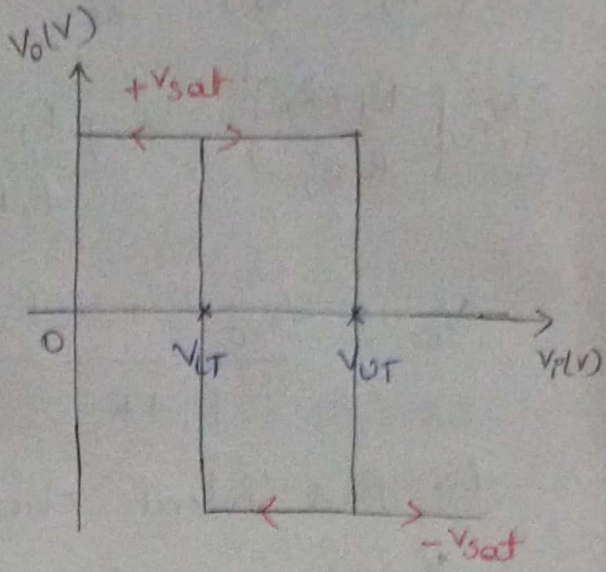
* Hysterisis Width:-

Difference b/w V_{UT} & V_{LT}

$$\boxed{V_H = V_{UT}-V_{LT} = \frac{2R_2}{R_1+R_2}[V_{sat}].}$$



Input and output waveforms.



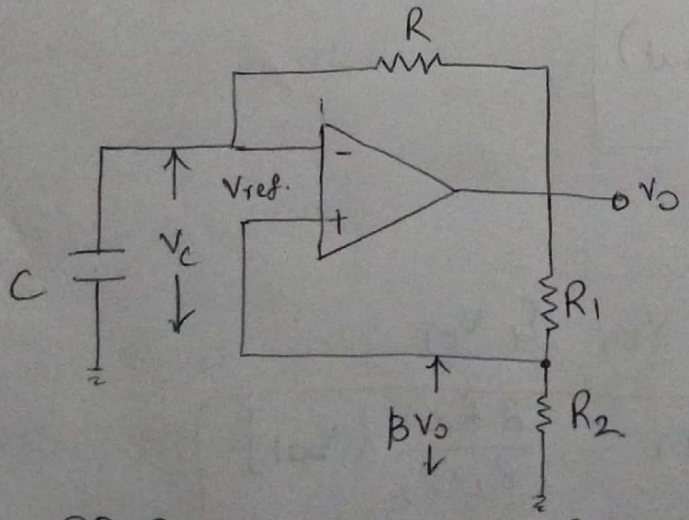
Hysteresis loop.

* Astable Multivibrator :- (square wave Generator).

* the astable Multivibrator contains two states. The two states are quasi-stable state. The output will vary between these two states only.

* The op-Amp square wave generator called free running oscillator, uses principle of generation of square wave o/p by forcing the op-Amp to operate in saturation region.

* The positive feedback is given. The fraction $\beta = R_2/R_1+R_2$ of output is feedback to non-Inverting i/p terminal. The reference voltage V_{ref} is βV_o and V_o takes or saturates b/w $+V_{sat}$ (or) $-V_{sat}$. so the value is $+\beta V_{sat}$ (or) $-\beta V_{sat}$.



OP-Amp square-wave Generator.

This is also comparator Hence V_c will compares with V_{ref}.

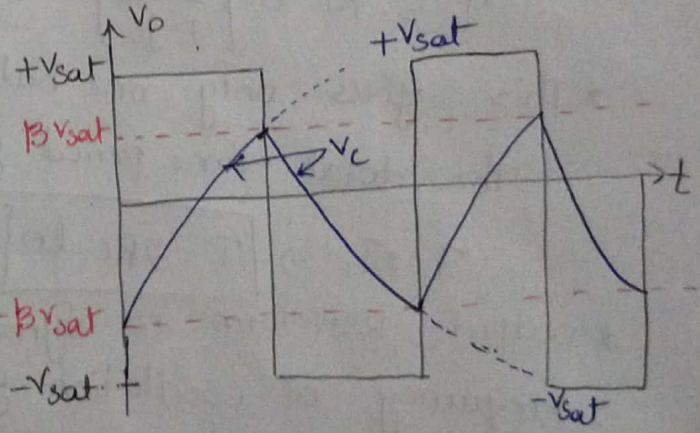
$V_{ref} = \beta V_o$

$V_c > \beta V_{sat}$; $V_o = -V_{sat}$

$V_c < \beta V_{sat}$; $V_o = +V_{sat}$

$$\beta = \frac{R_2}{R_1+R_2}$$

* The o/p is feedback to inverting terminal by a low pass RC circuit.
* Consider an instant of time when o/p is $+V_{sat}$. The capacitor starts charging towards $+V_{sat}$ through resistor R. The voltage at (+ve) non-Inverting terminal hold at $+\beta V_{sat}$ by R_1 & R_2 combinations.
* When the voltage at (-) inverting terminal becomes just greater than the reference voltage the o/p voltage is driven to $-V_{sat}$.
* At this instant, the voltage across the capacitor is $+\beta V_{sat}$ it begins to discharge through R i.e charges towards $-V_{sat}$.
* When the o/p voltage switches to $-V_{sat}$, the capacitor charges more and more negatively until its voltage just exceeds $-\beta V_{sat}$. The output switches back to $+V_{sat}$. This cycle repeats.
* Expression for frequency :-
* The frequency is determined by the time it takes the capacitor to charge from $-\beta V_{sat}$ to $+\beta V_{sat}$ and vice-versa.
* The voltage across the capacitor as function of time is given by



Wave form

$$V_c(t) = V_f + (V_i - V_f)\, e^{-t/RC}$$

where V_f = final voltage = $+V_{sat}$

and V_i = $-\beta V_{sat}$.

where $\beta = \frac{R_2}{R_1 + R_2}$

$$\therefore V_c(t) = V_{sat} + [-\beta V_{sat} - V_{sat}]e^{-t/RC}$$

$$= V_{sat} - [1+\beta]e^{-t/RC} V_{sat}$$

$$\therefore V_c(t) = V_{sat} - V_{sat}[1+\beta]e^{-t/RC}$$

At $t = T_1$, $V_c(t) = \beta V_{sat}$

$$\beta V_{sat} = V_{sat} - V_{sat}[1+\beta]e^{-T_1/RC}$$

$$V_{sat}[1+\beta]e^{-T_1/RC} = V_{sat}[1-\beta]$$

$$e^{-T_1/RC} = \frac{[1-\beta]}{[1+\beta]}$$

$$e^{T_1/RC} = \frac{1+\beta}{1-\beta}$$

Apply natural logarithm [ln] on both sides

$$\frac{T_1}{RC} = \ln\left[\frac{1+\beta}{1-\beta}\right]$$

$$T_1 = RC \ln\left[\frac{1+\beta}{1-\beta}\right]$$

* This gives only one-half of period.

∴ The total time-period given by

$$T = 2T_1 \Rightarrow \boxed{T = 2RC \ln\left[\frac{1+\beta}{1-\beta}\right]}$$

* output waveform is symmetrical

frequency of oscillation given by

$$f = \frac{1}{T}$$

$$\boxed{f = \frac{1}{2RC\ln\left[\frac{1+\beta}{1-\beta}\right]}}$$

for $R_1 = R_2$, $\beta = 0.5$ & $T = RC\ln(3)$

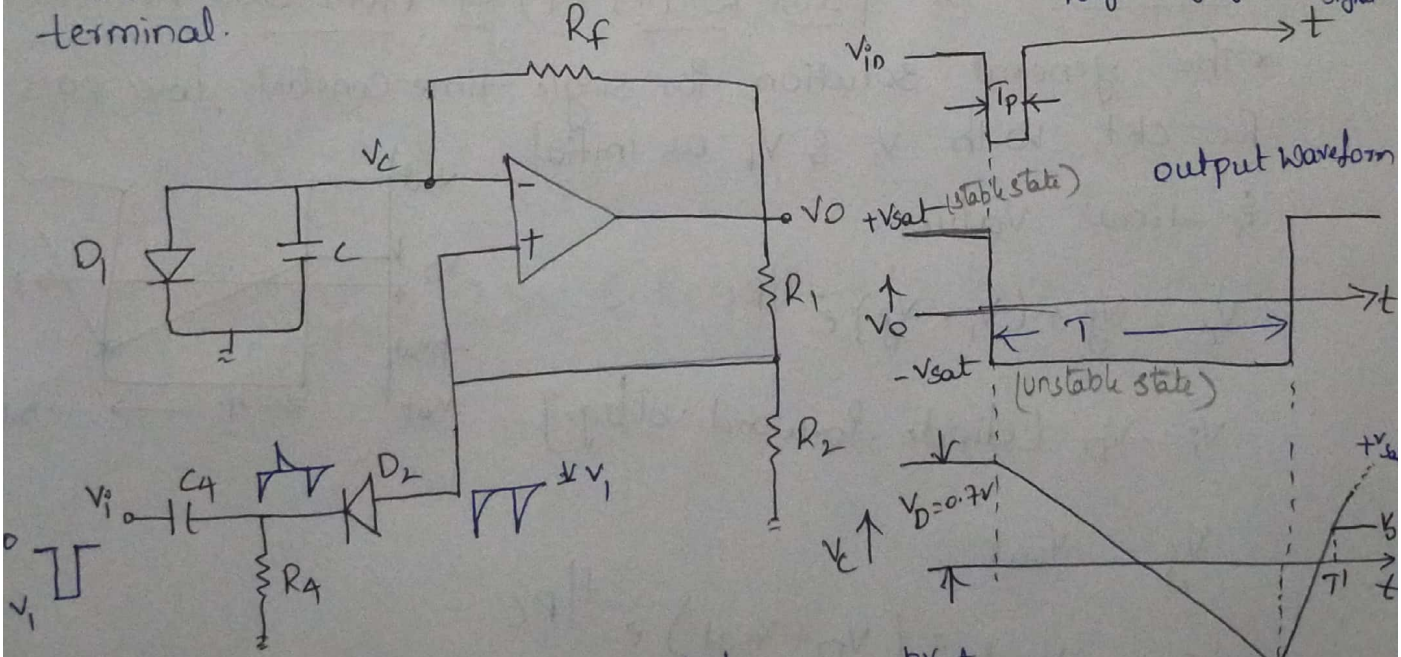
$$\boxed{T = 1.1RC}$$

*Monostable Multivibrator :-

*The monostable multivibrator has one stable state and other as quasi stable state. The ckt is useful for generating single o/p pulse of adjustable time duration in response to triggering pulse.

*The width of the pulse depends on the only one external components connected to the op-Amp. This is modified form of Astable multivibrator.

*Initially assume the output voltage is $+V_{sat}$. The diode D_1 is forward biased. the capacitor and it clamps to 0.7v, the voltage across the capacitor will be the forward voltage drop of the diode. i.e $V_c = 0.7v$. A negative going pulse signal of magnitude V_i passing through the differentiator R_4C_4 and the diode D_2 produces a negative going triggering pulse and is applied to the (+) non-Inverting input terminal.



*Assume that in stable state the o/p voltage V_o is $+V_{sat}$, the diode D_1 conducts and V_c the voltage across the capacitor 'c' gets clamped to +0.7v. The voltage at

+ve i/p terminal through R_1 & R_2 voltage divider n/w is $+\beta V_{sat}$

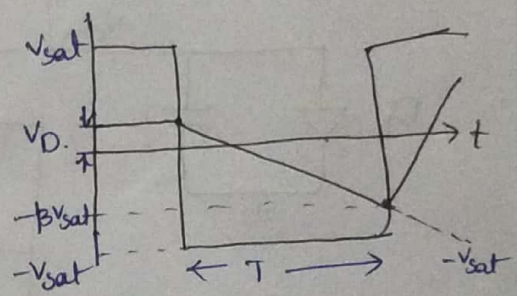
* If negative trigger of magnitude V_1 is applied to +ve i/p terminal. so that the effective of signal at this terminal is less than 0.7V i.e $[\beta V_{sat} + (-V_1) < 0.7V]$ the o/p of OP-Amp will switch from $+V_{sat}$ to $-V_{sat}$.

* The diode will now get reverse biased and capacitor starts discharging exponentially to $-V_{sat}$ through resistance R. The voltage at (+) i/p terminal is now $-\beta V_{sat}$.

* When the capacitor voltage V_c becomes just slightly more negative than $-\beta V_{sat}$ the o/p of OP-Amp switches back to $+V_{sat}$. The capacitor C now starts charging to $+V_{sat}$ through R until V_c is 0.7V as capacitor C gets clamped to voltage.

* Calculation of Pulse width (T) of Monostable Multivibrator

* The general solution for single time constant low pass RC ckt with V_i & V_f as initial & final values.



$$V_c = V_f + (V_i - V_f) e^{-t/RC}$$

$V_i = V_D$ [diode forward voltage]

$V_f = -V_{sat}$

$$V_c = -V_{sat} + (V_D + V_{sat}) e^{-t/RC}$$

At $t = T$ $V_c = -\beta V_{sat}$ (or) $V_o = -\beta V_{sat}$

$$\therefore -V_{sat}\beta = -V_{sat} + (V_D + V_{sat}) e^{-T/RC}$$

$$V_{sat}(1-\beta) = [V_D + V_{sat}]\, e^{-T/RC}$$

$$e^{+T/RC}(1-\beta) = \left[\frac{V_D + V_{sat}}{V_{sat}}\right]$$

$$e^{T/RC}[1-\beta] = \left[1 + \frac{V_D}{V_{sat}}\right]$$

$$e^{+T/RC} = \frac{[1 + V_D/V_{sat}]}{[1-\beta]}$$

Apply natural logarithm on b.s

$$\frac{T}{RC} = \ln\left[\frac{[1 + V_D/V_{sat}]}{[1-\beta]}\right]$$

$$T = RC \ln\left[\frac{1 + V_D/V_{sat}}{(1-\beta)}\right]$$

where $\beta = \frac{R_2}{R_1 + R_2}$

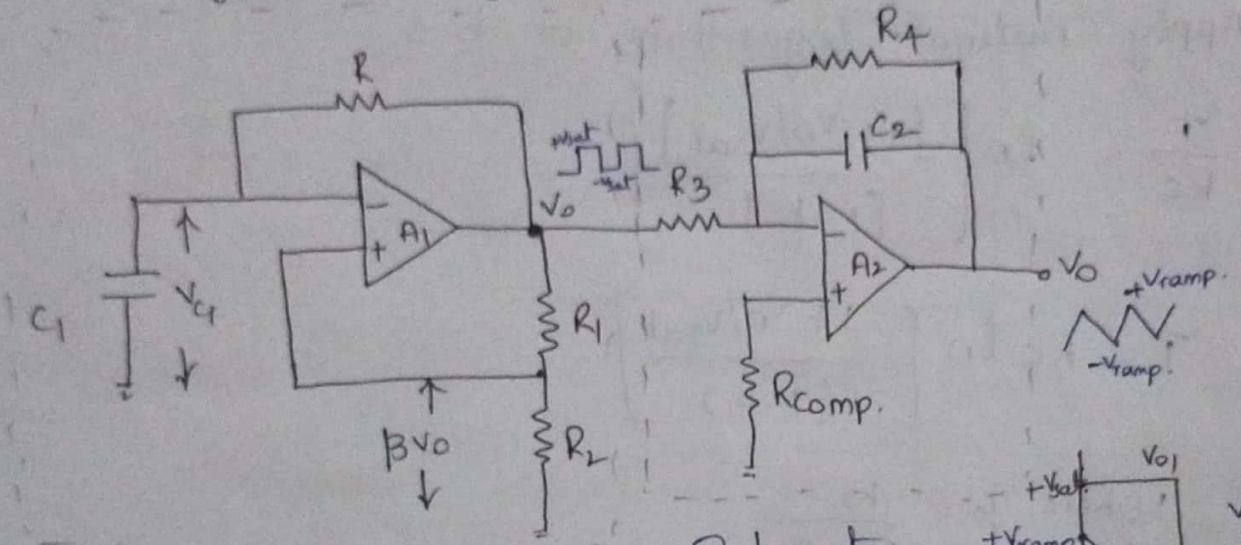
for $V_{sat} >> V_D$ & $R_1 = R_2$ with $\beta = 0.5$ then

then $\boxed{T = 0.69RC}$

* Triangular Waveform Generator :-

* A triangular waveform : Because of its linearity it can be used in
  - Analog to Digital Convertor [ADC]
  - Pulse width modulation [PWM] circuits
    - Switch mode power supply [SMPS]
    - Motor driver control circuits.

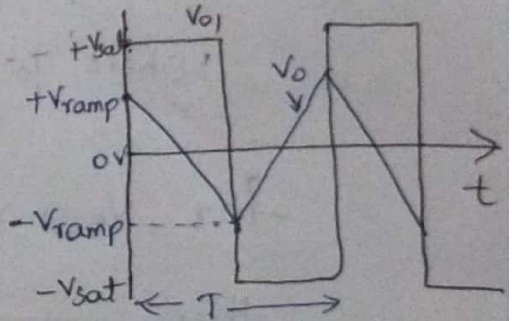
* A triangular waveform is generated by integrating a square waveform. A triangular wave generator formed by converting an integrator to square wave generator.



Square wave generator (Astable ckt)

Integrator

Triangular waveform generator.



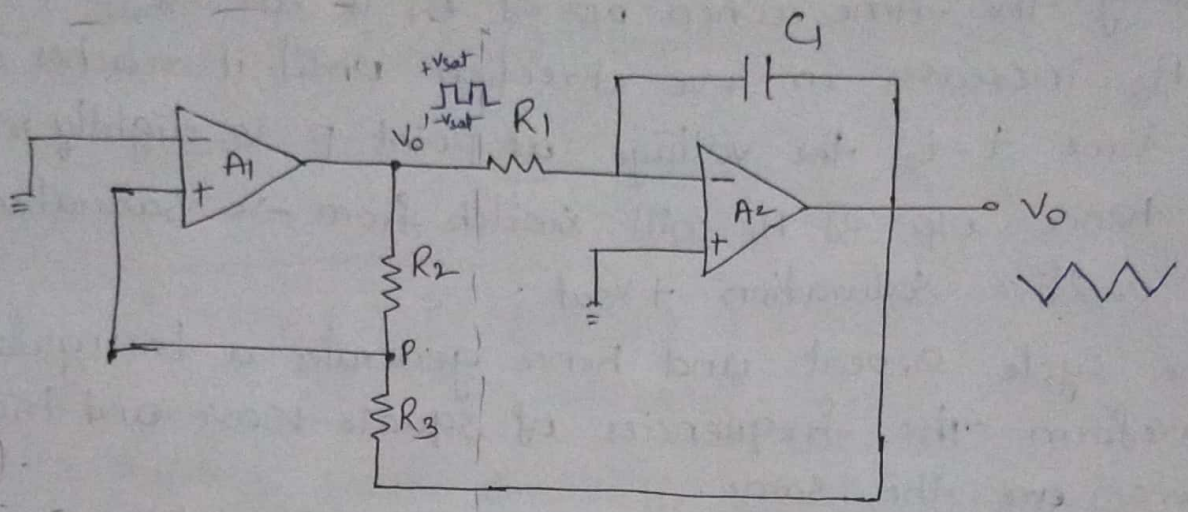
output waveforms.

* the amplitude of square wave is constant at $\pm V_{sat}$. the amplitude of triangular wave will decrease as frequency increases.

* This is because the reactance of capacitor C_2 in feedback circuit decreases at high frequency's. A resistance R_4 is connected across C_2 to avoid the saturation problem at low frequencies in case of practical Integrator.

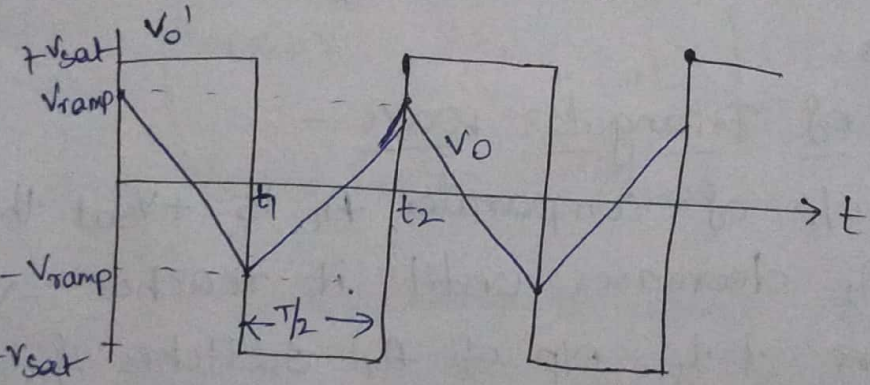
*Another triangular wave generator using lesser number of components. It basically consists of two level comparator followed by integrator. The o/p of comparator A_1 is square wave of amplitude $\pm V_{sat}$ and applied to (-ve) Inverting i/p terminal of Integrator A_2 producing triangular waveform.

*This triangular waveform is feedback as i/p to comparator A_1 through a voltage divider R_2 & R_3.



Schmitt Trigger Integrator

Triangular waveform generator [using less no. of components]



*operation:-

* Consider that o/p of comparator A_1 is at $+V_{sat}$. The $+V_{sat}$ is an i/p to the Integrator A_2. The o/p of A_2 is -ve going ramp.

* Thus one end of voltage divides $R_2 R_3$ is at positive saturation $+V_{sat}$ of A_1 and other is negative going ramp of A_2.
* At time $t=t_1$, when negative going ramp attains certain value $-V_{ramp}$, the effective voltage at point P is slightly less than or hence, o/p of A_1 will switch from +ve saturation $+V_{sat}$ to -ve saturation $-V_{sat}$.
* During the time when o/p of A_1 is at $-V_{sat}$ the o/p of A_2 increases in +ve direction until it reaches $+V_{ramp}$.
* At time $t=t_2$ the voltage at point P is slightly more than 0V, hence o/p of A_1 will switch from -ve saturation $-V_{sat}$ to positive saturation $+V_{sat}$.
* The cycle repeat and hence generates a triangular waveform. The frequencies of square wave and triangular wave are the same.
* The amplitude of triangular wave depends on Rc values of Integrator A_2 and o/p voltage levels of A_1. The desired amplitude can be set by using appropriate Zeners diodes.

* Frequency of Triangular wave :-

When the o/p of comparator A_1 is $+V_{sat}$ the o/p of Integrator A_2 decreases until it reaches $-V_{ramp}$. At this time $t=t_1$ o/p of A_1 switches from $+V_{sat}$ to $-V_{sat}$. Voltage at point P is 0V.

$-V_{ramp} \rightarrow$ developed across R_2.

$+V_{sat} \rightarrow$ developed across R_3

$$\frac{-V_{ramp}}{R_2} = -\frac{+V_{sat}}{R_3}$$

(or)

$$-V_{ramp} = \frac{-R_2}{R_3}(+V_{sat})$$

* When o/p of comparator A_1 is $-V_{sat}$ the o/p of Integrator A_2 increases until it reaches $+V_{ramp}$. At this time $t=t_2$ o/p of A_1 switches from $-V_{sat}$ to $+V_{sat}$. Voltage at point p is 0V.

$+V_{ramp}$ - developed across R_2

$-V_{sat}$ - developed across R_3

$$\frac{+V_{ramp}}{R_2} = -\frac{(-V_{sat})}{R_3}$$

$$+V_{ramp} = -\frac{R_2}{R_3}(-V_{sat})$$

* The peak to peak amplitude of the triangular waveform is given by

$$V_{o(P-P)} = +V_{ramp} - (-V_{ramp})$$

$$V_{o(P-P)} = \frac{2R_2}{R_3}(V_{sat})$$

$$V_{sat} = |+V_{sat}| = |-V_{sat}|$$

* The amplitude of triangular wave decreases with an increase in R_3 the time taken for o/p to switch from $-V_{ramp}$ to $+V_{ramp}$ is half the time period $T/2$. Substituting these values in basic Integrator equating we have

$$V_o = -\frac{1}{RC}\int V_i\, dt$$

$V_i = \mp V_{sat}$

$V_o = V_{o(P-P)}$

$$V_{o(P-P)} = -\frac{1}{R_1C_1}\int_0^{T/2}(-V_{sat})\,dt$$

$$= \left(\frac{V_{sat}}{R_1 C_1}\right) \int_0^{T/2} dt$$

$$= \frac{V_{sat}}{R_1 C_1} \left[T/2\right]$$

$$T = 2 R_1 C_1 \cdot \frac{V_{o(P-P)}}{V_{sat}}$$

Substituting the value of $V_{o(P-P)}$ we get

$$T = 2 \frac{R_2}{R_3} (V_{sat}) \cdot \frac{2 R_1 C_1}{V_{sat}}$$

$$\boxed{T = \frac{4 R_1 C_1 R_2}{R_3}}$$

Frequency of oscillation (f_o) given by

$$\boxed{f_o = \frac{1}{T} = \frac{R_3}{4 R_1 C_1 R_2}}$$

*Oscillators :-

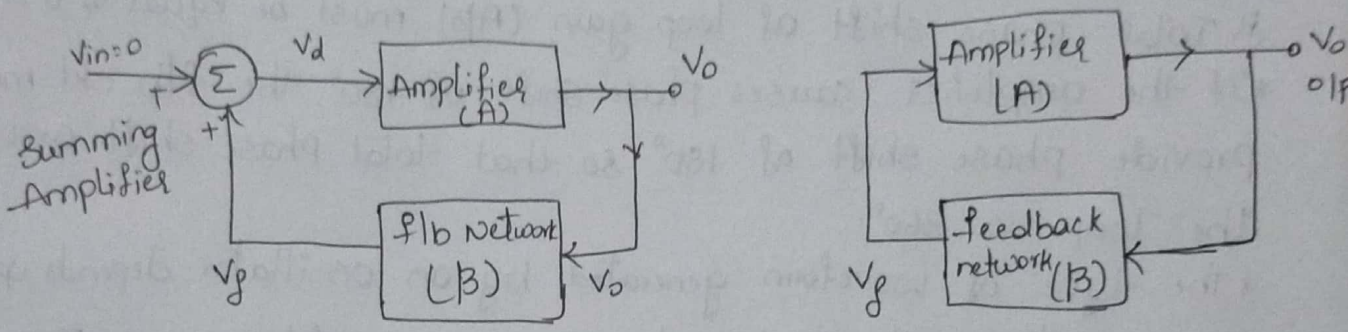
*The basic structure of sine-wave oscillator comprises of an Amplifier with gain 'A' and frequency selective feedback network with transfer ratio β.

*An oscillator is a ckt that generates repetitive waveform of fixed amplitude and frequency without any external input signal. It is used in radio, television, computers and communications.

*Principle :-

An oscillator is type of feedback amplifier in which part of output is feedback to input through feedback circuit.

* If signal feedback is of proper magnitude and phase ckt produces alternating currents (or) voltages



Block Diagram.

* Here the input voltage is zero ($V_{in}=0$) It uses positive f/b.

Gain with positive f/b:

$$V_d = V_{in} + V_f.$$

A → open loop gain

β - feedback ratio.

Also $A = \frac{V_o}{V_d} \Rightarrow V_o = AV_d$

$$\beta = \frac{V_f}{V_o} \Rightarrow V_f = \beta V_o$$

$$\therefore V_d = \beta V_o + V_{in}$$

$$\frac{V_o}{A} = \beta V_o + V_{in}$$

$V_o = A\beta V_o + V_{in}$ (A)

$V_o[1 - A\beta] = AV_{in}$

$$A_f = \frac{V_o}{V_{in}} = \frac{A}{1 - A\beta}$$

for $V_{in} = 0$ & $V_o \neq 0 \Rightarrow \boxed{A\beta = 1}$

In polar form, $A\beta = 1 \angle 0^\circ$ or 360°

* Barkhausen criterion :-

- The oscillator should satisfy two conditions for sustained oscillation

(i) Magnitude of (or) product of feedback factor and loop gain $A\beta$ must be equal to unity $|A\beta| = 1$

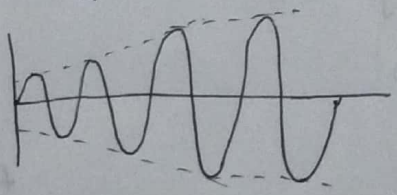
(ii) Total phase shift of loop gain $(A\beta)$ must be equal to 0° or 360°

* If the amplifier causes phase shift of 180°, the f/b ckt must provide phase shift of 180° so that total phase shift around the loop is 360°.

* The type of waveform generated by an oscillator depends upon components in the ckt and may be sinusoidal, square (or) Triangular

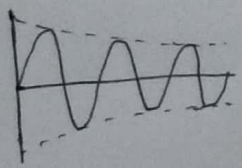
(i) $|A\beta| > 1$

for $|A\beta| > 1$ the o/p oscillates but produces growing type oscillations.



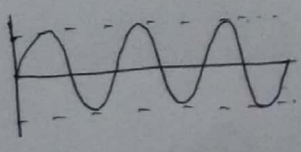
(ii) $|A\beta| < 1$

for $|A\beta| < 1$ the o/p oscillates but produces decaying type oscillations.



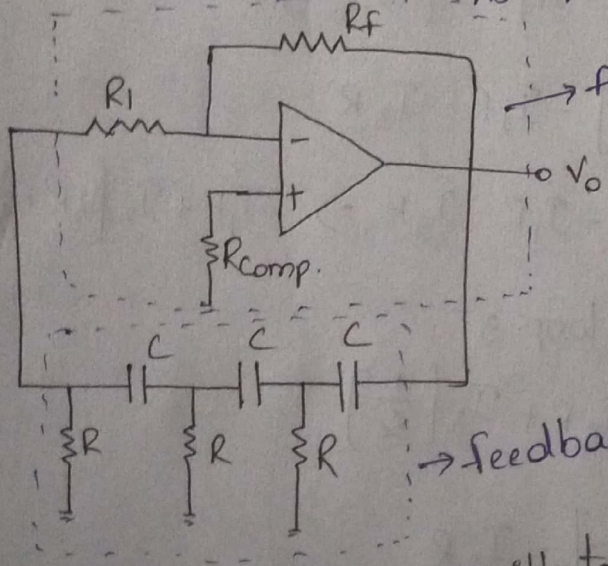
(iii) $|A\beta| = 1$

for $|A\beta| = 1$, the o/p oscillates but produces sustained type oscillations



*Rc phase shift oscillators :-

* The Rc phase shift oscillator circuits of an op-Amp as amplifying stages and three Rc cascaded networks as feedback circuit. The feedback circuit provides f/b voltages from the o/p back to i/p of the amplifier.
* An op-Amp used in Inverting mode and provides 180° phase shift. An additional 180° phase shift is provided by cascaded Rc n/w to obtain total phase shift around closed loop as 360° (or) 0°.
* The f/b n/w consists of three identical Rc stages. Each of Rc phase shift stages provides 60° phase-shift such that total phase shift due to f/b n/w is 180°.



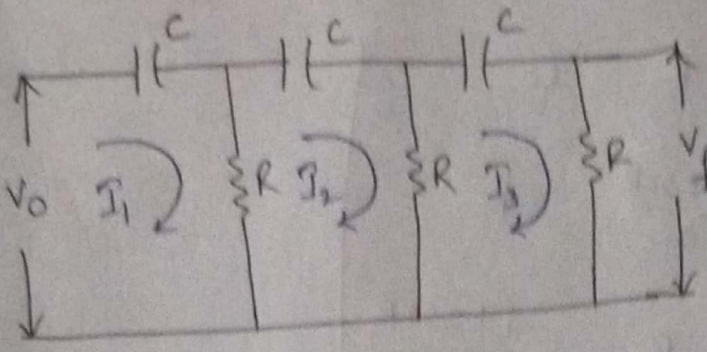
Rc phase shift oscillator.

*Frequency of oscillations :-

At particular frequency when phase shift of caused Rc network is exactly 180° and gain of amplifier is sufficiently large the ckt will oscillates at that frequency. This freq. is called frequency of oscillations.

*Derivation for frequency of oscillations :-

Transfer function of Rc f/b network.



Applying KVL at loop-1

$$V_0 = I_1\left[\frac{1}{j\omega c}\right] + [I_1 - I_2]R$$

$$V_0 = I_1\left[R + \frac{1}{j\omega c}\right] - I_2 R.$$

Applying KVL at loop-2

$$0 = (I_2 - I_1)R + I_2\left[\frac{1}{j\omega c}\right] + [I_2 - I_3]R$$

$$0 = -I_1 R + I_2\left[R + R + \frac{1}{j\omega c}\right] - I_3 R$$

$$0 = -I_1 R + I_2\left[2R + \frac{1}{j\omega c}\right] - I_3 R$$

Applying KVL at loop-3

$$0 = (I_3 - I_2)R + I_3\left[\frac{1}{j\omega c}\right] + I_3(R)$$

$$0 = -I_2 R + I_3\left[R + R + \frac{1}{j\omega c}\right]$$

$$0 = -I_2 R + I_3\left[2R + \frac{1}{j\omega c}\right]$$

Replacing $s = j\omega$. writing eqn's in matrix form, we have

$$\begin{matrix} & I_1 & I_2 & I_3 \end{matrix}$$

$$\begin{bmatrix} \left[R + \frac{1}{sc}\right] & -R & 0 \\ -R & \left[2R + \frac{1}{sc}\right] & 0 \\ 0 & -R & \left[2R + \frac{1}{sc}\right] \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} V_0 \\ 0 \\ 0 \end{bmatrix}$$

Using cramers rule to obtain I_3.

$$D = \begin{bmatrix} \frac{1+SRC}{SC} & -R & 0 \\ -R & \frac{1+2SCR}{SC} & -R \\ 0 & -R & \frac{1+2SCR}{SC} \end{bmatrix}$$

$$= \left[\frac{1+SCR}{SC}\right]\left[\left(\frac{1+2SCR}{SC}\right)\left(\frac{1+2SCR}{SC}\right) - (-R)(-R)\right] + R\left[(-R)\left[\frac{1+2SCR}{SC}\right] - 0\right] + 0.$$

$$= \frac{(1+SCR)}{SC}\left[\frac{(1+2SCR)^2}{(SC)^2} - R^2\right] + R\left[\frac{-R(1+2SCR)}{SC}\right] + 0$$

$$= \frac{(1+SCR)(1+2SCR)^2}{S^3C^3} - \frac{R^2(1+SCR)}{SC} - \frac{R^2(1+2SRC)}{SC} + 0.$$

$$= \frac{(1+SCR)(1+4SRC+4S^2R^2C^2)}{S^3C^3} - \left[\frac{R^2+3CR^3+R^2+2SCR^3}{SC}\right]$$

$$= \frac{1+4SRC+4S^2R^2C^2+SCR+4S^2R^2C^2+4S^3R^3C^3 - [R^2S^2C^2 + 3S^3C^3R^3]}{S^3C^3}$$

$$= \frac{1+5SCR+8S^2C^2R^2+4S^3C^3R^3-2R^2S^2C^2-3S^3C^3R^3}{S^3C^3}$$

$$D = \frac{1+5SRC+6S^2R^2R^2+S^3R^3C^3}{S^3C^3}$$

for $I_3 = \frac{D_3}{D}$.

$$D_3 = \begin{bmatrix} \frac{1+SRC}{SC} & -R & V_0 \\ -R & \frac{1+2SRC}{SC} & 0 \\ 0 & -R & 0 \end{bmatrix}$$

$$= \left(\frac{1+SRC}{SC}\right)(0-0) + R(0-0) + V_0[(-R)(-R) - 0]$$

$$D_3 = V_0 R^3$$

$$\boxed{V_f = I_3 R}$$

$$V_f = I_3 R = \frac{D_3}{D} R = \frac{V_0 R^3 S^3 C^3}{1 + 5SCR + 6S^2R^2C^2 + S^3C^3R^3}$$

Substituting value of I_3 in V_0 then

$$\beta = \frac{V_f}{V_0} \Rightarrow V_f = \beta V_0.$$

$$\beta = \frac{S^3R^3C^3}{1 + 5SCR + 6S^2R^2C^2 + S^3R^3C^3}$$

Replacing $s = j\omega$; s^2 by $(j\omega)^2 = -\omega^2$, s^3 by $(j\omega)^3 = (-j\omega^3)$

$$\beta = \frac{-j\omega^3 R^3 C^3}{1 + 5j\omega CR - 6\omega^2C^2R^2 - j\omega^3R^3C^3}$$

Dividing Numerator and denominator by $-j\omega^3R^3C^3$ then

$$\left[\alpha = \frac{1}{\omega RC}\right]$$

$$\beta = \frac{1}{1 + 6j\alpha - 5\alpha^2 - j\alpha^3}$$

$$\frac{1}{\frac{1+5j\omega CR}{-j\omega^3R^3C^3} - \frac{6\omega^2C^2R^2}{-j\omega^3R^3C^3} - \frac{j\omega^3R^3C^3}{-j\omega^3R^3C^3}}$$

$$\frac{1}{1 - \frac{6}{j\omega RC} + \frac{5}{\omega^2R^2C^2} - \frac{1}{j\omega^3R^3C^3}}$$

$$\beta = \frac{1}{[1-5\alpha^2]+j\alpha[6-\alpha^2]}$$

To have phase shift of 180° imaginary part of Deromirator must be zero.

$$\alpha[6-\alpha^2]=0 \Rightarrow \alpha^2=6 \Rightarrow \boxed{\alpha=\sqrt{6}.}$$

$$\frac{1}{\omega RC} = \sqrt{6}.$$

$$\omega = \frac{1}{RC\sqrt{6}.} \Rightarrow 2\pi f = \frac{1}{RC\sqrt{6}.}$$

$$\boxed{f = \frac{1}{2\pi RC\sqrt{6}}}$$

* Expression for gain :-

Imaginary part is zero.

$$\beta = \frac{1}{1-5(6^2)}$$

$$\beta = \frac{1}{1-5(6)} = \frac{1}{1-30} = -\frac{1}{29}.$$

$$|\beta| = \frac{1}{29}$$

for sustained oscillations

$$|A\beta| \geq 1$$

$$|A||\beta| \geq 1$$

$$|A| \geq \frac{1}{|\beta|} \geq \frac{1}{1/29}$$

$$\boxed{|A| \geq 29}$$

for oscillations to occur gain of OP-Amp must be equal to (or) greater than 29, which can be adjusted using the resistors R_f & R_1

*Advantages:-

- Circuit is simple to design
- Produces o/p over Af range
- Produces sinusoidal waveform as o/p.
- It is fixed frequency oscillators.

*Disadvantages:-

- The frequency stability is poor due to the change in values of various components due to effect of temp. aging etc.

*for an RC phase shift oscillator ckt with identical phase-shift n/w of $R = 10k\Omega$, $C = 0.01\mu f$ used. Determine the frequency of oscillations.

$R = 10k\Omega$

$C = 0.01\mu f$

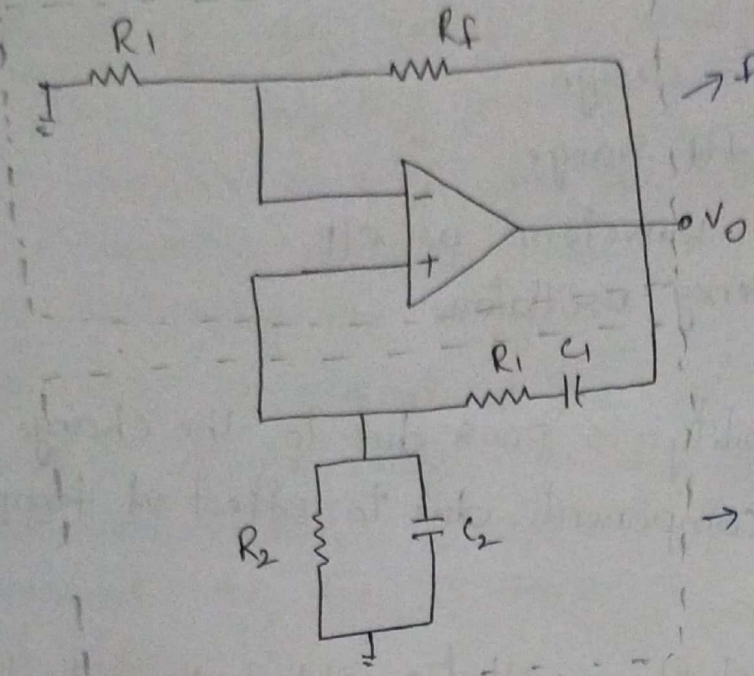
$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$= \frac{1}{2 \times 3.14 \times 10 \times 10^3 \times 0.01 \times 10^{-6} \times \sqrt{6}}$$

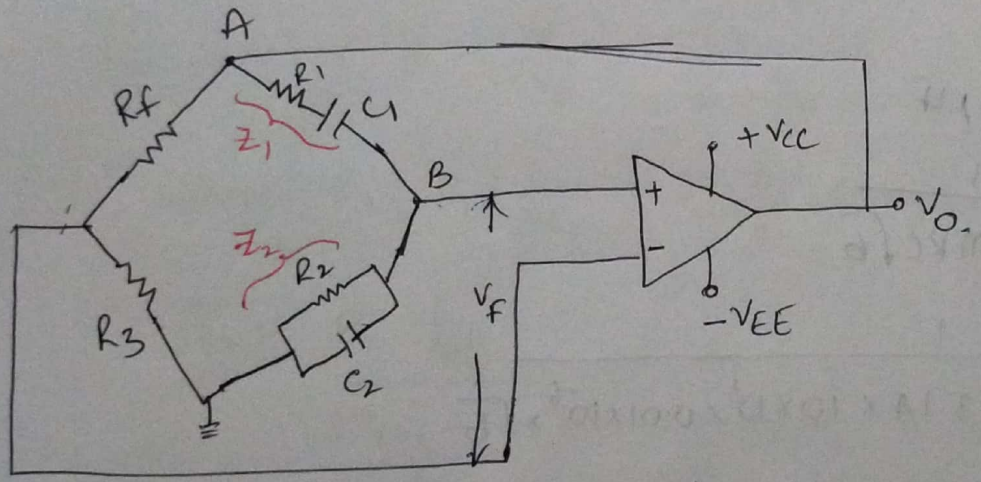
$$\boxed{f = 6.497\ KHz.}$$

*Wein Bridge oscillator :-

• Wien bridge oscillator becomes the most popular audio frequency range signal generator circuit.



Wein bridge oscillator.



Wein bridge oscillator showing bridge network.

*The wein bridge ckt is connected blw the amplifier i/p and o/p terminal. The f/b n/w is called lead-lag while at low frequency it acts like lead while at high frequency it acts as lag n/w.

* The feedback signal in this ckt is connect to non-Inverting i/p terminal so that the op-Amp working as a non-Inverting Amplifier.
* The f/b n/w need not provide any phase-shift. The Wien bridge has series Rc n/w in one arm & parallel Rc n/w in adjoining arm.
* The resistors R_3 & R_f are connected in remaining two arms. The condition of zero phase shift around the ckt is achieved by balancing the bridge.
* The o/p Ac signal of the op-Amp amplifier is f/b to point A of the bridge. The f/b signal V_f across the paralled combination R_2C_2 is applied to the non-Inverting i/p terminal of the op-Amp.
* Analysis:-

Gain of op-Amp is given by

$$A = 1 + \frac{R_f}{R_1}$$

f/b factor $\beta = \frac{V_f}{V_o} = \frac{Z_2}{Z_1 + Z_2}$

where $Z_1 = R_1 + \frac{1}{SC_1} = \frac{SC_1R_1 + 1}{SC_1}$

$$Z_2 = \frac{R_2 \frac{1}{SC_2}}{\frac{SR_2C_2 + 1}{SC_2}} = \frac{R_2}{1 + SR_2C_2}$$

Sub. values of Z_1 & Z_2 we get

$$\beta = \frac{\frac{R_2}{(1+SR_2C_2)}}{\left(\frac{1+SC_1R_1}{SC_1}\right) + \left(\frac{R_2}{1+SR_2C_2}\right)}$$

$$= \frac{\frac{R_2}{(1+sR_2C_2)}}{\frac{(1+sR_1C_1)(1+sR_2C_2)+R_2sC_1}{(sC_1)(1+sR_2C_2)}}$$

$$\beta = \frac{sR_2C_1}{1+s(R_1C_1+R_2C_2+R_2C_1)+s^2R_1R_2C_1C_2}$$

put $s = j\omega$

$$\beta = \frac{j\omega R_2C_1}{1+j\omega(R_1C_1+R_2C_2+R_2C_1)-\omega^2R_1R_2C_1C_2}$$

for β to be real quantity

real part = 0

$$1-\omega^2R_1R_2C_1C_2 = 0$$

$$\omega^2R_1R_2C_1C_2 = 0$$

$$\omega^2 = \frac{1}{R_1R_2C_1C_2}$$

$$\omega = \frac{1}{\sqrt{R_1R_2C_1C_2}}$$

$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

let $R_1 = R_2 = R$; $C_1 = C_2 = C$

$$\boxed{f_0 = \frac{1}{2\pi RC}}$$

Condition for oscillations

$$\beta = \frac{R_2 C_1}{R_1 C_1 + R_2 C_2 + R_2 C_1} \quad [\text{real part} = 0]$$

for $R_1 = R_2 = R$ & $C_1 = C_2 = C$

$$\beta = \frac{RC}{3RC} = \frac{1}{3}$$

$|A\beta| \geq 1$ [sustained oscillations]

$|A| \geq 3$. [$\because |A||B| \geq 1 \Rightarrow |A||1/3| \geq 1$]

Here $A = 1 + \frac{R_f}{R_1} = 3$

$$\frac{R_f}{R_1} = 3 - 1 \Rightarrow \frac{R_f}{R_1} = 2 \Rightarrow \boxed{R_f = 2R_1}$$

*Advantages:-

- The ckt provides good frequency stability.
- It provides sinusoidal waveform.

*Disadvantages:-

- The circuit cannot generate very high frequencies.

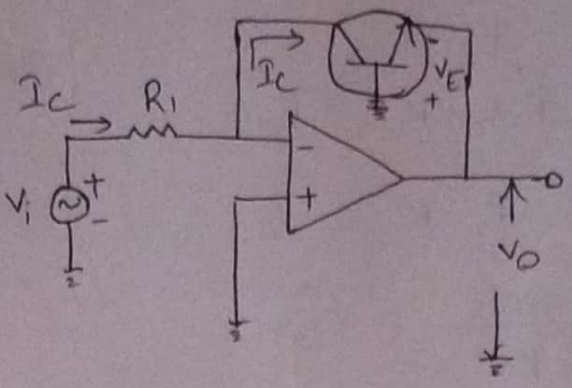
*Log and Antilog Amplifier:-

- There are several applications of logs and antilogs Amplifies. Antilog computation requires functions like $\ln x$, $\log x$, $\sin$.
- log Amplifiers used to compress dynamic range of signal and also used in digital voltmeter and spectrum analyser.
- log and Antilog amplifiers are useful in signal compression, Multiplication and division of signals, finding roots and power of signal.

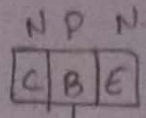
*Log Amplifier :-

The log amp ckt consists of a ground base transistor placed in feedback path.

*Since the collector is held at virtual ground and base is also grounded, the transistors voltage and current relationship becomes similar to that of diode and given by



Fundamental Log-Amp circuit.



As base is connected to gnd the transistor acts as a diode.

$$I_E = I_S \left[e^{qV_E/KT} - 1 \right]$$

Since $I_C \cong I_E$ for grounded base transistor.

$$I_C = I_S \left[e^{qV_E/KT} - 1 \right]$$

where I_S - Emitter saturation current.

k - Boltzmann's constant

T - Absolute Temperature.

$$\therefore \frac{I_C}{I_S} = \left[e^{qV_E/KT} - 1 \right]$$

$$e^{qV_E/KT} = \frac{I_C}{I_S} + 1 \qquad \left[\frac{I_C}{I_S} + 1 \cong \frac{I_C}{I_S} \right]$$

$$e^{qV_E/KT} = \frac{I_C}{I_S}$$

Taking natural log on both sides then

$$\frac{qV_E}{KT} = \ln \left[\frac{I_C}{I_S} \right]$$

$$V_E = \frac{KT}{q} \ln \left[\frac{I_C}{I_S} \right]$$

Also $I_C = \frac{V_i}{R_1}$

and $V_E = -V_o$

$$V_o = -\frac{kT}{q} \ln\left[\frac{V_i}{I_S R_1}\right]$$

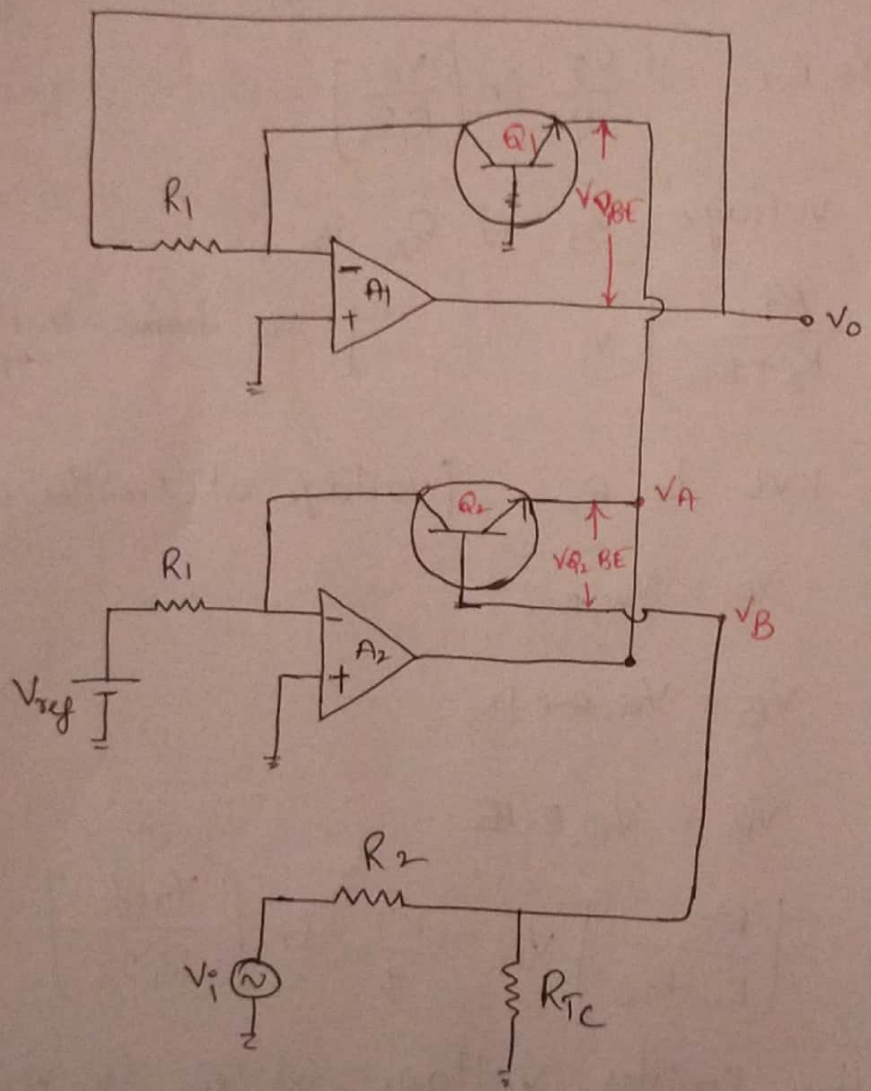
(or)

$$V_o = -\frac{kT}{q} \ln\left[\frac{V_i}{V_{ref}}\right]$$

$V_{ref} = R_1 I_S$

The o/p voltage is proportional to the logarithm of the i/p voltage.

* Anti log Amplifier:-



Anti log Amplifier.

* The i/p V_i for the antilog Amplifier is fed into the temperature compensating voltage divider R_2 & R_{TC} and then to base of Q_2
* The o/p V_o of antilog Amplifier is feedback to Inverting i/p of A_1 through resistor R_1.
* The base to Emitter voltage of transistor Q_1 & Q_2 written as.

$$V_{Q_1\,B\text{-}E} = \frac{KT}{q} \ln\left[\frac{V_o}{R_1 I_S}\right]$$

$$V_{Q_2\,B\text{-}E} = \frac{KT}{q} \ln\left[\frac{V_{ref}}{R_1 I_S}\right]$$

Since the base Q_1 is tied to ground we get

$$V_A = -V_{Q_1\,B\text{-}E} = -\frac{KT}{q} \ln\left[\frac{V_o}{R_1 I_S}\right]$$

The base voltage V_B of Q_2 is

$$V_B = \left[\frac{R_{TC}}{R_2 + R_{TC}}\right] V_i$$ [V_B ~~form~~ - voltage divider apply]

Applying KVL to Q_2 [voltage at Emitter of Q_2]

~~$+V_{Q_2\,B\text{-}E} = V_B + V_{Q_1\,B\text{-}E}$~~

~~$V_{E_2} = V_B + V_{Q_2\,B\text{-}E}$~~ ×

$$V_{Q_2\,E\text{-}B} = V_B + V_{Q_2\,B\text{-}E}$$

$$V_{Q_2\,E\text{-}B} = \left(\frac{R_{TC}}{R_2 + R_{TC}}\right) V_i - \frac{KT}{q} \ln\left[\frac{V_{ref}}{R_1 I_S}\right]$$

But the Emitter voltage of Q_2 is V_A

$$V_A = V_{Q_2\,E\text{-}B}.$$

$$-\frac{KT}{q}\ln\left[\frac{V_o}{R_1 I_s}\right] = \left[\frac{R_{Tc}}{R_2+R_{Tc}}\right]V_i - \frac{KT}{q}\ln\left[\frac{V_{ref}}{R_1 I_s}\right]$$

$$\left[\frac{R_{Tc}}{R_2+R_{Tc}}\right]V_i = \frac{KT}{q}\ln\left[\frac{V_{ref}}{R_1 I_s}\right] - \frac{KT}{q}\ln\left[\frac{V_o}{R_1 I_s}\right]$$

$$\left[\frac{R_{Tc}}{R_2+R_{Tc}}\right]V_i = \frac{-KT}{q}\ln\left[\frac{V_o}{R_1 I_s} - \frac{V_{ref}}{R_1 I_s}\right]$$

$$-\frac{q}{KT}\left[\frac{R_{Tc}}{R_2+R_{Tc}}\right]V_i = \ln\left[\frac{V_o}{V_{ref}}\right] \qquad \left[\because \ln[a-b] = \ln\left[\frac{a}{b}\right]\right.$$

changing natural log (i.e) ln to $\log_{10}$, we get

Multiply by 0.4343 on both sides

$$(-0.4343)\underbrace{\frac{q}{KT}\left[\frac{R_{Tc}}{R_2+R_{Tc}}\right]}_{k'}V_i = 0.4343\ln\left[\frac{V_o}{V_{ref}}\right]$$

↓ This can be written as $\log_{10}$

$$-k'V_i = \log_{10}\left[\frac{V_o}{V_{ref}}\right]$$

$$\frac{V_o}{V_{ref}} = 10^{-k'V_i}$$

$$\boxed{V_o = V_{ref}\left[10^{-k'V_i}\right]}$$

Thus an increase of i/p by 1 Volt causes the o/p decreases by decade.

*Multiplier and Divider :-

• Analog Multiplier :-

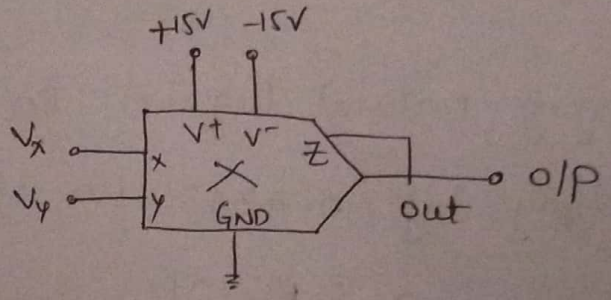
There are number of applications of Analog Multiplier

- Frequency doubling.
- Measurement of real power
- Detecting phase-angle difference b/w two signals of equal frequency.
- Multiplying two signals
- Dividing one signal by another.
- Taking square root.
- Squaring signal.

*Multiplier :-

Two input signals V_x & V_y are provided

- The o/p is the product of two i/p's divided by reference voltage V_{ref}.



Multiplier symbol.

*Thus o/p voltage is scaled version of x & y i/p's. The o/p voltage given by

$$V_o = \frac{V_x V_y}{V_{ref}}.$$

V_{ref} - is Internally set to 10V

$$V_o = \frac{V_x V_y}{10}.$$

$V_x < V_{ref}$

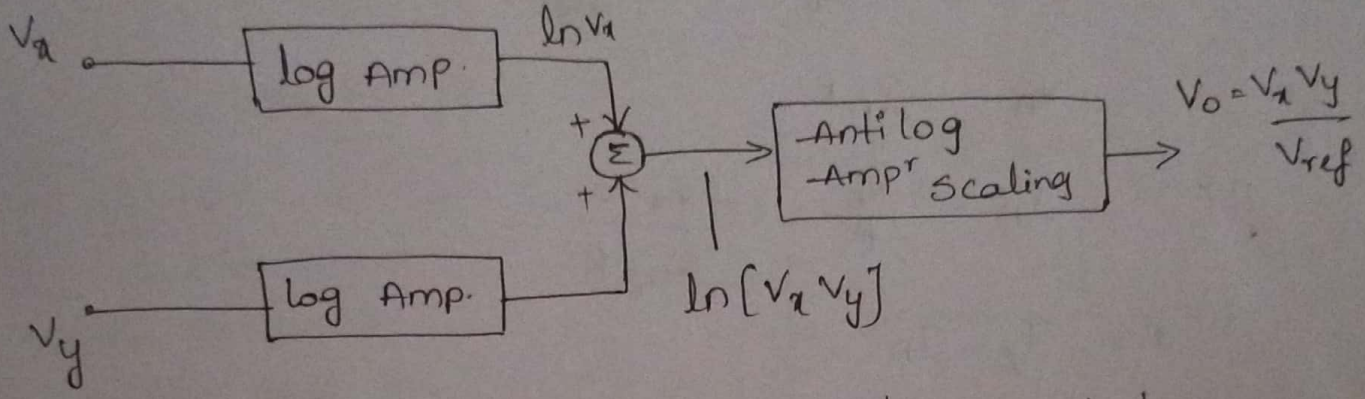
$V_y < V_{ref}$.

*If both the i/p's are positive, Ic is said to be one quadrant multiplier. If one i/p is held +ve & other altered to swing both +ve & -ve, Ic is called

two-quadrant multiplier. If both the i/p's are either +ve/-ve IC is called four-quadrant multiplier.

*The best way to make ckt to multiply two i/p's is log-antilog method. This method relies on mathematical relationship that sum of logarithm of two numbers equals logarithm of product of these numbers.

$$\ln V_x + \ln V_y = \ln [V_x \times V_y]$$



Block diagram of log-antilog multiplier.

*log Ampr require i/p's and reference voltage to be of some polarity. This restricts the log-anti log multipliers to one-quadrant operation. A technique that provides four-quadrant multiplication is transconductance multiplier AD 533, AD 534, AD 633 → ICs

*Divider:-

*Division, the complement of multiplication can be accomplished by placing the multiplier ckt element in OP-Amp's feedback loop.

*The o/p voltage of divider with the i/p signals V_z & V_x as divident & divisor respectively is given by

$$V_o = -V_{ref} \cdot \frac{V_z}{V_x}$$

Proof :- Op-Amp inverting terminal is at virtual ground.

$$\therefore I_Z = I_A$$

$$I_Z = \frac{V_Z}{R}$$

o/p voltage V_A of multiplier is determined by multiplication of V_x & V_y

$$V_A = \frac{V_x V_y}{V_{ref}} = \frac{V_x V_o}{V_{ref}}$$

$$V_A = -I_A R$$

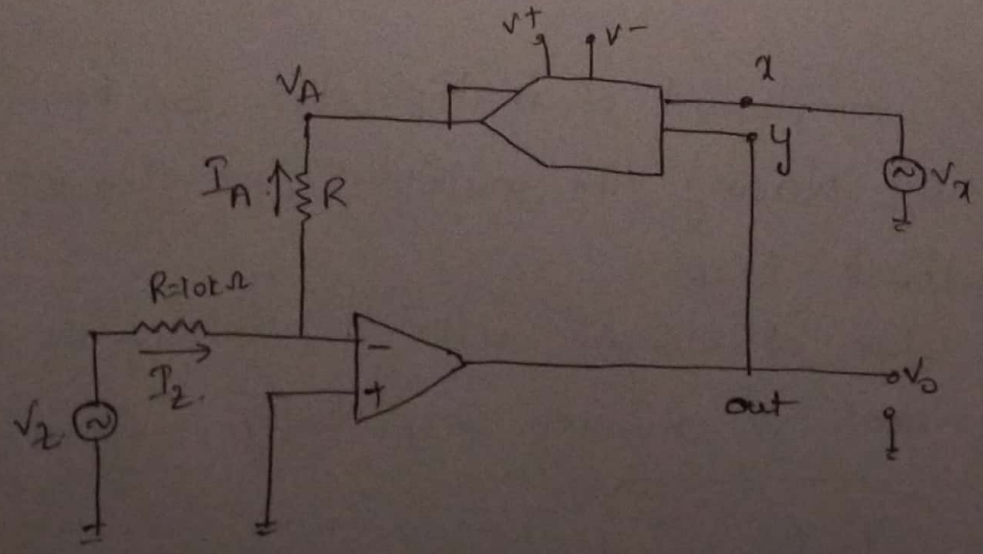
$$I_A = \frac{-V_A}{R} = \frac{-V_x V_o}{V_{ref} \cdot R}$$

As $I_Z = I_A$

$$I_Z = \frac{-V_x V_o}{V_{ref} R}$$

$$V_Z = I_Z R = \frac{-V_x V_o}{V_{ref}}$$

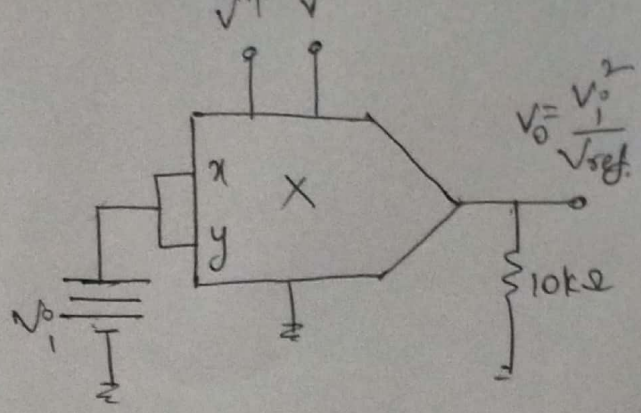
$$\boxed{V_o = -V_{ref} \cdot \frac{V_Z}{V_x}}$$



Multiplier IC configured as divider.

*squaring ckt:-

The basic multiplier can be used to square any +ve or -ve number provider. The number can be represented by a voltage blw 0 to V_{ref}.

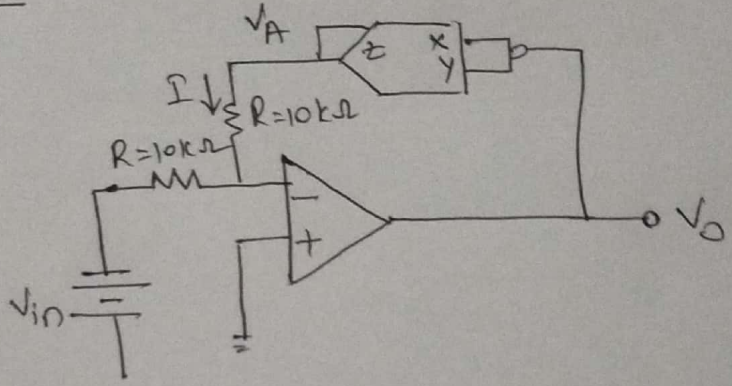


squaring ckt.

The voltage V_i representing the number is connected both the i/p's.

*finding square root:-

A Divider ckt can be used to find square-roots by connecting both the i/ps of multiplier to o/p of an op-Amp.



from figure

$$V_A = \frac{V_o^2}{V_{ref}} \quad \therefore V_o^2 = -V_{in} V_{ref}.$$

& $V_A = -V_{in}$ $\qquad V_o = \sqrt{V_{ref}|V_{in}|}$

Thus o/p voltage V_o is proportional to square root of magnitude of V_{in}.

MODULE - 3

FILTER, TIMER AND PLL.

*Filter :- Def :- Filters are circuits that are capable of passing signals within a band of frequencies while rejecting (or) attenuating or blocking signals of frequencies outside this band. This property of filters is also called "frequency selectivity".

*Passive filters :- The circuit built using Rc, RL, or RLC ckts.

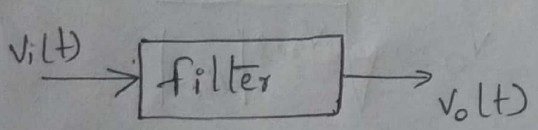
*Active filters :- The ckt that employs one or more Op-amps in the design an addition to resistors and capacitors.

*Rc filters used for audio or low frequency operation while Lc filters used for radio frequency operation. Crystals provide stable operation at higher frequencies.

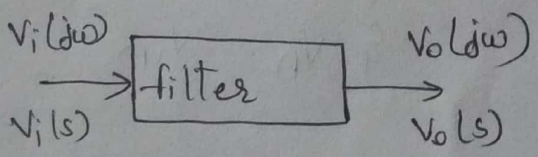
*Digital filters :- Digital filters are implemented using a digital computer or special purpose digital hardware.

*Analog filters :- Analog filters may be classified as either passive or active and are usually implemented with R, L and C components and operational Amplifiers.

*Representation of filter :-



Time domain



frequency domain.

The filter can be represented in time domain and frequency domain as shown in figure.

The filter can easily analyzed in frequency domain The transfer function of filter is ratio of laplace transform of olp voltage to laplace transform of input voltage.

$H(s) = \frac{V_o(s)}{V_i(s)}$ $\quad H(j\omega) = \frac{V_o(j\omega)}{V_i(j\omega)}$

In polar form

$H(j\omega) = |H(j\omega)| e^{j\theta(\omega)}$

where $|H(j\omega)|$ is Magnitude or gain function.

$\theta(\omega)$ is phase function.

*Advantages of Active filters over Passive

- Active filters can be designed to provide required gain and hence no attenuation as in the case of Passive filters.
- No loading effect, because of high input resistance and low output resistance of op-Amp.
- Active filters are cost effective as wide variety of economical op-amps are available.

*Application of Active filters :-

- Active filters are mainly used in communication and signal processing circuits.
- They are also employed in a wide range of applications such as entertainment, medical electronics etc.

*The most commonly used filters :-

(i) Low-Pass filter

(ii) High-pass filter

(iii) Band-pass filter

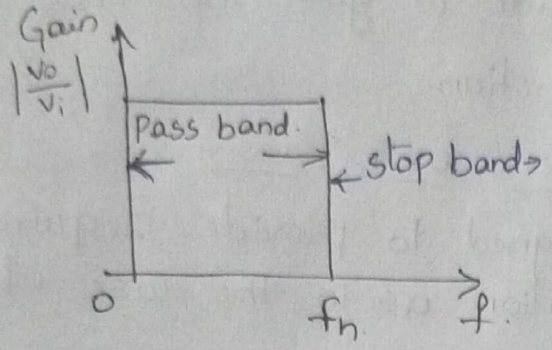
(iv) Band-Reject filter

(v) All pass filter.

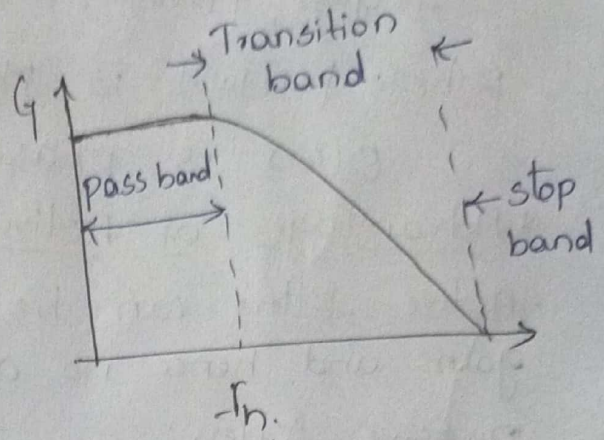
* Ideal and Practical characteristics of filter :-

(i) Low Pass filter :-

A low pass filter allows low frequency signals and attenuates all other frequency.



Ideal.



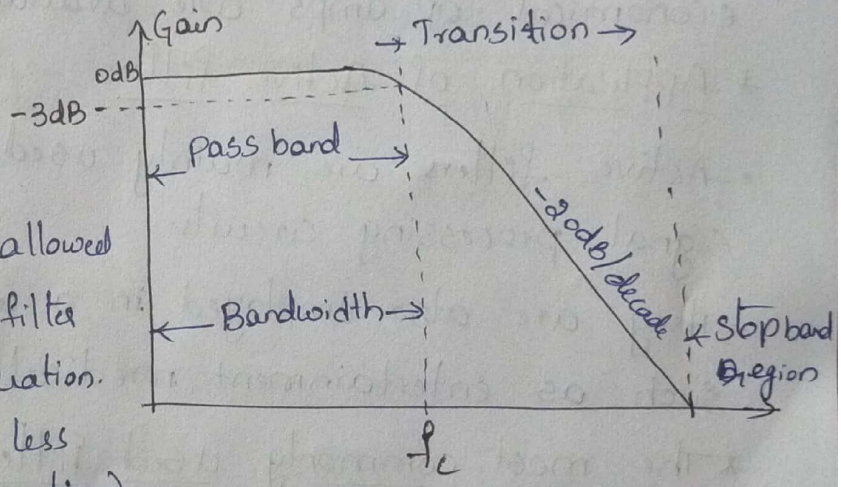
Practical.

Pass band $0 < f < f_h$

Stop band $f > f_h$.

*Pass band :-

Pass band of a filter is the range of frequencies that are allowed to pass through the filter with minimum attenuation. (usually defined as less than -3dB of attenuation).

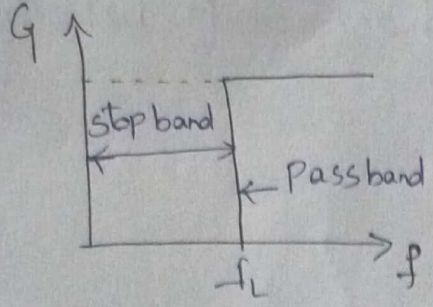


• Transition region :- The transition region where the fall-off occurs.

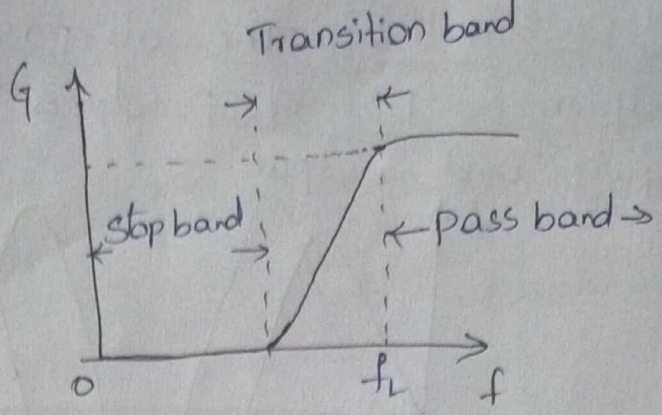
• stop band :- stop band is the range of frequencies that have the most attenuation.

* Critical frequency, f_c (also called the cutoff frequency) defines the end of the passband and normally specified at the point where the response drops -3dB [70.7%] from the pass band response.

* High pass filter :-



Ideal.

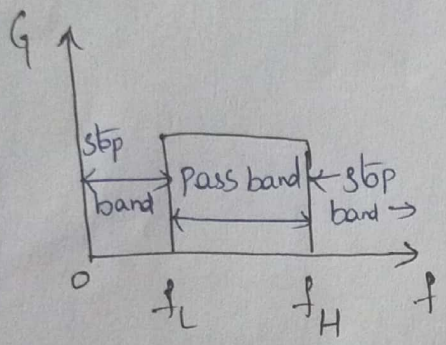


Practical.

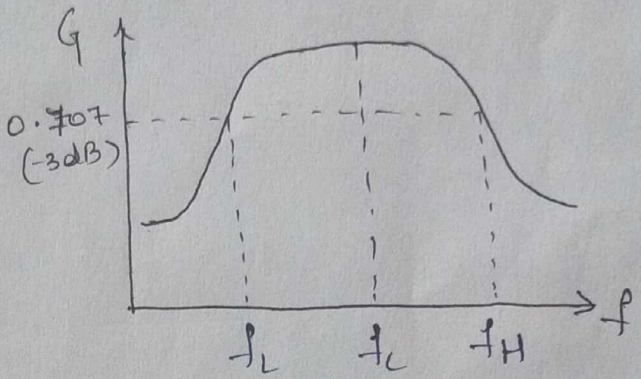
Passband : $f > f_L$

stop band $0 < f < f_L$

* Band pass filter :-



Ideal.



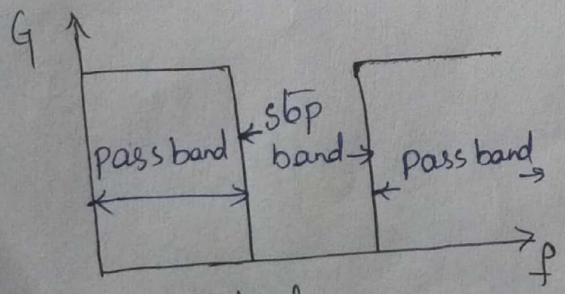
Practical.

Pass band $f_L < f < f_H$

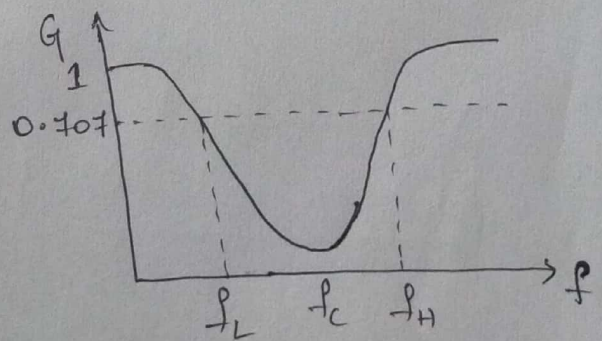
stop band ① $0 < f < f_L$

② $f_H < f < \infty$.

* Band stop (or) Band reject filter :-



Ideal.



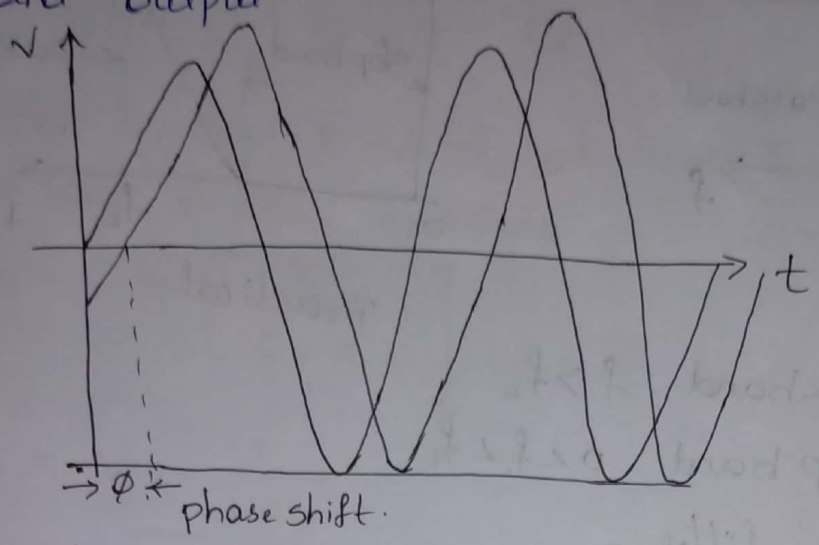
Practical.

Pass band ① $0 < f < f_L$

② $f_H < f < \infty$.

stop band $f_L < f < f_H$.

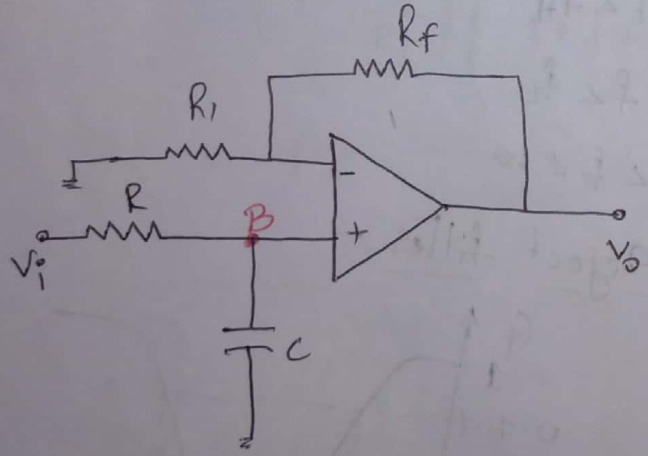
*All pass filter :- The all pass filters passes all the frequencies but it produces the phase shift between input and output.



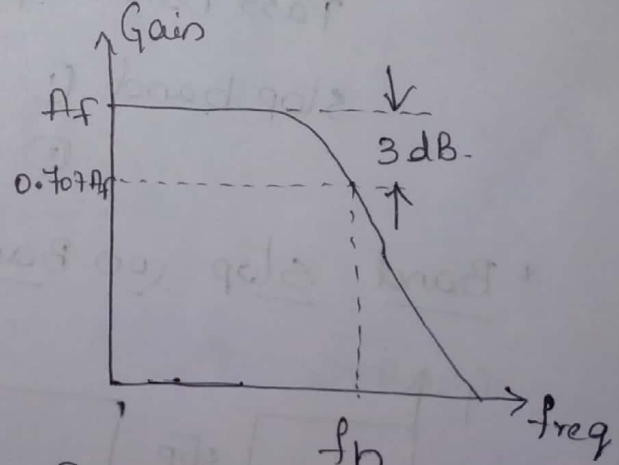
*First order low pass filter : [Butterworth low pass filter] :-

A first order filter consists of a single RC network connected to the (+ve) input terminal of OP-Amp.

- The resistors R_1 & R_f determines the gain of the filter in pass band.
- Allowing the flatest possible pass band, this filter is generally the most popular in use.



First order lpf.



frequency Response.

- low pass filter allows low frequencies and attenuates high frequencies.

The output voltage expression for non-Inverting op-Amp. i.e The closed loop gain of the op-Amp is

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_B \quad \text{— (1)}$$

where V_B is the potential at +ve input terminal i.e voltage across capacitor.

$$V_B = V_i \left\{ \frac{X_C}{R + X_C} \right\}$$

$$\left[X_C = \frac{1}{j\omega_c} \right]$$

$$= V_i \cdot \frac{\frac{1}{j\omega C}}{R + \frac{1}{j\omega C}}$$

$$V_B = V_i \times \frac{1}{1 + j\omega RC} \quad \text{— (2)}$$

Sub. eqn (2) in eqn (1),

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_i \times \frac{1}{1 + j\omega RC}$$

$$\frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right] \left[\frac{1}{1 + j\omega RC} \right]$$

$$\frac{V_o}{V_i} = A_f \cdot \frac{1}{1 + j\omega RC} \Rightarrow \frac{A_f}{1 + j 2\pi f RC}$$

$$\therefore \boxed{\frac{V_o}{V_i} = \frac{A_f}{1 + j\left[f / f_h\right]}}$$

let $f_h = \frac{1}{2\pi RC}$

where A_f = pass band gain $\left(1 + \frac{R_f}{R_1}\right)$

f = operating frequency

f_h = high cut off freq. = $\frac{1}{2\pi RC}$

Magnitude of gain $\left| \frac{V_o}{V_i} \right| = \frac{A_f}{\sqrt{1 + (f/f_h)^2}}$

phase angle $\theta = -\tan^{-1}[f/f_h]$

- At very low frequencies i.e $f < f_h$

$$\left|\frac{V_o}{V_i}\right| = A_f \quad \text{i.e constant.}$$

- At $f = f_h$, $\left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{2}} = 0.707 A_f$.
- At very high frequencies i.e $f > f_h$

$$\left|\frac{V_o}{V_i}\right| \simeq 0.$$

* The frequency response of 1st order LPF is shown in fig. It has max. gain A_f at $f = 0$ Hz.
* At $f = f_h$ the gain falls to 0.707 times the max. gain A_f
* The freq. range from 0 to f_h is called pass band gain
- for $f > f_h$ the gain decreases at a constant rate of -20 dB/decade.
- The freq. range $f > f_h$ is called stop band.

* Designing steps :-

1. choose the cutoff frequency.
2. choose capacitor value $\leq 1\mu f$.
3. find $R = \frac{1}{2\pi f_c}$
4. The resistance R_f & R_1 can be selected depending on the required gain in pass band.

$$A_f = 1 + \frac{R_f}{R_1}$$

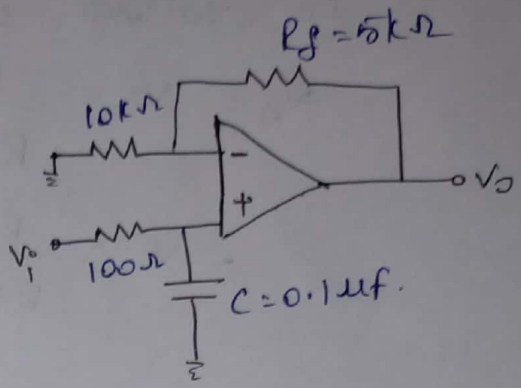
* Design a low pass filter at a cut off frequency of 15.9 kHz with a pass band gain 1.5.

Given $f_h = 15.9\,kHz$

$A_f = 1.5$

We know that $f_h = \frac{1}{2\pi RC}$

choose $R \cdot C = 0.1\,\mu f$, then $R = \frac{1}{2\pi f_c}$



$$R = \frac{1}{2 \times 3.14 \times 15.9 \times 10^3 \times 0.1 \times 10^{-6}}$$

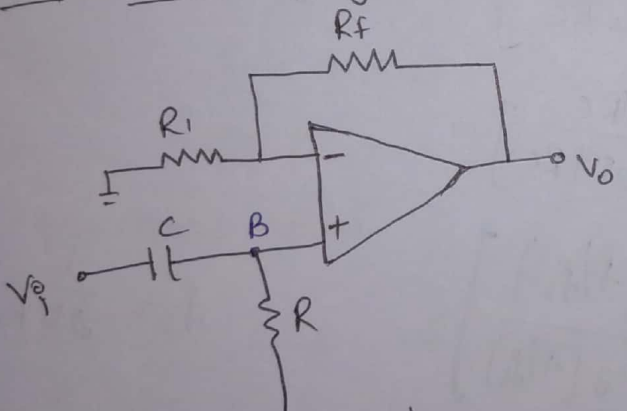
$R = 100\Omega$

We know that $A_f = 1 + \frac{R_f}{R_1} = 1.5$

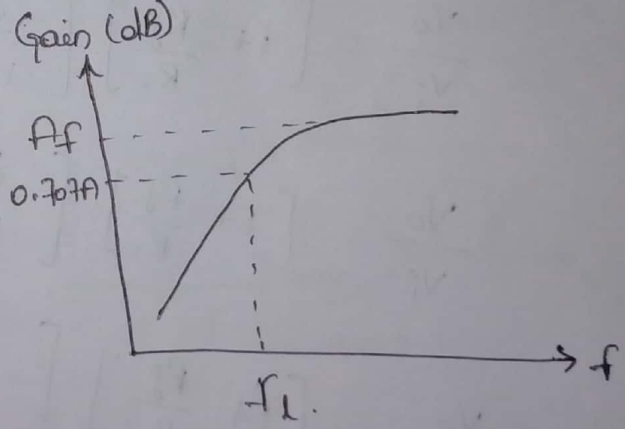
$\frac{R_f}{R_1} = 0.5$

Assume $R_1 = 10k\Omega$ then $R_f = 5k\Omega$

*first order High pass filter:-



High pass filter



frequency response.

* HPf allows high frequencies and rejects low frequencies.

The 1st order HPf formed by interchanging frequency.

* The 1st order HPf with a lower cut-off frequency f_L. At f_L the magnitude of gain is 0.707 times its pass band value.

The output voltage of non-Inverting OP-Amp is

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_B \quad -(1)$$

Where V_B is the potential at +ve i/p terminal.

i.e voltage across resistor.

$$V_B = V_i \times \frac{R}{R + X_C}$$

$$= V_i \times \frac{R}{R + \frac{1}{j\omega C}}$$

$$V_B = V_i \times \frac{j\omega RC}{1 + j\omega RC} \quad -(2)$$

Sub eqn (2) in (1), we get.

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_i \times \frac{j\omega RC}{1 + j\omega RC}$$

$$\frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right] \left[\frac{j\omega RC}{1 + j\omega RC}\right]$$

$$\frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right] \left[\frac{j2\pi fRC}{1 + j2\pi fRC}\right]$$

$$\frac{V_o}{V_i} = \left[1 + \frac{R_f}{R_1}\right] \left[\frac{j(f/f_L)}{1 + j(f/f_L)}\right] \qquad \therefore f_L = \frac{1}{2\pi RC}$$

$$\therefore \frac{V_o}{V_i} = A_f \frac{[j(f/f_L)]}{1 + j(f/f_L)} \Rightarrow \left|\frac{V_o}{V_i}\right| = \frac{A_f (f/f_L)}{\sqrt{1 + (f/f_L)^2}}$$

Divide the both numerator & denominator with $[j(f/f_L)]$

$$\frac{V_o}{V_i} = A_f \frac{j(f/f_L)/j(f/f_L)}{\frac{1 + j(f/f_L)}{j(f/f_L)}}$$

$$\frac{V_o}{V_i} = A_f \cdot \frac{1}{1+\frac{1}{j(f/f_L)}}$$

$$= A_f \cdot \frac{1}{1+\frac{j}{(f/f_L)}} \Rightarrow \frac{V_o}{V_i} = \frac{A_f}{1-j(f_L/f)}$$

$$\left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{1+(f_L/f)^2}}$$

- At low frequencies i.e $f < f_L$, $\left|\frac{V_o}{V_i}\right| \simeq 0$

At $f = f_L$, $\left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{2}} = 0.707 A_f$

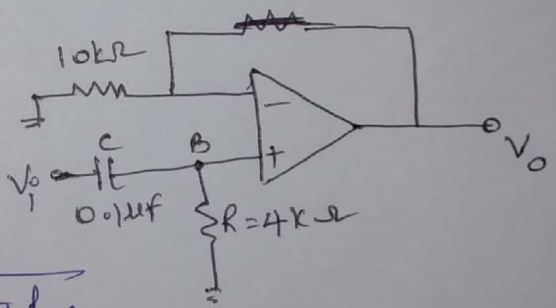
At Higher frequencies i.e $f > f_L$, $\left|\frac{V_o}{V_i}\right| = A_f$ i.e constant

The frequency range 0 to f_L is called 'stop band' and $f > f_L$ is called 'pass band'.

+ Design a 1st order HPF with a cutoff frequency of 400Hz & a pass band gain of 1

Given $f_L = 400Hz$

$A_f = 1$



We know that $f_L = \frac{1}{2\pi RC}$

choose $C = 0.1\mu f$, then $R = \frac{1}{2\pi f_L C}$

$$R = \frac{1}{2\times 3.14\times 400\times 0.1\times 10^{-6}} = 4k\Omega$$

We know that pass band gain $A_f = 1 + \frac{R_f}{R_1} = 1$

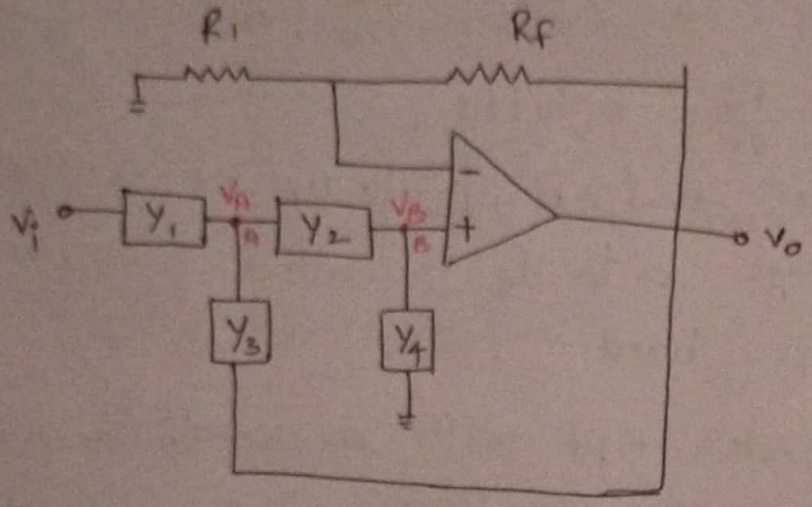
$$\frac{R_f}{R_1} = 0$$

Select $R_1 = 10k\Omega$

$R_f = 0$.

* Second order low pass Butterworth filter :-

- An improved filter response can be obtained by using second order active filter.
- The second order filter consists of two RC pairs and has a roll off rate of -40dB/decade. The general second-order filter called sallen-key filter.
- The cut off frequency of filter decided by Y_1, Y_2, Y_3, Y_4 while the gain of filter is decided by the resistors R_1 & R_f.



$i = \frac{V}{R}$

$i = V \times \frac{1}{R}$ → impedance

$i = V \times \frac{1}{Z}$

$i = V \times Y$

Y [admittance]

General second order [sallen key filter].

→ An OP-Amp is connected in non-Inverting mode.

$$V_o = \left[1 + \frac{R_f}{R_1}\right] V_B \quad — (1)$$

$$V_o = A_f V_B$$

$$V_B = \frac{V_o}{A_f} \quad — (2) \qquad \text{where } A_f = \left[1 + \frac{R_f}{R_1}\right].$$

Apply nodal Analysis at node 'A'

$$(V_A - V_i) Y_1 + (V_A - V_o) Y_3 + (V_A - V_B) Y_2 = 0.$$

$$V_A Y_1 - V_i Y_1 + V_A Y_3 - V_o Y_3 + V_A Y_2 - V_B Y_2 = 0$$

$$V_A [Y_1 + Y_2 + Y_3] - V_o Y_3 - \frac{V_o}{A_f} Y_2 = V_i Y_1 \qquad \left[\because V_B = \frac{V_o}{A_f}\right]$$

$$V_A [Y_1 + Y_2 + Y_3] - V_o Y_3 - \frac{V_o}{A_f} Y_2 = V_i Y_1 \quad — (3)$$

Apply nodal Analysis at node B.

$$(V_B - V_A)Y_2 + V_B Y_4 = 0.$$

$$V_B Y_2 - V_A Y_2 + V_B Y_4 = 0$$

$$V_B[Y_2 + Y_4] = V_A Y_2$$

$$V_A = \frac{V_B[Y_2 + Y_4]}{Y_2} \Rightarrow V_A = \frac{V_o}{A_f}\frac{(Y_2 + Y_4)}{Y_2} \quad -④ \quad \left[\because V_B = \frac{V_o}{A_f}\right]$$

Sub. Eqn ④ in Eqn ③

$$\frac{V_o(Y_2+Y_4)}{A_f Y_2}[Y_1+Y_2+Y_3] - V_o Y_3 - \frac{V_o Y_2}{A_f} = V_i Y_1$$

$$V_o\left[\frac{(Y_2+Y_4)}{A_f Y_2}[Y_1+Y_2+Y_3] - Y_3 - \frac{Y_2}{A_f}\right] = V_i Y_1$$

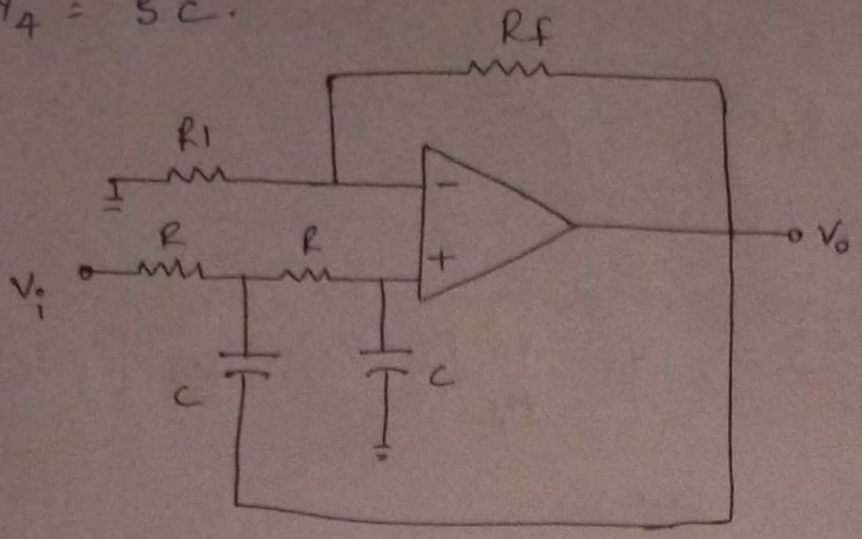
$$V_o\left[\frac{(Y_2+Y_4)(Y_1+Y_2+Y_3) - A_f Y_2 Y_3 - Y_2^2}{A_f Y_2}\right] = V_i Y_1$$

$$\frac{V_o}{V_i} = \frac{A_f Y_1 Y_2}{(Y_2+Y_4)(Y_1+Y_2+Y_3) - A_f Y_2 Y_3 - Y_2^2}$$

$$\frac{V_o}{V_i} = \frac{A_f Y_1 Y_2}{Y_1Y_2 + Y_2^2 + Y_2Y_3 + Y_1Y_4 + Y_2Y_4 + Y_3Y_4 - A_f Y_2 Y_3 - Y_2^2}$$

$$\frac{V_o}{V_i} = \frac{A_f Y_1 Y_2}{Y_1Y_2 + Y_2Y_3[1 - A_f] + Y_4[Y_1+Y_2+Y_3]}$$

To make second order LPF choose $Y_1, Y_2 = \frac{1}{R}$ & $Y_3 Y_4 = sC$.



choose $Y_1 = Y_2 = \frac{1}{R}$ and $Y_3 = Y_4 = sC$

$$\frac{V_o}{V_i} = H(s) = \frac{A_f \cdot \frac{1}{R^2}}{\frac{1}{R^2} + sC\left[\frac{1}{R} + \frac{1}{R} + sC\right] + \frac{sC}{R}[1 - A_f]}$$

$$= \frac{A_f \frac{1}{R^2}}{\frac{1}{R^2}\left[1 + sCR^2\left[\frac{2}{R} + sC\right] + sCR[1 - A_f]\right]}$$

$$= \frac{A_f}{1 + sCR^2\left[\frac{2}{R} + sC\right] + sCR(1 - A_f)}$$

$$= \frac{A_f}{1 + 2sCR + s^2C^2R^2 + sCR - sCRA_f}$$

$$= \frac{A_f}{1 + 3sCR + s^2C^2R^2 - sCRA_f}$$

$$H(s) = \frac{A_f}{s^2C^2R^2 + sCR[3 - A_f] + 1}$$

Transfer function H(s) of low pass filter [second order] can be obtained by dividing Nr & Dr by $1/R^2C^2$ then we get

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o/R^2C^2}{s^2 + \frac{s}{RC}[3 - A_f] + \frac{1}{R^2C^2}}$$

Comparing with equation [standard form of any second order system.

$$\boxed{H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_o \omega_h^2}{s^2 + \alpha \omega_h s + \omega_h^2}}$$

$\alpha = 3 - A_f$ & $\omega_h = 1/RC$

A_f - Gain [Non-Inverting]

ω_h - Upper cutoff freq. rad/sec

α - damping coefficient.

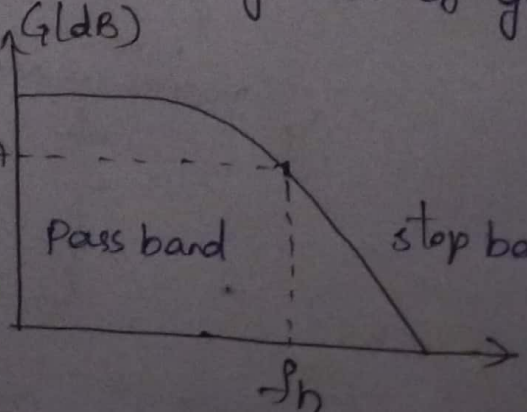
$\omega_h = \frac{1}{RC} \Rightarrow 2\pi f_h = \frac{1}{RC}$ (or) $\boxed{f_h = \frac{1}{2\pi RC}}$

Put $s = j\omega$ and $\alpha = 1.414$ the voltage gain magnitude of a second order low pass filter can be obtained as

$$|H(j\omega)| = \left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{1 + (f/f_h)^4}}$$

for nth order low pass filter the magnitude of gain

$$\left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{1 + (f/f_h)^{2n}}}$$



* Design steps :-

1. choose cut off freq.
2. The design can be simplified by selecting $R_1 = R_2 = R$ & $C_1 = C_2 = C$.
3. choose the value of $C \leq 1\mu f$.
4. calculate the value of R from the eqn. $f_h = \frac{1}{2\pi RC}$.
5. $A_0 = \left(1 + \frac{R_f}{R_1}\right)$; for $n=2$ the damping factor $\alpha = 1.414$; A The pass band gain $A_0 = 3 - \alpha = 3 - 1.414$

$A_0 = 1.586$.

$R_f = 0.586 R_1$.

$1.586 = 1 + \frac{R_f}{R_1}$

$\frac{R_f}{R_1} = 0.586$

* Design a 2nd order LPF having cutoff freq. of 1KHz Draw its freq. response.

Given $f_h = 1KHz$

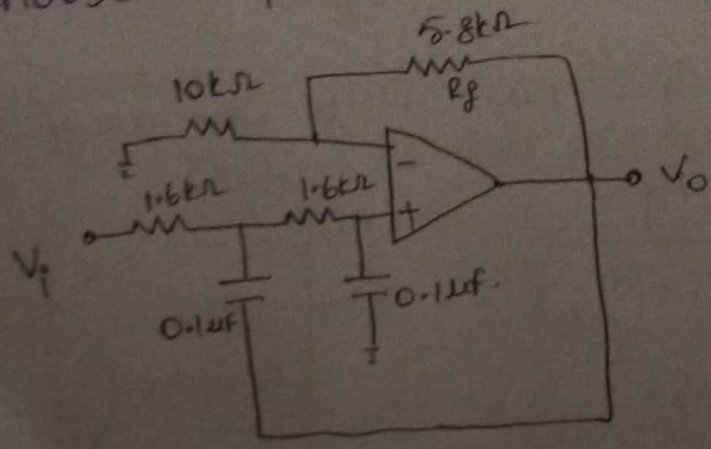
We know that $f_h = \frac{1}{2\pi RC}$

choose $C = 0.1\mu f$ then $R = \frac{1}{2\pi f_h C} \Rightarrow R = \frac{1}{2\pi \times 1 \times 10^3 \times 0.1 \times 10^{-6}}$

$R = 1.6k\Omega$

We know that $R_f = 0.586 R_1$

choose $R_1 = 10k\Omega$ then $R_f = 5.86k\Omega$



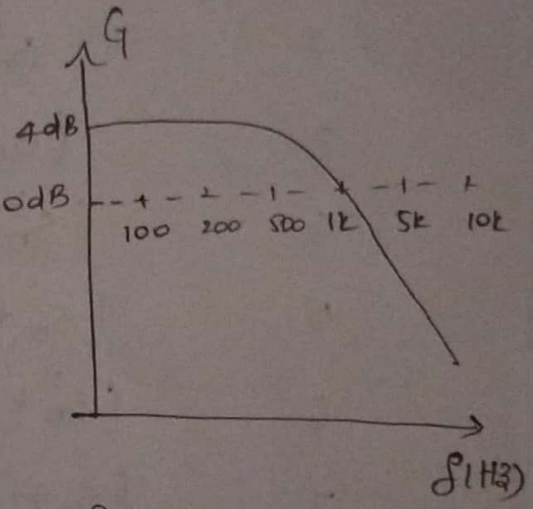
Frequency response

$$\left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{1+(f/f_h)^4}}$$

We know that $A_f = 1 + \frac{R_f}{R_1} = 1 + 0.586 = 1.586$

$$\left|\frac{V_o}{V_i}\right| = \frac{1.586}{\sqrt{1+\left(f/1KH_2\right)^4}}$$

f	$\frac{V_o}{V_i}$	$\left\|\frac{V_o}{V_i}\right\|$ dB
100	1.58	3.97
200	1.58	3.97
500	1.58	3.97
1k	1.54	3.95
5k	0.06	-24.4
10K	0.02	-33.9



freq. response.

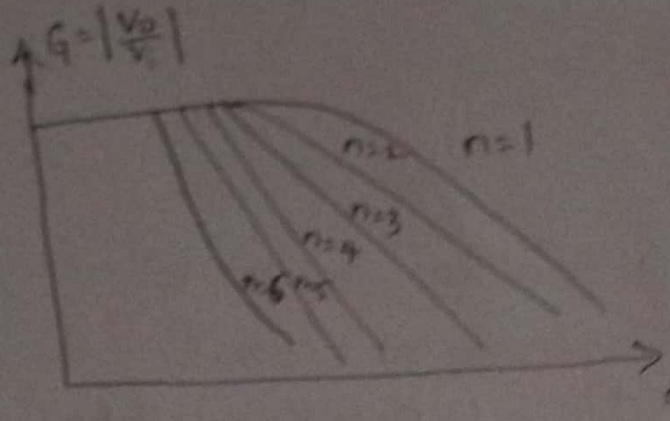
* Higher order low pass filter :-

. A second order filter produces -40dB/decade rolloff rate in stop band. The roll off increases with increase in the order of the filter.

* Each increase in order will produce -20dB/dec. additional increases the roll off rate. for nth order filter roll-off rate will be $-n \times 20$dB/decade.

Ex: 5th order.

$$H(s) = \underbrace{\frac{A_{01}}{s_n^2 + \alpha_1 s_n + 1}}_{2^{nd}\text{ order}} \cdot \underbrace{\frac{A_{02}}{s_n^2 + \alpha_2 s_n + 1}}_{2^{nd}\text{ order}} \cdot \underbrace{\frac{A_0}{s_n + 1}}_{1^{st}\text{ order}}$$



Roll off rate for different values of n.

* Butterworth Polynomials :-

order n	factors of polynomials
1.	S_n+1
2.	$S_n^2+1.414S_n+1$
3.	$(S_n+1)(S_n^2+S_n+1)$
4.	$[S_n^2+0.765S_n+1][S_n^2+1.848S_n+1]$
5.	$[S_n+1][S_n^2+0.618S_n+1][S_n^2+1.618S_n+1]$
6.	$[S_n^2+0.518S_n+1][S_n^2+1.414S_n+1][S_n^2+1.932S_n+1]$
7.	$[S_n+1][S_n^2+0.545S_n+1][S_n^2+1.247S_n+1][S_n^2+1.804S_n+1]$
8.	$[S_n^2+0.390S_n+1][S_n^2+1.11S_n+1][S_n^2+1.663S_n+1]$ $[S_n^2+1.962S_n+1]$.

Higher order filter can be built by using cascading number of first & second order filter.

* Design a fourth order Butterworth low pass filter having upper cut off frequency 1KHz. (10)

Sol The upper cut off frequency $f_h = 1KHz$.

$n = 4$

choose $C = 0.1\mu f$.

$$f_H = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi f_h C} \Rightarrow R = \frac{1}{2\times 3.14\times 1\times 10^3\times 0.1\times 10^{-6}}$$

$R = 1.6k\Omega$

Here we get damping factors $\alpha_1 = 0.765$ & $\alpha_2 = 1.848$.

The pass band gain of two quadratic factors are

$$A_{o_1} = 3-\alpha_1 = 3-0.765 = 2.236$$

$$A_{o_2} = 3-\alpha_2 = 3-1.848 = 1.152.$$

The transfer function of fourth order low pass Butterworth filter is

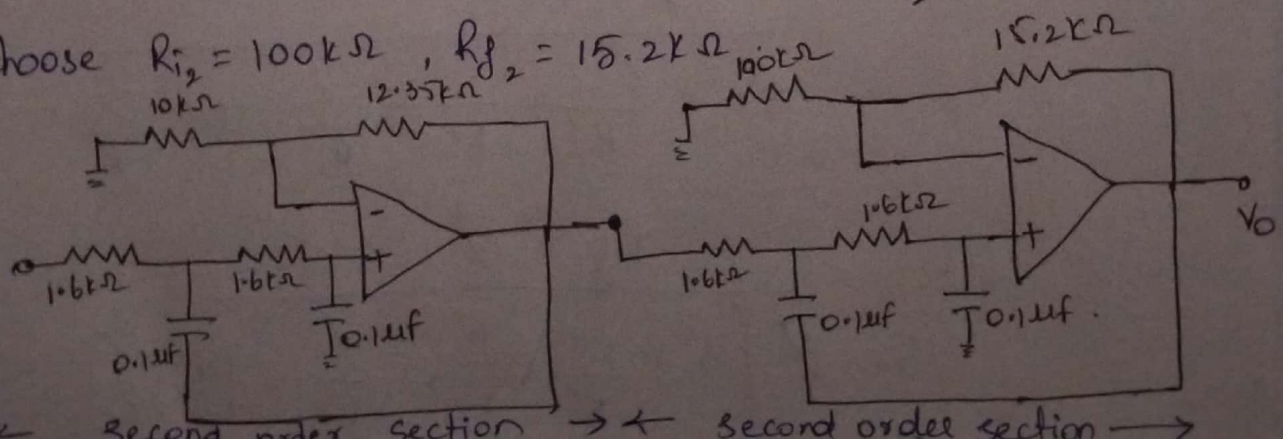
$$\frac{2.235}{S_n^2+0.765S+1} \cdot \frac{1.152}{S_n^2+1.848S_n+1}$$

Now $A_{o_1} = 1+\frac{R_{f_1}}{R_{i_1}} \Rightarrow 2.235 = 1+\frac{R_{f_1}}{R_{i_1}} \Rightarrow \frac{R_{f_1}}{R_{i_1}} = 1.235$.

let $R_{f_1} = 12.35k\Omega$ & $R_{i_1} = 10k\Omega$. then we get $A_{o_1} = 2.235$

$$A_{o_2} = 1+\frac{R_{f_2}}{R_{i_2}} \Rightarrow 1.152 = 1+\frac{R_{f_2}}{R_{i_2}} \Rightarrow \frac{R_{f_2}}{R_{i_2}} = 0.152$$

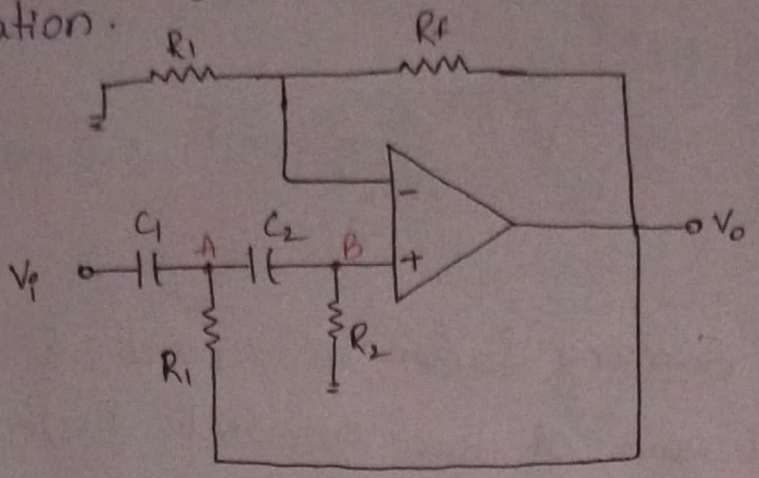
choose $R_{i_2} = 100k\Omega$, $R_{f_2} = 15.2k\Omega$



~~* High pass~~

* Second order High pass Butterworth filter :-

* High pass filter is the complement of the low pass filter. It is formed by interchanging R and C in the low pass configuration.



General expression for second order filter

$$\frac{V_o}{V_i} = \frac{A_f Y_1 Y_2}{Y_1 Y_2 + Y_4(Y_1 + Y_2 + Y_3) + Y_2 Y_3 [1 - A_f]}$$

for Hpf put $Y_1 = Y_2 = sC$ & $Y_3 = Y_4 = \frac{1}{R}$.

$$H(s) = \frac{V_o}{V_i} = \frac{A_f s^2 C^2}{s^2 C^2 + \frac{1}{R}\left[sC + sC + \frac{1}{R}\right] + \frac{sC}{R}[1 - A_f]}$$

$$= \frac{A_f s^2 C^2}{s^2 C^2 + \frac{1}{R}\left[2sC + \frac{1}{R}\right] + \frac{sC}{R}[1 - A_f]}$$

$$= \frac{A_f s^2 C^2}{s^2 C^2 + \frac{2sC}{R} + \frac{1}{R^2} + \frac{sC}{R} - A_f \cdot \frac{sC}{R}}$$

$$= \frac{A_f s^2 C^2}{C^2\left[s^2 + \frac{2s}{RC} + \frac{1}{R^2 C^2} + \frac{s}{RC} - A_f \frac{s}{RC}\right]}$$

$$= \frac{A_f s^2}{s^2 + \frac{3s}{RC} + \frac{1}{R^2C^2} - A_f \frac{s}{RC}}$$

$$H(s) = \frac{A_f s^2}{s^2 + \frac{s}{RC}[3 - A_f] + \frac{1}{R^2C^2}}$$

Comparing with the standard eqn of second order system transfer function

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A_f s^2}{s^2 + \alpha \omega_l s + \omega_l^2}$$

$$\omega_l = \frac{1}{RC} \quad ; \quad \alpha = 3 - A_f \quad ; \quad \omega_l^2 = \frac{1}{R^2C^2}$$

$$2\pi f_l = \frac{1}{RC} \Rightarrow f_l = \frac{1}{2\pi RC}$$

$$\therefore H(s) = \frac{A_f s^2}{s^2 + (3 - A_f)\omega_l s + \omega_l^2}$$

Put $s = j\omega$ & $(3 - A_f) = \alpha = 1.414$ the voltage gain magnitude of second order Hpf given by

$$H(j\omega) = \left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{1 + (f_l/f)^4}}$$

Generalized expression for n^{th} order Hpf.

$$|H(j\omega)| = \frac{A_f}{\sqrt{1 + (f_l/f)^{2n}}}$$

*Design a HPF with cutoff freq. of 10kHz with a pass band gain of 1.5. Also plot the frequency response for the designed filter.

let $C = 0.02\,\mu f$ [$< 1\mu f$]

lower cut off freq. $f_1 = 10kHz$.

$$f_1 = \frac{1}{2\pi RC}$$

$$R = \frac{1}{2\pi f_1 C} \Rightarrow R = \frac{1}{2\times 3.14\times 10\times 10^3\times 0.02\times 10^{-6}}$$

$R = 795.77\,\Omega$ $\quad R \simeq 1k\Omega$

Gain $A_f = 1.5$

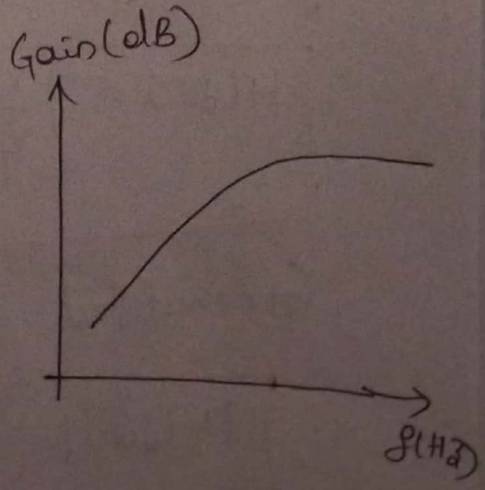
$$A_f = 1 + \frac{R_f}{R_1} \Rightarrow 1.5 = 1 + \frac{R_f}{R_1} \Rightarrow 0.5R_1 = R_f$$

Select $R_1 = 10k\Omega$ $\quad R_f = 5k\Omega$.

To obtain frequency response consider the magnitude of transfer function of filter given by

$$\left|\frac{V_o}{V_i}\right| = \frac{A_f}{\sqrt{1+(f_1/f)^2}} = \frac{1.5}{\sqrt{1+\left(\frac{10k}{f}\right)^2}}$$

f	$\frac{V_o}{V_i}$	$\left(\frac{V_o}{V_i}\right)_{dB} = 20\log\left\|\frac{V_o}{V_i}\right\|$
100	0.0149	-36.5
200	0.029	-30.75
500	0.074	-22.61
1k	0.149	-16.53
5k	0.670	-3.47
10k	1.060	0.506
12k	1.060	0.506.



-12dB.

*Determine the order of LPf i.e to provide 40dB attenuation at $\frac{\omega}{\omega_h} = 2$ (12)

Given $\frac{\omega}{\omega_h} = 2$

Transfer function of n^{th} order butterworth LPf given by

$$|H(j\omega)| = \frac{A_0}{\sqrt{1+\left(\frac{\omega}{\omega_h}\right)^{2n}}}$$

$$\left|\frac{H(j\omega)}{A_0}\right| = \frac{1}{\sqrt{1+(\omega/\omega_h)^{2n}}}$$

Given $20\log\left|\frac{H(j\omega)}{A_0}\right| = -40$ dB.

$$\frac{H(j\omega)}{A_0} = 10^{-2} = 0.01 \Rightarrow 0.01 = \frac{1}{\sqrt{1+(\omega/\omega_h)^{2n}}}$$

$$\frac{1}{[1+(2)^{2n}]} = (0.01)^2 \Rightarrow 1+(2)^{2n} = \frac{1}{(0.01)^2}$$

$$2^{2n} = 10^4 - 1 = 9999 \Rightarrow 2n\log 2 = \log 9999$$

$$n \simeq 6.64$$

$\therefore$ order of the filter $n = 7$.

*Band pass filter [BPf].

A band pass filter has a pass band between low cut off frequencies f_H and f_L such that $f_H > f_L$ any i/p frequency outside of this passband is attenuated.

*Two types of band pass filters are there which are classified based on the figure of merit (or) Quality factor (Q_f).

(i) for $Q \leq 10$ the BPf is called wide band pass filter In this type the band pass is wide and we get large BW.

(ii) for $Q > 10$ the band pass filter called narrow band pass filter. The band pass is very narrow and the BW is very small.

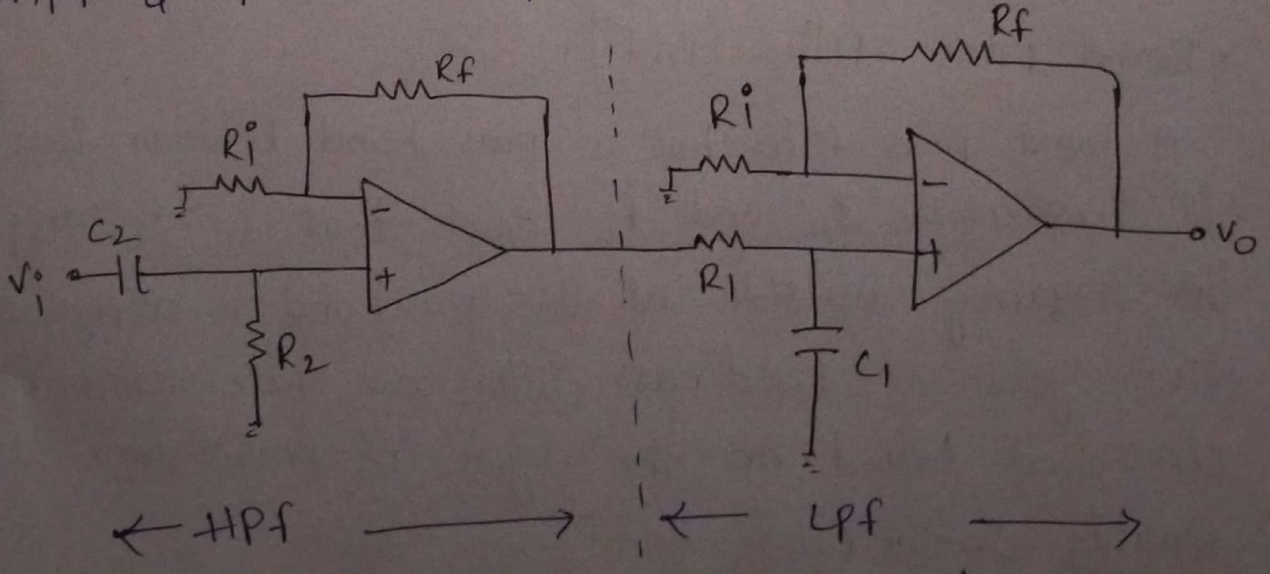
'Q' is a measure of selectivity the higher the value of Q, the more selectivity is the filter (or) narrow its B.W.

*The relationship b/w Q & BW, the center frequency f_c is given by $Q = \frac{f_c}{BW} \Rightarrow$ $\boxed{Q = \frac{f_c}{f_H - f_L}}$

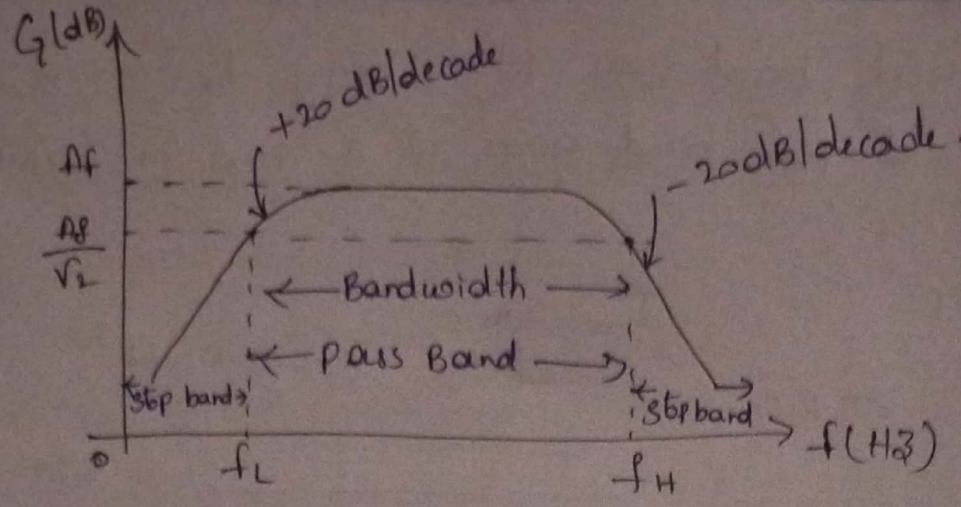
*Wide Band pass filter:-

A wide band pass filter can be formed by simply cascading high-pass & low-pass section. If HPf & LPf are of first order then the band pass filter (BPf) is of first order with roll off ±20dB/decade.

*In HPf & LPf are of second order the BPf is of second order. The order of BPf depends on order of HPf & LPf. for BPf response, $f_H >> f_L$.



first order Band pass filter.



frequency response.

*for wide band response, f_H must be greater than f_L, the voltage gain expression for the two sections are given by

$$\left|\frac{V_o}{V_i}\right| = \frac{Af}{\sqrt{1+(f/f_h)^2}} \quad [LPf]$$

$$\left|\frac{V_o}{V_i}\right| = \frac{Af\,(f/f_L)}{\sqrt{1+(f/f_L)^2}} \quad [HPf]$$

The overall gain wide band pass filter is the product of two gains $Af_T = A_1 \cdot A_2$

$$\left|\frac{V_o}{V_i}\right| = \frac{Af_T\,[f/f_L]}{\sqrt{\left[1+(f/f_L)^2\right]\left[1+f/f_H\right]^2}}$$

Af_T = Total pass band gain $Af_1 \times Af_2$

f = input frequency

f_L = lower cut off freq.

f_H = Higher cutoff freq.

Design a wide band pass filter having $f_L = 400Hz$ & $f_h = 2KHz$ and pass band gain of 4. find the value of Q of the filter.

for LPF

$$f_h = \frac{1}{2\pi R_1 C_1} \qquad \text{choose } C_1 = 0.01\mu f$$

$$R_1 = \frac{1}{2\pi f_h C_1} = \frac{1}{2\times 3.14\times 2\times 10^3\times 0.01\times 10^{-6}} = 7.9k\Omega$$

for HPF

$$f_L = \frac{1}{2\pi R_2 C_2} \qquad \text{choose } C_2 = 0.01\mu f$$

$$R_2 = \frac{1}{2\pi f_L C_2} = \frac{1}{2\times 3.14\times 400\times 0.01\times 10^{-6}} = 39.8k\Omega$$

Pass band gain $A_{f_T} = 4$, $A_{f_1} = 2$ $A_{f_2} = 2$

$$A_{f_1} = A_{f_2} = 1 + \frac{R_f}{R_i} = 2$$

$$R_f = R_i$$

Let $R_i = 10k\Omega$, $R_f = 10k\Omega$ for both LPF & HPF

$$Q = \frac{f_o}{BW}$$

$$f_o = \sqrt{f_H f_L} = \sqrt{2000\times 400} = 894.4$$

$$BW = f_H - f_L = 2000 - 400 = 1600$$

$$Q = \frac{894.4}{1600} = 0.56$$

obviously for wide band pass filter, Q is very low i.e $Q < 10$.

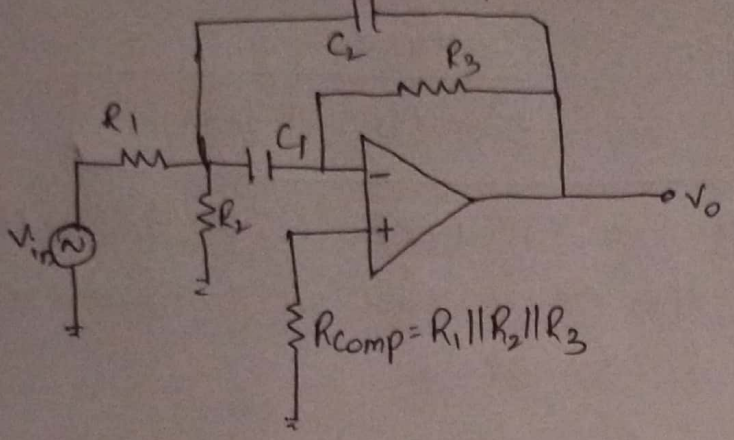
* Narrow Band pass filter :-

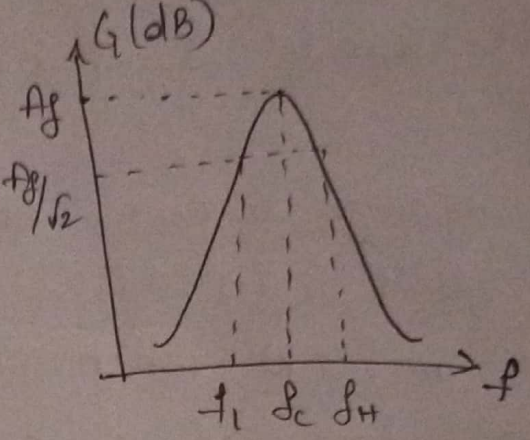
* The narrow BPf uses only one op-Amp unlike two used by wide band pass filter.

(i) It has two feedback paths.

(ii) Op-Amp is in inverting configuration.

* Due to feedback path it is called multiple feedback filter.





* The input applied to the inverting input terminal. Thus op-Amp used in inverting configuration. Important parameters are f_H, f_L, f_c & Q.

Designing steps

Choose $C_1 = C_2 = C$

$$R_1 = \frac{Q}{2\pi f_c C A_f}$$

$$R_2 = \frac{Q}{2\pi f_c C [2Q^2 - A_f]}$$

$$R_3 = \frac{Q}{\pi f_c C}$$

$$A_f = \frac{R_3}{2R_1}$$

for Narrow BPf $A_f < 2Q^2$ the gain must satisfies the Eqn.

* An important advantage of multiple feedback filter is changing the center frequency.

* The new center frequency can be achieved by changing the resistance R_2 without changing B.W & gain.

$$R_2' = R_2\left[\frac{f_c}{f_c'}\right]^2$$

Transfer function is $H(s) = \dfrac{-A_0 \alpha \omega_0 s}{s^2 + \alpha \omega_0 s + \omega_0^2}$

* Design a narrow BPF with two f/b paths with $f_c = 1.5\,kHz$, $Q = 7$ & $A_f = 15$ calculate the new value of resistance in the ckt which change f_c to 2kHz.

choose $C_1 = C_2 = C = 0.02\,\mu f$

$$R_1 = \frac{Q}{2\pi f_c C A_f} = \frac{7}{2\times 3.14 \times 1.5\times 10^3 \times 0.02\times 10^{-6}\times 15}$$

$$R = 2.47\,k\Omega$$

$$R_2 = \frac{Q}{2\pi f_c C[2Q^2 - A_f]} = \frac{7}{2\times 3.14\times 1.5\times 10^3 \times 0.02\times 10^{-6}[2\times 49 - 15]}$$

$$R_2 = 477.4\,\Omega$$

$$R_3 = \frac{Q}{\pi f_c C} = \frac{7}{3.14\times 1.5\times 10^3 \times 0.02\times 10^{-6}} \Rightarrow R_3 = 7$$

$$R_3 = 74.27\,k\Omega$$

Resistance R_2 changed to get $f_c' = 2\,kHz$

$$R_2' = R_2\left[\frac{f_c}{f_c'}\right]^2$$

$$= 447.4 \times \left[\frac{1.5}{2}\right]^2 = 251.6\,\Omega$$

* Band Reject filter :-

The band Reject filter is also called as Band stop (or) Band elimination. In this filter frequencies are attenuated in stop band and passed outside this band.

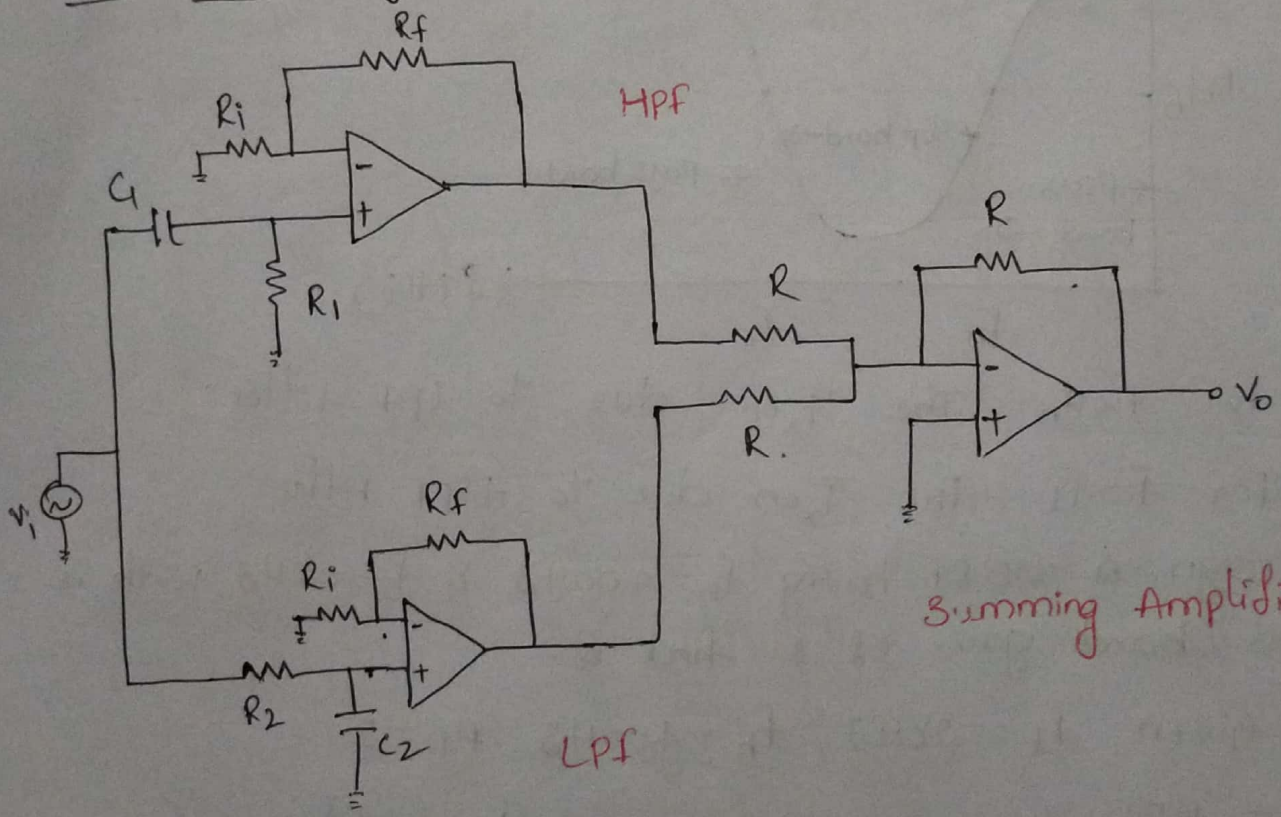
* They are classified into two types:

(i) Narrow Band Reject filter.

(ii) Wide Band Reject filter.

* Narrow band Reject filter is commonly called as Notch filter. and is useful for the rejection of a single frequency such as 50Hz power line frequency hum.

Wide Band Reject filter :-



Wide BRf.

* Wide band stop filter consists of LPf, HPf and summing amplifier. The LPf, HPf are excited by common input V_i.

* The output of LPf & HPf are given as i/p to inverting summing Amplifier.

*To obtain the better performance the wide band stop filter follows two conditions

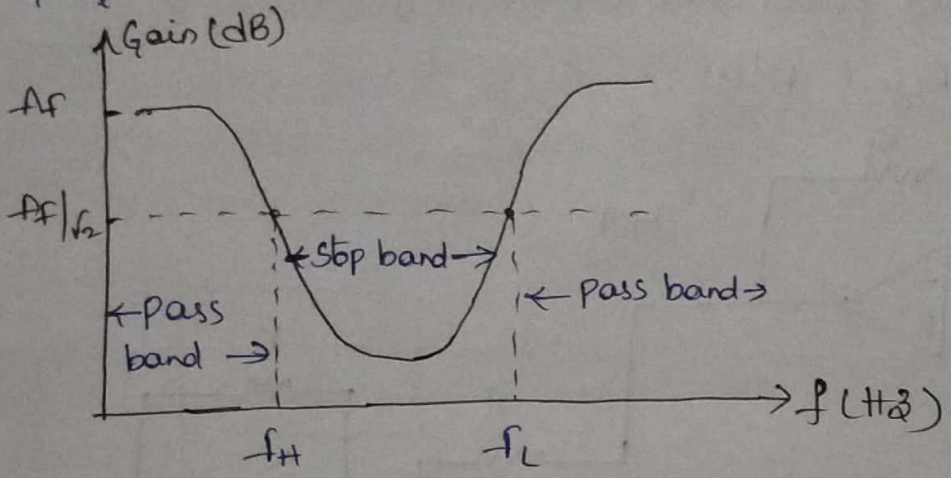
i. The low cut off frequency f_L of high pass filter must be greater than high cut off frequency f_h of LPF

$$f_L >> f_H.$$

ii. The pass band gain of both LPF & HPF must be equal

• for simplicity the gain of summing amplifier is said to be the freq. of wide band stop filter is shown in fig.

*Both LPF & HPF provided attenuation in stop band blw f_h & f_L.



for $f < f_h$, The $T_x$on due to LPF filter.

for $f > f_L$ the $T_x$on due to HPF filter.

*Design a WBRf having $f_h = 400Hz$ & $f_L = 2KHz$ with a pass band gain of 2 find Q.

Given $f_L = 2KHz$, $f_h = 400Hz$, $Af = 2$

for HPF

$$f_L = \frac{1}{2\pi R_1 C_1}$$

choose $C_1 = 0.1\mu f$

$$R_1 = \frac{1}{2\pi f_L C_1} = \frac{1}{2\pi \times 2\times10^3 \times 0.1\times10^{-6}}$$

$$R_1 = 796\,\Omega$$

for LPF.

$f_h = 400Hz$

choose $C_2 = 0.1\mu f$

$$R_2 = \frac{1}{2\pi f_h C_2} = \frac{1}{2\pi \times 400 \times 0.1\times10^{-6}}$$

$$R_2 = 4K\Omega.$$

$A_f = A_{f_1} * A_{f_2} = 2$

$\therefore A_f = 1 + \frac{R_f}{R_i} \Rightarrow 2 = 1 + \frac{R_f}{R_i} \Rightarrow R_f = R_i$

Let $R_i = 10k\Omega$ then $R_f = 10k\Omega$.

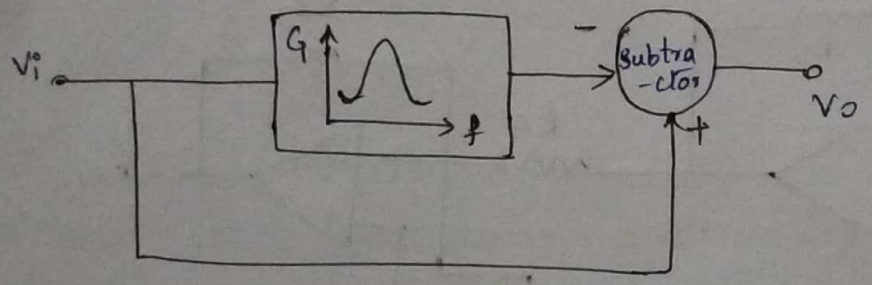
Gain of inverting summing amplifier = 1.

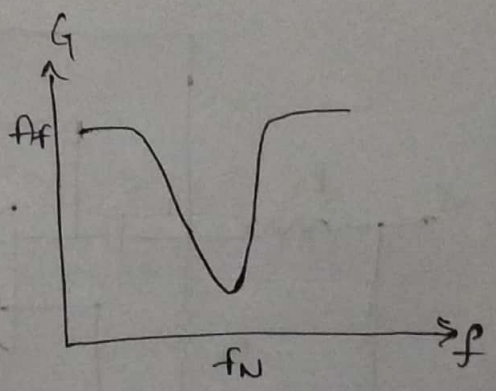
all resistors are equal.

* Narrow Band Reject filter [Notch filter] :-

Narrow BRf is used for rejection of single frequency such as 50Hz power line frequency hum (noise). It is also used in biomedical instrumentation and blanking of control line.

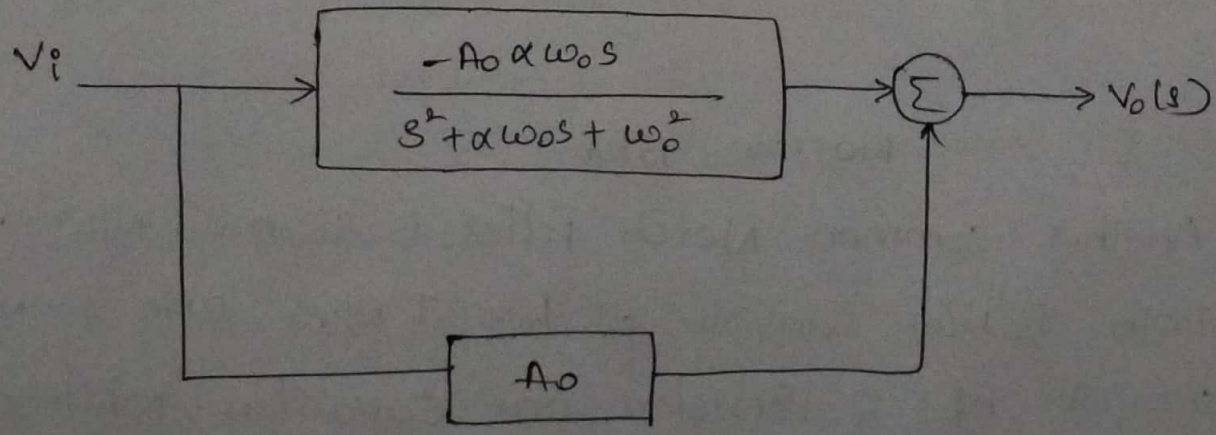
*The best way to design a notch filter is to subtract band pass filter o/p from its i/p. The stop band of this filter is very narrow.



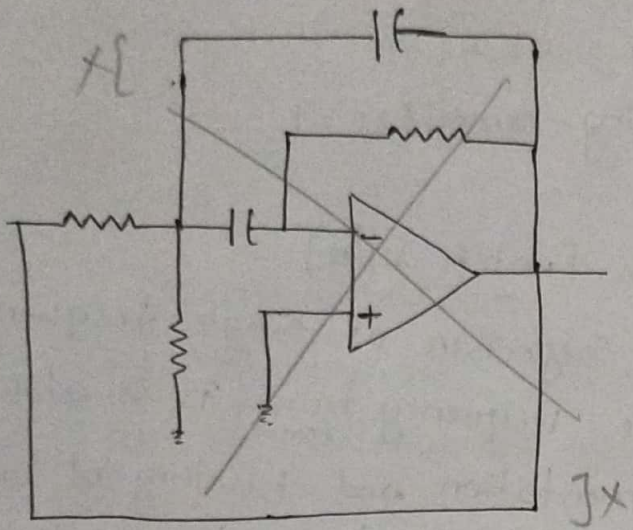


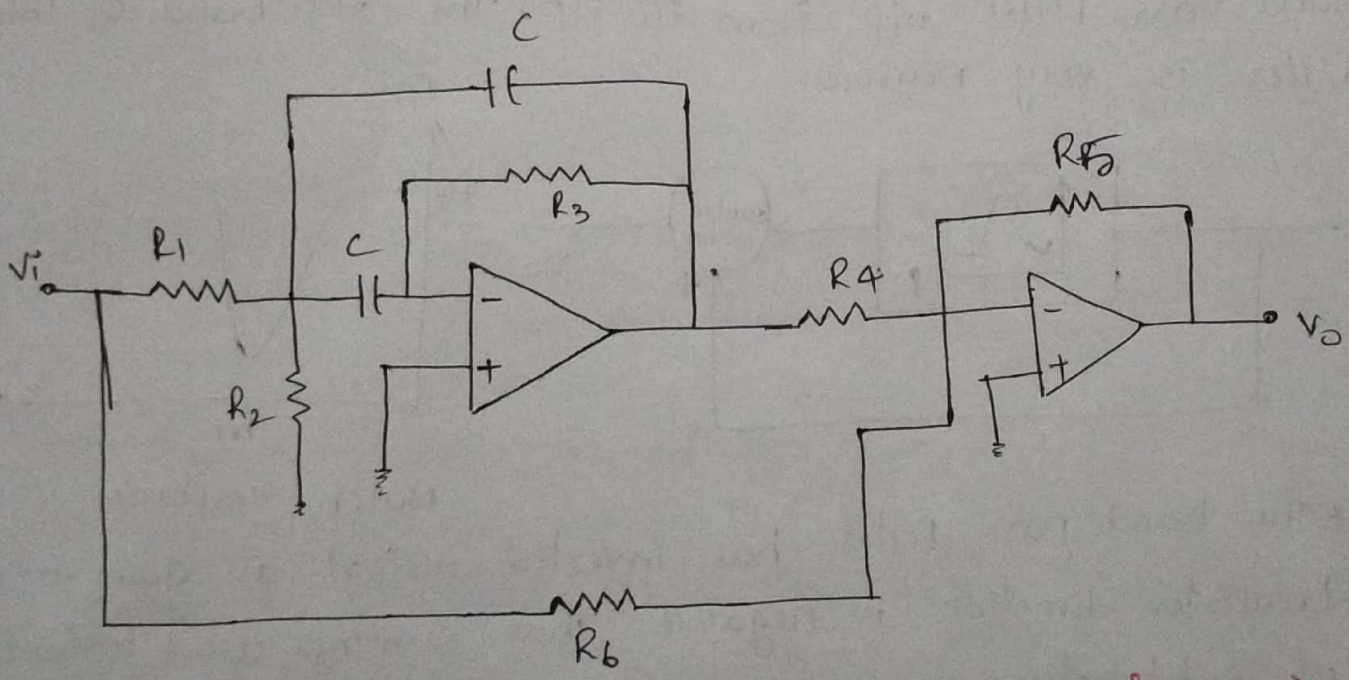
Notch response

*The band pass filter has inverted output as gain or transfer function is negative. Thus summer used instead of subtractor.



*This is transfer function of second order notch filter for $\omega << \omega_0$ & $\omega >> \omega_0$ gain of pass band is A_0 and at $\omega = \omega_0$ gain is Zero.

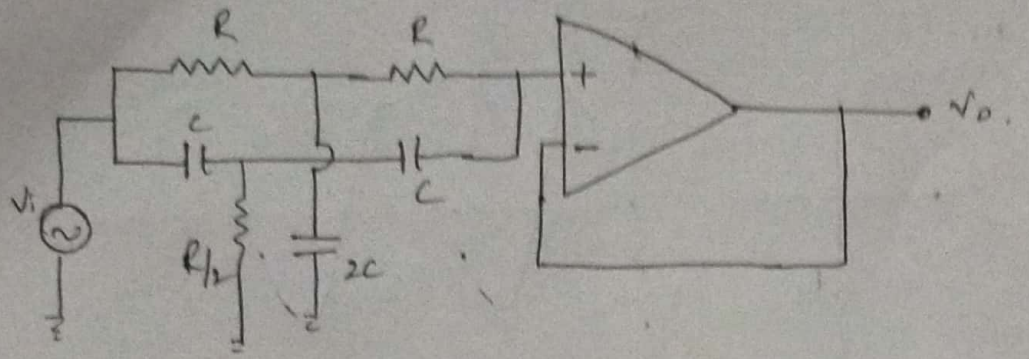




← BPf ——————→ ← Summer →

Narrow BRf.

Another common Notch filter is Twin-T N/w. The twin T-N/w consists of two T N/w's. One T-N/w consists of 2 Resistors one Capacitors. while other T-N/w consists of 2 capacitors and one Resistors.



Twin - T network.

By using this we can determine the f_N, BW. The frequency at which max. attenuation occurs is called Notch frequency.

$$f_N = \frac{1}{2\pi RC}$$

$$Q = \frac{f_o}{BW}$$

$$Q = \frac{1}{2(2-A_f)} \quad \text{w.r.to gain}$$

*All pass filter :-

All pass filter passes all frequency components of i/p signal without any attenuation and provides desired phase shift at different frequencies of i/p signal.

* When signals are transmitted over the transmission lines such as telephone wires, they undergo change in phase.

* Thus phase changes can be compensated by all pass filter thus all pass fillers are also called delay equalizers (or) phase correctors Assume $R_f = R_1$

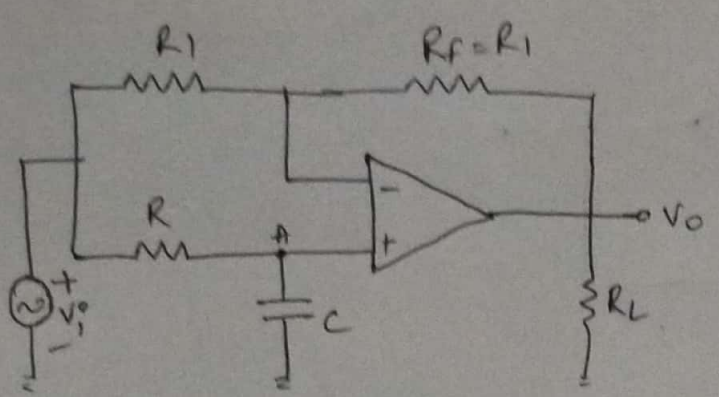
* The o/p voltage V_o of filter can be obtained by using super position theorem

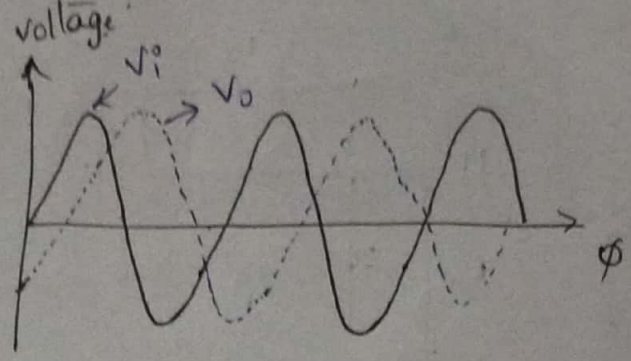
$$V_o = -\frac{R_f}{R_1} V_i + \left[1 + \frac{R_f}{R_1}\right] V_a$$

Where V_a is voltage at node A.

$$R_f = R_1$$

$$V_o = -V_i + 2V_a \quad \text{— (1)}$$





$$V_a = \frac{X_c}{R+X_c} V_i$$

Sub. value of V_a in eqn (1), we get

$$V_o = -V_i + 2\left[\frac{X_c}{R+X_c}\right] V_i$$

$$V_o = -V_i + \left[2\,\frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}\right] V_i$$

$$V_o = -V_i + \frac{2V_i}{1+j\omega RC} \Rightarrow V_o = +V_i\left[-1 + \frac{2}{1+j\omega RC}\right]$$

$$\frac{V_o}{V_i} = \left[\frac{-1-j\omega RC+2}{1+j\omega RC}\right] \Rightarrow \frac{V_o}{V_i} = \left[\frac{1-j2\pi fRC}{1+j2\pi fRC}\right]$$

Magnitude of voltage gain given by

$$|A| = \left|\frac{V_o}{V_i}\right| = \frac{\sqrt{1+(2\pi fRC)^2}}{\sqrt{1+(2\pi fRC)^2}} = 1$$

Thus $|V_o| = |V_i|$ throughout the freq. range. The phase shift ϕ can be varies with freq.

$$\phi = -\tan^{-1}(2\pi fRC) - \tan^{-1}(2\pi fRC) \Rightarrow \boxed{\phi = -2\tan^{-1}[2\pi fRC]}$$

for given R & C and can be varied from 0° to -180°

frequency varies from 0 to ∞.

As phase shift is -ve, o/p V_o lags V_i

ϕ can be made +ve by interchanging R and C.

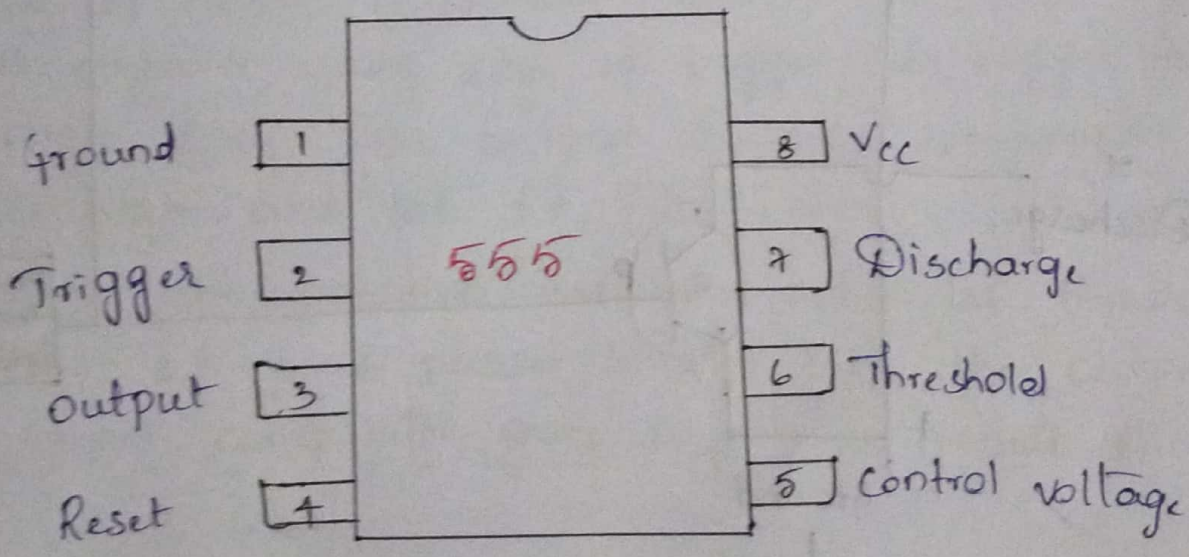
555 TIMER

* The 555 timer is highly stable device for generating accurate time delay or oscillations.

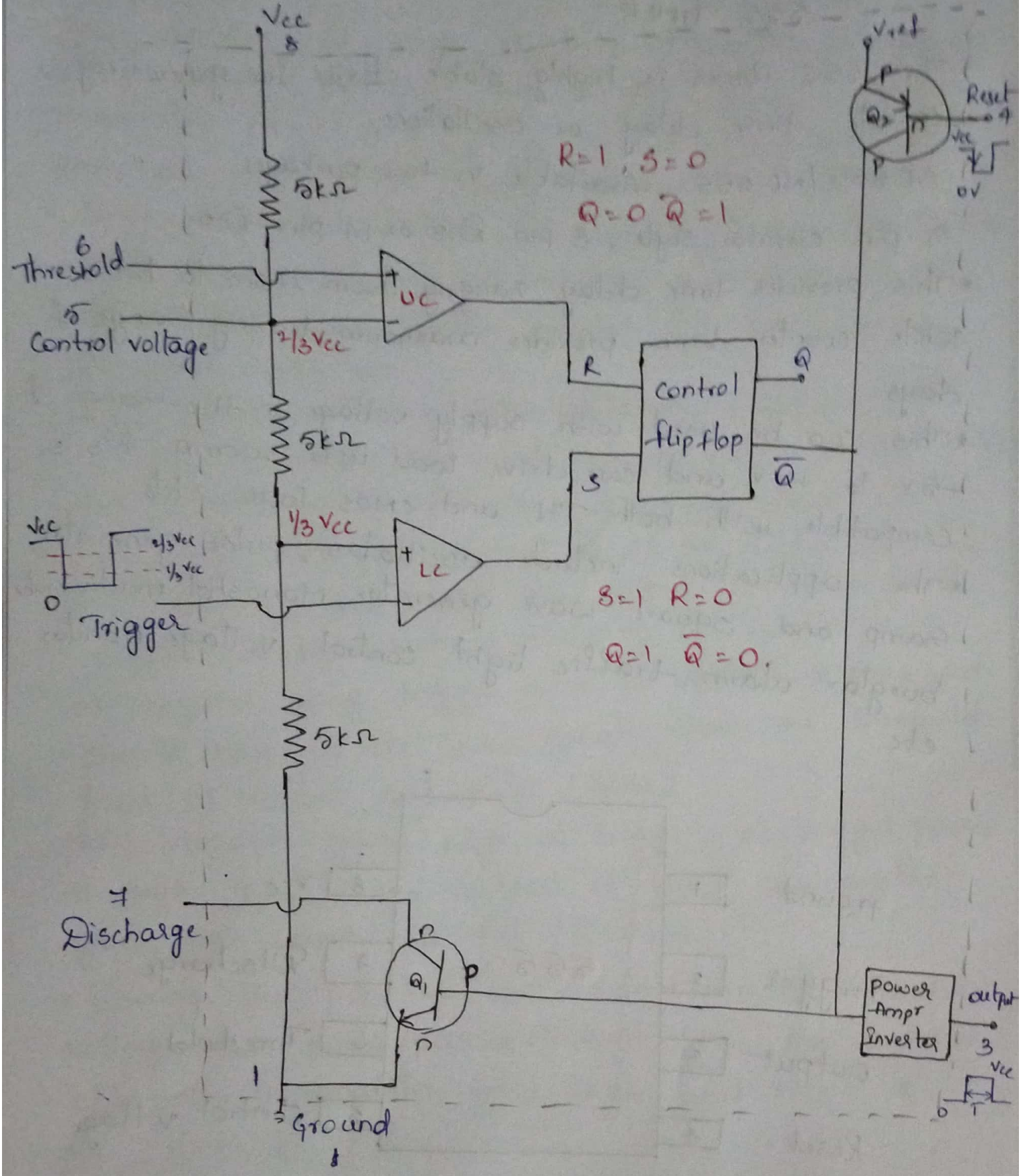
SE 555 / NE 555 - Available in two packages.

8 pin circular style, 8 pin DIP or 14 pin DIP.

* This provides time delay ranging from μsec to hours while counter timer, provides maximum timing range of days.
* This can be used with supply voltage in the range of +5V to +18V, and can drive load upto 200mA. This is compatible with both TTL and CMOS logic ckts.
* The applications include oscillators, pulse generator, ramp and square wave generator, Monoshot multivibrator burglar alarm, traffic light control, voltage monitor etc.



Pin diagram.



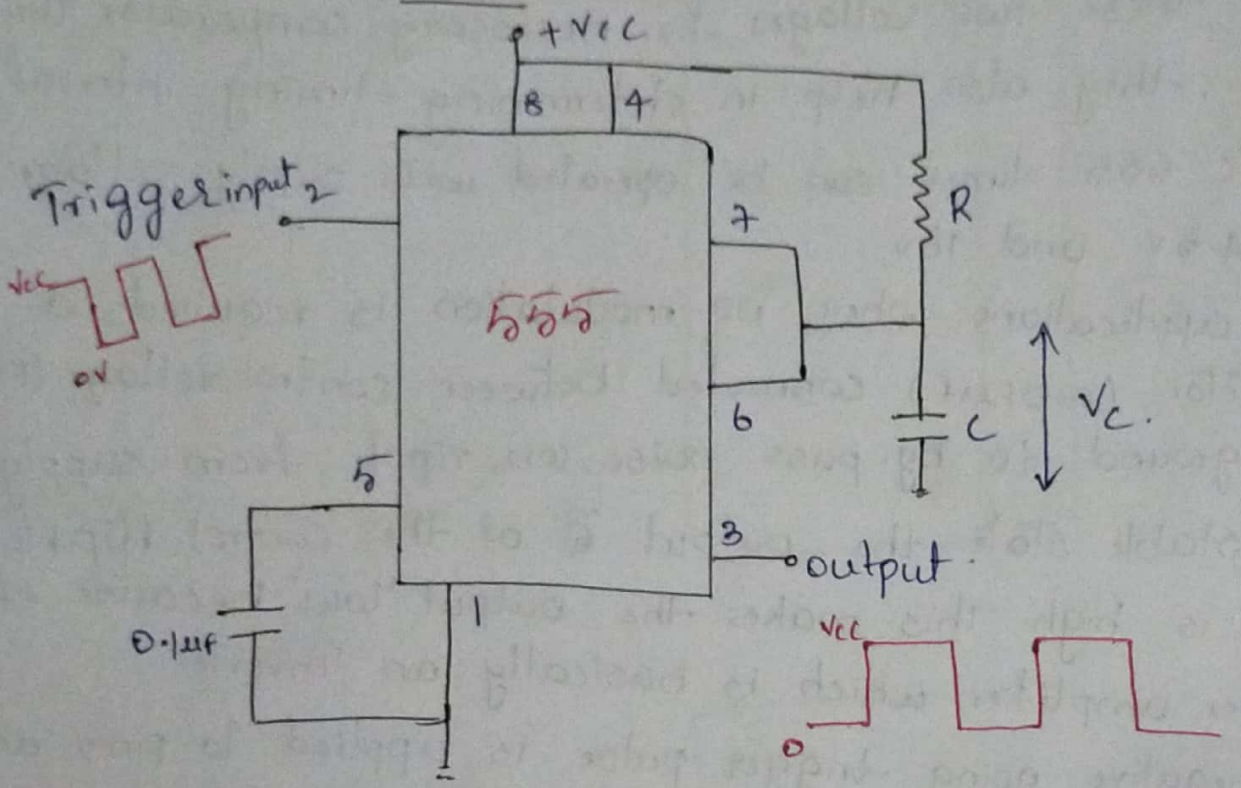
functional diagram.

Description :-

* Three resistors of 5kΩ of internal resistors acts as a voltage divider, providing bias voltage $(\frac{2}{3})V_{cc}$ to upper comparator (UC) and $(\frac{1}{3})V_{cc}$ to lower comparator [LC] where as V_{cc} is the supply voltage.
* Since these two voltages fix necessary comparator threshold voltage, they also help in determining timing interval.
* The IC 555 timer can be operated with supply voltage blw 4.5V and 16V.
* In applications where no modulation is required, a capacitor (0.01μf) connected between control voltage (pin 5) and ground to by-pass noise (or) ripple from supply.
* In stable state, the output $\bar{Q}$ of the control flipflop (ff) is high. This makes the output 'low' because of power amplifier which is basically an Inverter.
* A negative going trigger pulse is applied to pin 2 and should have its dc level greater than the threshold level of lower comparator ($\frac{1}{3}V_{cc}$).
* At negative going edge of trigger, as trigger passes through $\frac{1}{3}V_{cc}$, the output of lower comparator goes high and sets ff [$\bar{Q}=0, Q=1$]
* During the positive excursion when the threshold voltage at pin 6 passes through $\frac{2}{3}V_{cc}$ the output of upper comparator goes High and resets the ff [$Q=0, \bar{Q}=1$]
* The reset input (pin 4) resets ff overriding the effect of any instruction coming to ff from lower comparator.

* The transistor Q_2 serves as buffer to isolate the reset input from ff and the transistor Q_1. Also Q_1 is driven by an Internal reference voltage V_{ref} obtained from supply voltage V_{cc}.

* Monostable Operation :-

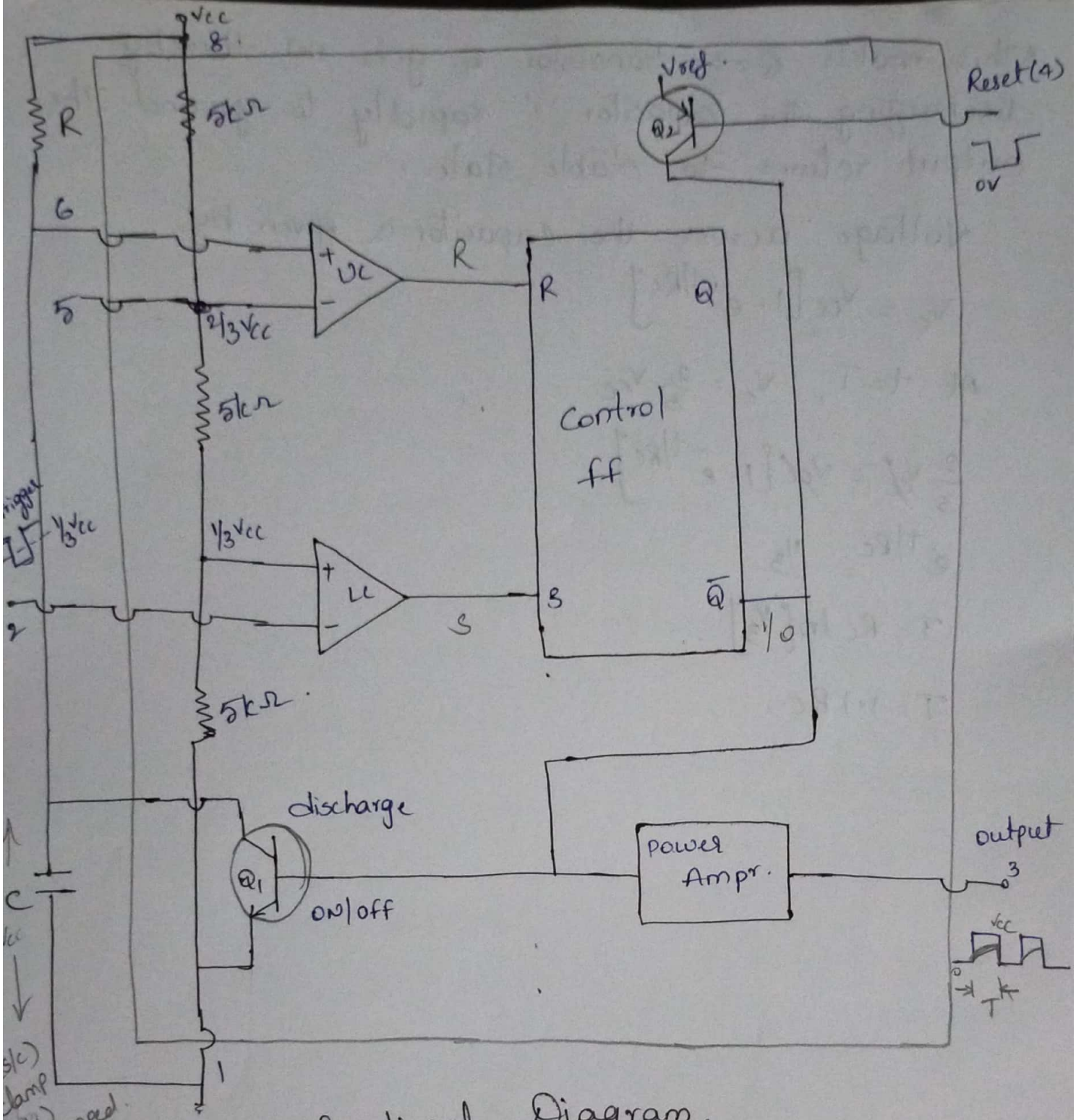


Monostable Multivibrator.

Operation :-

. In stable state, ff holds transistors ON (Q_1) thus clamping the external timing capacitor 'c' to ground. The output remains at ground (low).

* As trigger passes through $\frac{1}{3}V_{cc}$, ff is set i.e $S=1, R=0 \Rightarrow \bar{Q}=0$ [$Q=1$] This makes the transistor Q_1 off ord short circuit across timing capacitor c is released.



functional Diagram.

*As $\bar{Q}$ is low, output goes high (V_{cc}). The timing cycle now begins. Since 'c' is unclamped, voltage across it rises exponentially through R towards V_{cc} with time constant Rc.

*After time period 'T' the capacitor voltage is just greater than $\frac{2}{3}V_{cc}$ and upper comparator resets the ff. R=1, S=0; $\bar{Q}$ = 1 [Q=0]

*This makes $\bar{Q} = 1$ transistor Q_1 goes ON thereby discharging the capacitor 'c' rapidly to ground. The output returns to stable state.

Voltage across the capacitor is given by.

$$V_c = V_{cc}\left[1 - e^{-t/Rc}\right]$$

At $t = T$, $V_c = \frac{2}{3} V_{cc}$

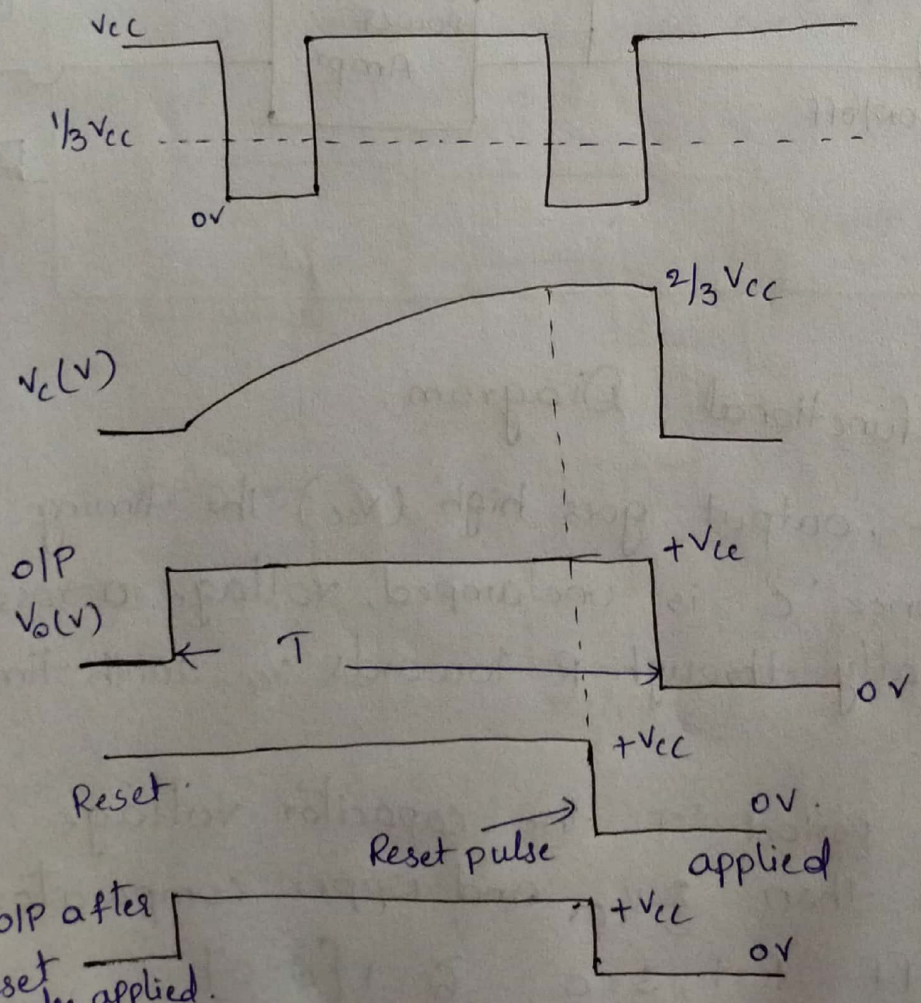
$$\frac{2}{3} V_{cc} = V_{cc}\left[1 - e^{-t/Rc}\right]$$

$$e^{-T/Rc} = 1/3$$

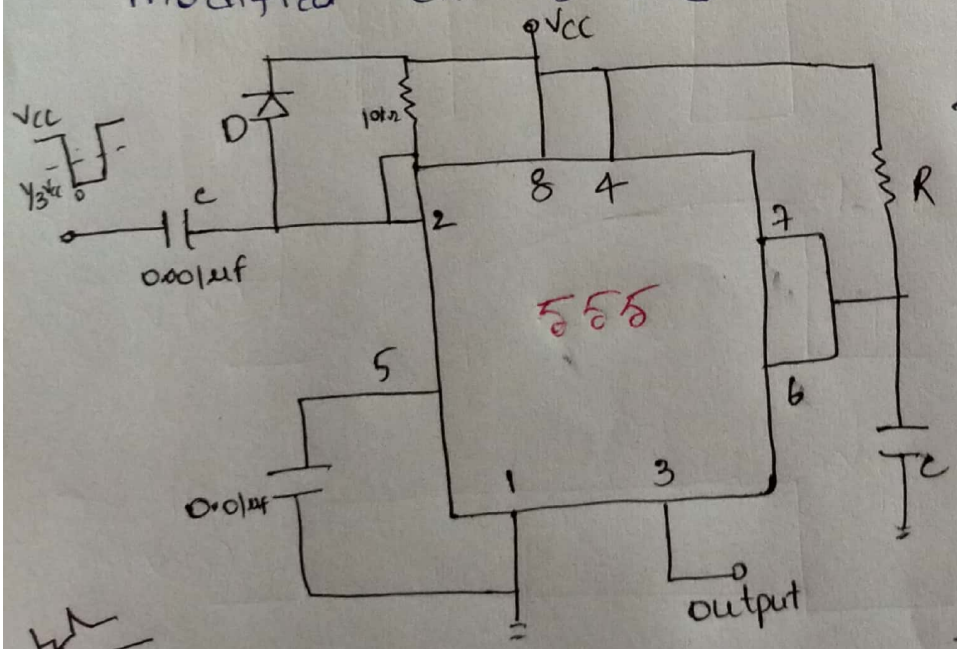
$$T = Rc \ln[1/3]$$

$$T = 1.1\, Rc.$$

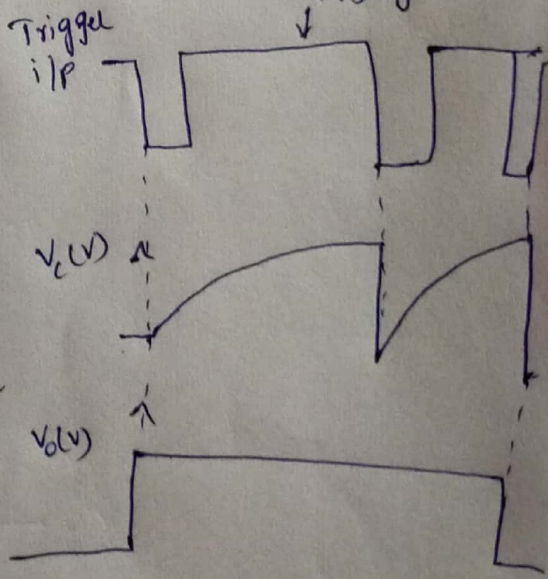
Timing pulse :-

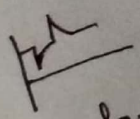


* The timing interval is independent of the supply voltage once triggered the output remains in High state until time T elapses which depends on value of R and C.
* Any additional trigger pulse coming during this time will not change the output state. If a negative going reset pulse is applied to reset terminal (pin 4) during timing cycle transistor Q_2 goes off, Q_1 turns ON and external timing capacitor C is immediately discharged
* The output Q_2 is connected directly to input of Q_1 so as to turn ON Q_1 immediately and thereby avoid propagational delay through the ff.
* Even if the reset ip is released, output will still remain low until negative going trigger pulse is again applied to pin 2.
* Monostable ckt mis-triggers on positive edge pulses, even with control pin bypass capacitor. To prevent this modified ckt is used.



Missing pulse detector



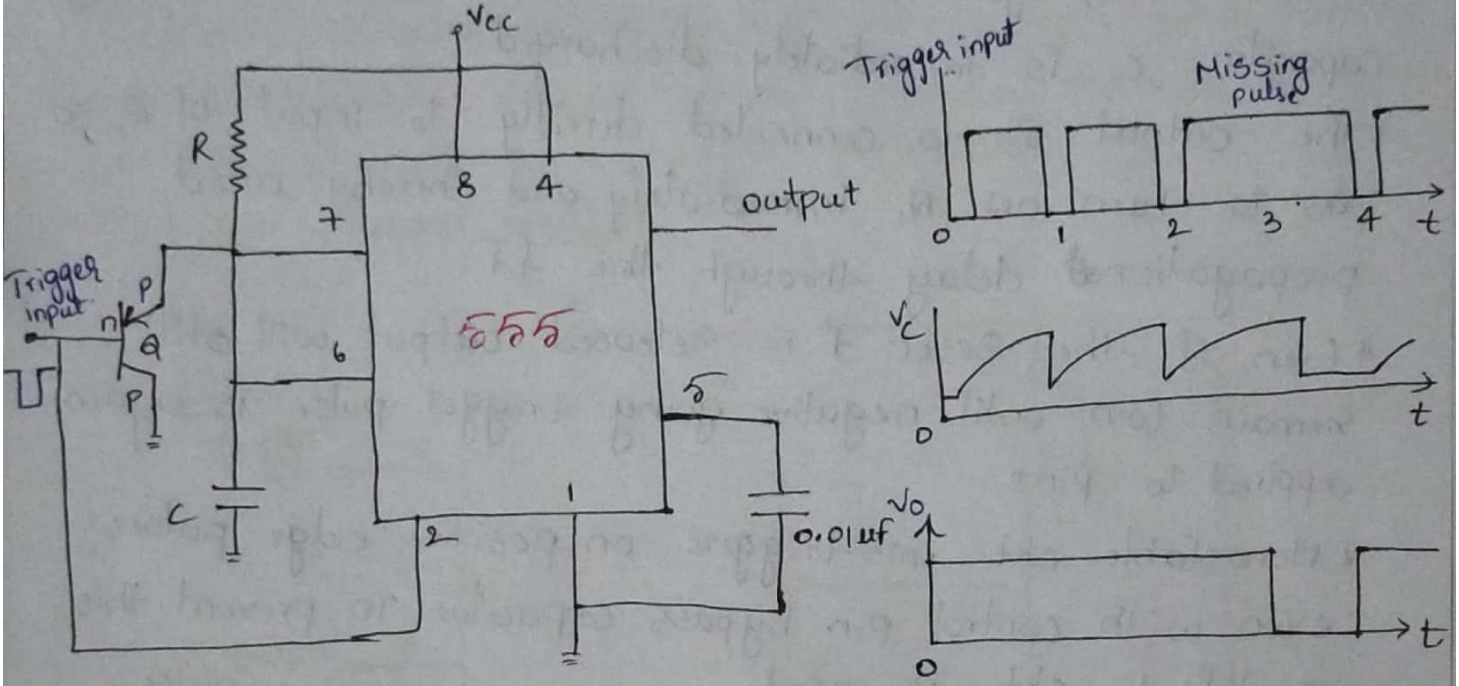


waveform at pin2

* The resistor and capacitor combination forms the differentiator ckt. During the positive going edge of trigger, diode D becomes forward biased, thereby limiting amplitude of pulse positive spike to 0.7V.

* Applications in Monostable Mode :-

• Missing pulse Detector :-



Missing pulse Detector Monostable ckt

output of Missing pulse detector.

* Whenever, input trigger is low, emitter diode of transistor Q is forward biased. The capacitor C gets clamped to 0.7V. The output of timer goes High.

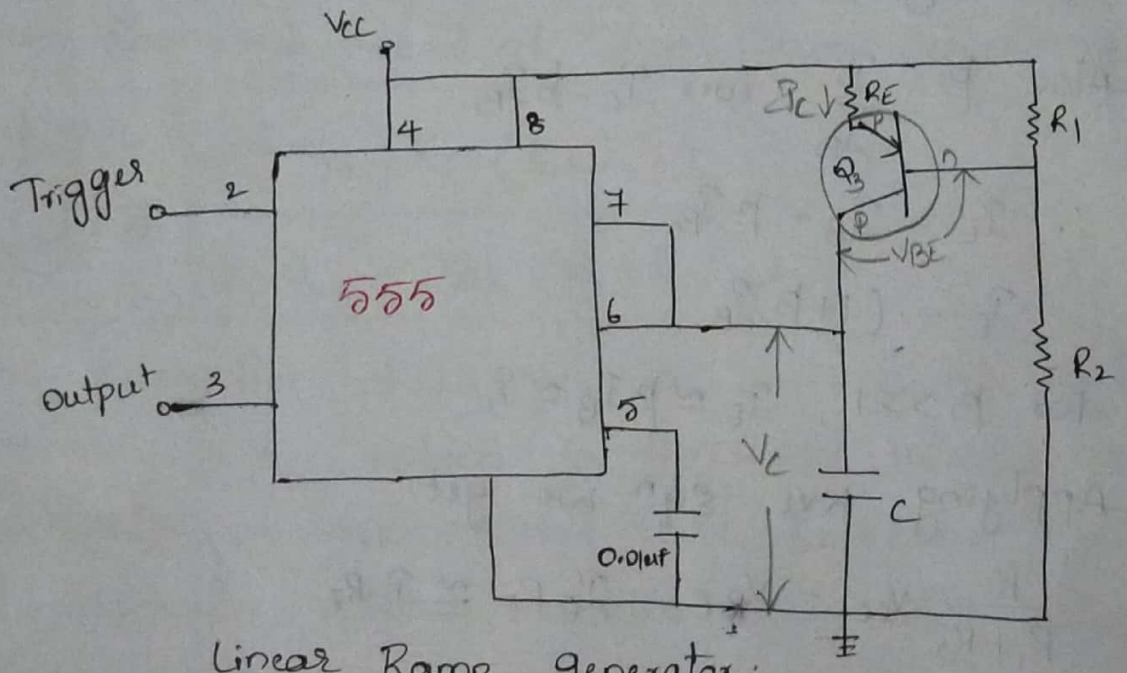
* The circuit is designed such that the time period of monostable ckt is slightly greater (1/3) than that of triggering pulses.

* As long as trigger pulse train keeps coming at pin 2 the output remains High. If a pulse misses the trigger input is High and transistor Q is cut off [off].

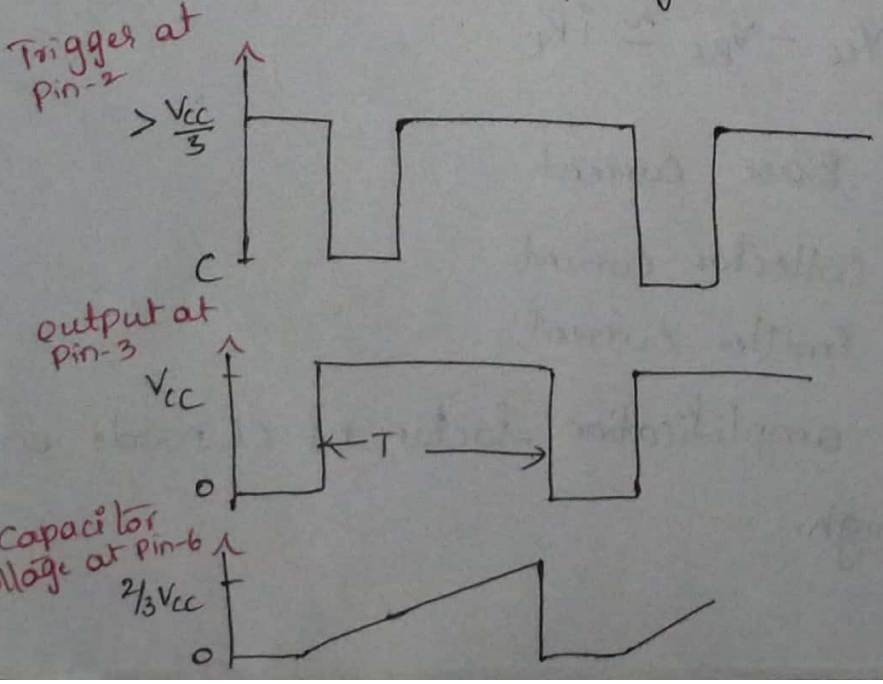
* The 555 timer enters into normal state of Monostable operation. The output goes low after time T of monoshot.
* This type of ckt used to detect the missing heartbeat It can also be used for speed control and measurement.

- pnp → when the base i/p is -ve then Q_1 - ON
- when trigger i/p high then Q_1 will be in off condition means missing condition
- whenever trigger i/p goes high the n-type base receives +ve value the Q will be off condition normal operation is resumed back to monostable multivibrator.

* Linear Ramp Generator :-



Linear Ramp generator.



* A linear ramp can be generated using the linear ramp generator. The resistor R of the monostable ckt is replaced by constant current source.

* The capacitor voltage V_c is charged linearly by the constant current source formed by transistor Q_3.

→ The capacitor voltage V_c given by

$$V_c = \frac{1}{C}\int_0^t i\,dt \quad \text{— (1)}$$

Where i - current supplied by the constant current source.

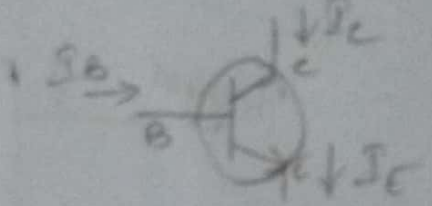
$V_c = \alpha t$, $\alpha = \frac{i}{C}$

$V_c = \frac{1}{C} i \int dt$

$V_c = \frac{i}{C} t$

$I_E = I_B + I_C$

Also $\beta = \frac{I_C}{I_B}$ (or) $I_C = \beta I_B$



$\therefore I_E = I_B + \beta I_B$

$I_E = (1+\beta) I_B$.

for $\beta >> 1$, $I_E \simeq \beta I_B \simeq I_C$

Applying KVL Eqn we get

$$\frac{R_1}{R_1+R_2} V_{CC} - V_{BE} = I_E R_E \simeq I_C R_E$$

(or) $$\frac{R_1}{R_1+R_2} V_{CC} - V_{BE} \simeq i R_E$$

Where I_B - Base current

I_C - Collector current

I_E - Emitter current

β - current amplification factor of CE mode and is very high.

$$i = \frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2)} \quad -(2)$$

Substituting value of current in V_c then

$$V_c = \left[\frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{C\, R_E (R_1+R_2)} \right] \times t$$

At time $t=T$ the capacitor voltage V_c becomes $\frac{2}{3}V_{CC}$

then $$\frac{2}{3}V_{CC} = \left[\frac{R_1 V_{CC} - V_{BE}(R_1+R_2)}{R_E (R_1+R_2)\, C} \right] \times T$$

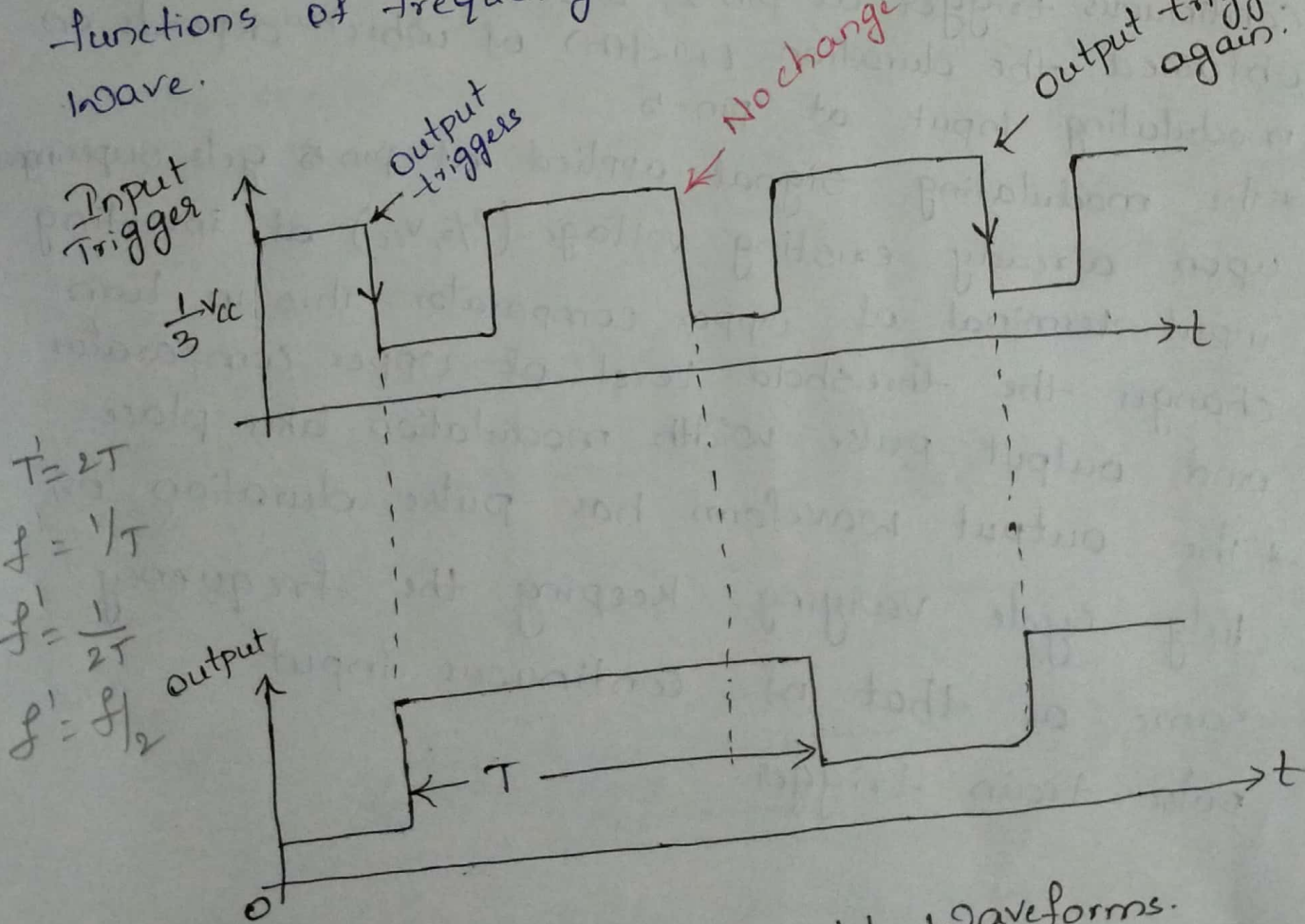
Thus the time period of linear ramp generator given by

$$T = \left[\frac{\left(\frac{2}{3}V_{CC}\right) R_E (R_1+R_2) C}{R_1 V_{CC} - V_{BE}(R_1+R_2)} \right]$$

*The capacitor discharges as soon as its voltage reaches $\frac{2}{3}V_{CC}$ which is threshold of the upper comparator in monostable ckt functional diagram. The capacitor voltage remains zero until another trigger pulse is applied.

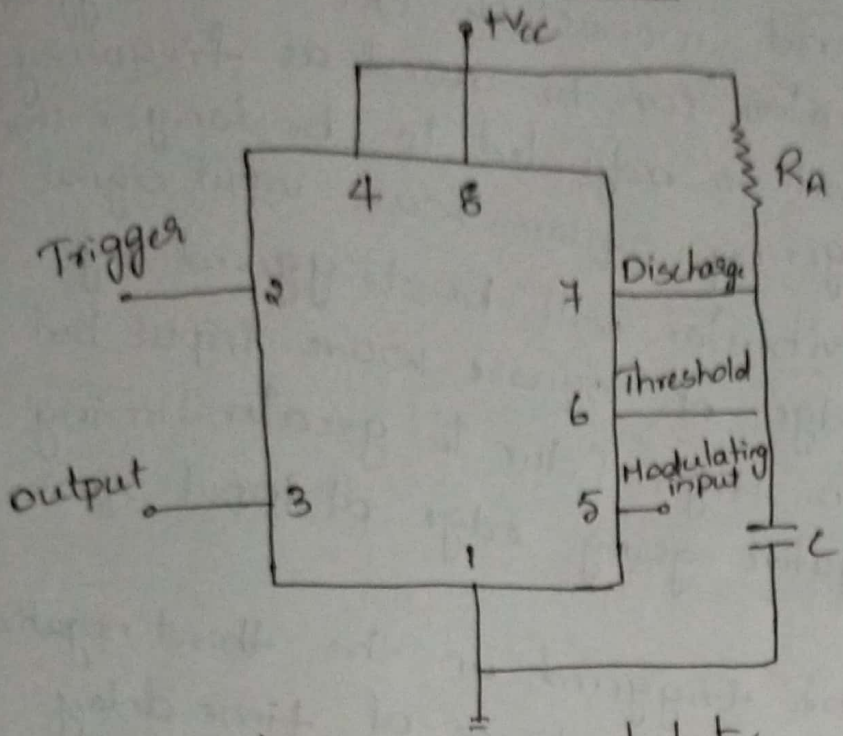
* Frequency Divider :-

* A continuously triggered monostable ckt when triggered by square wave generator can be used as frequency divider if timing interval is adjusted to be longer than the period of the triggering square-wave input signal.
* The monostable Multivibrator will be triggered by first negative going edge of square wave input but the output will remain High [due to greater timing interval] for next negative going edge of input square-wave.
* The monoshot will be triggered on the third negative going input, depending on the choice of time delay. Hence in this way, the output can be made integral functions of frequency of the input trigger square-wave.

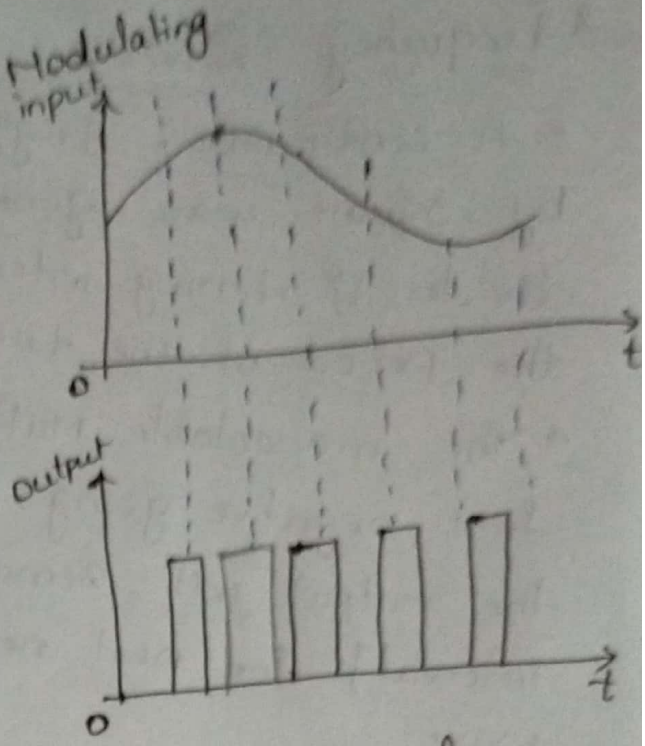


Freq. Divider ckt waveforms.

* Pulse Width Modulation :-



Pulse Width Modulator.

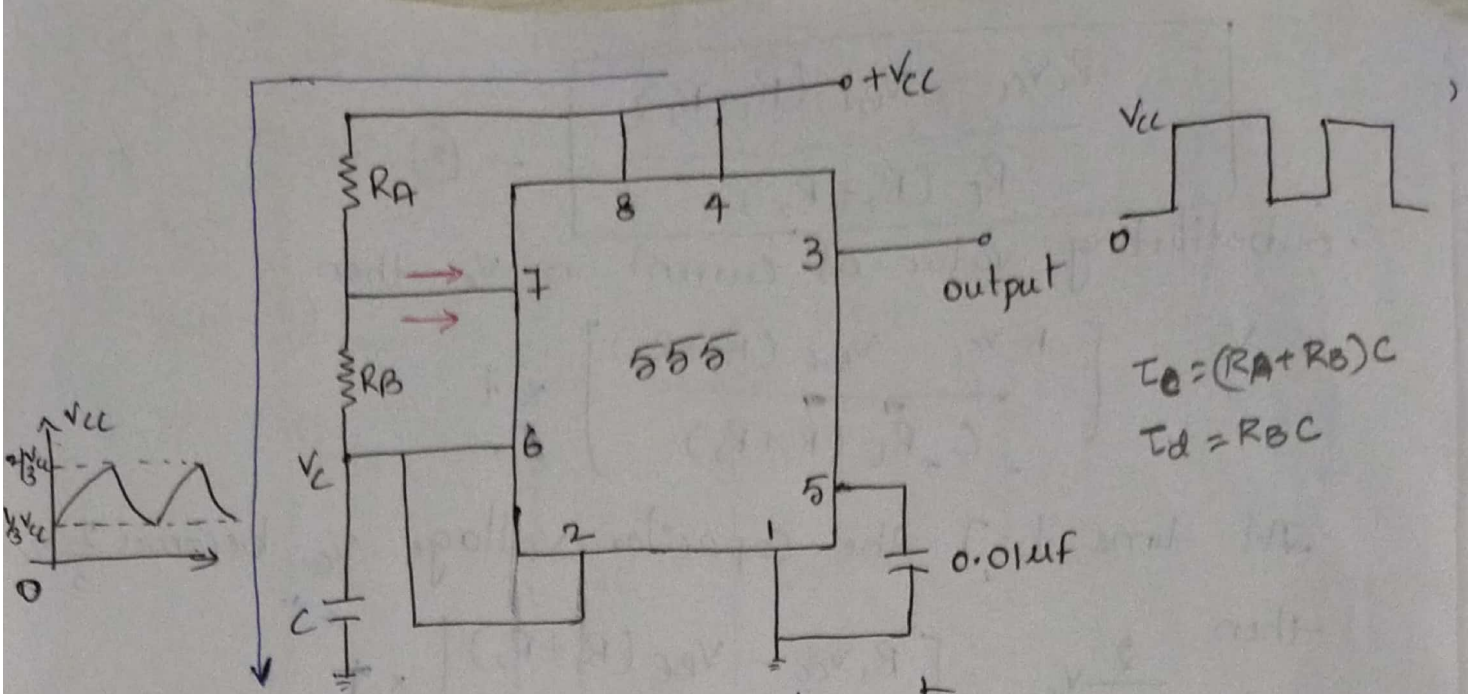


Output Waveform

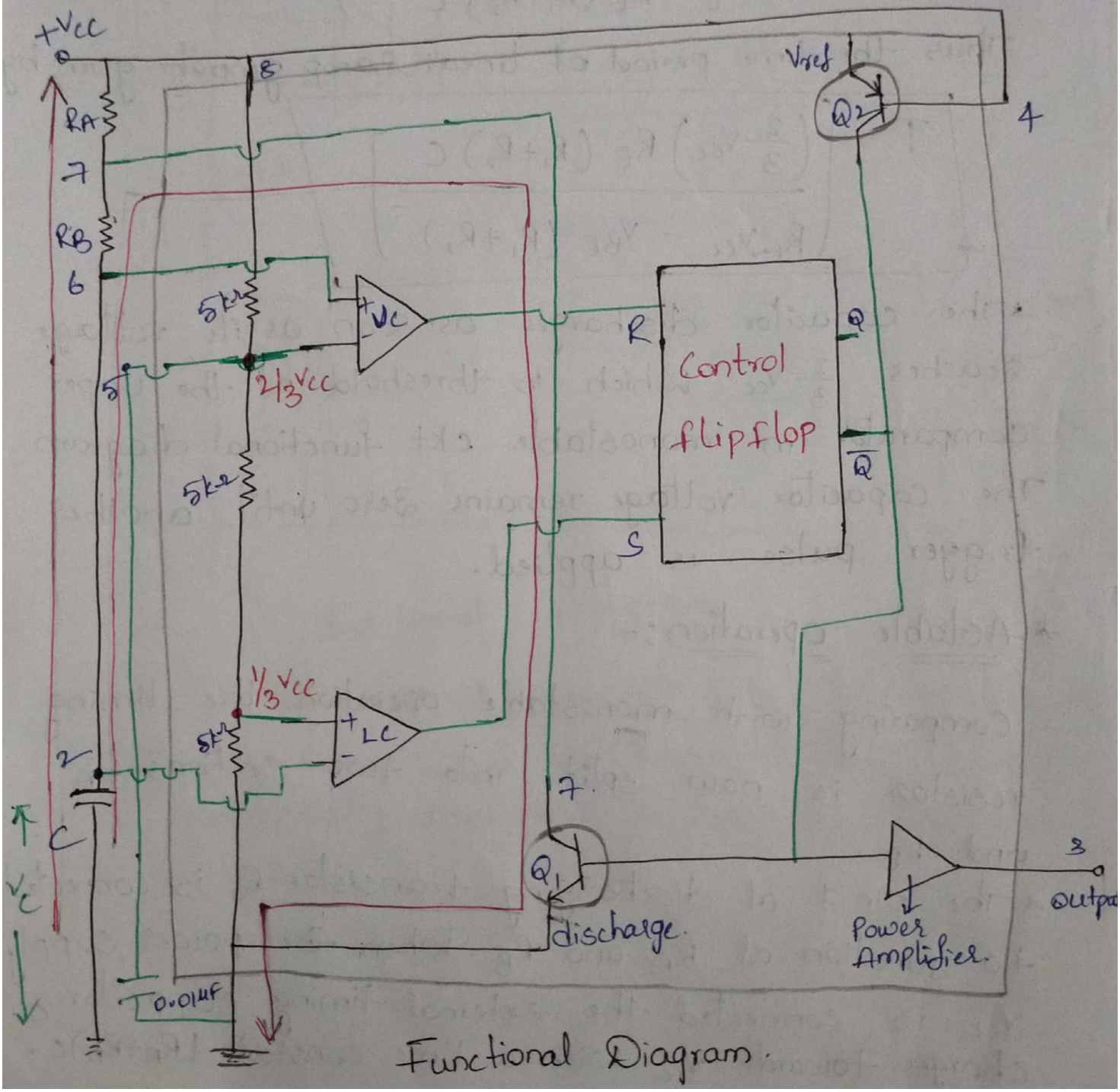
*This is basically a monostable multivibrator with modulating input signal applied at pin 5. By application of continuous trigger at pin 2, a series of output pulses are obtained the duration (width) of which depends on modulating input at pin-5.

*The modulating signal applied at pin 5 gets superimposed upon already existing voltage ($\frac{2}{3}V_{cc}$) at inverting input terminal of upper comparator. This in turn changes the threshold level of upper comparator and output pulse width modulation takes place.

*The output waveform has pulse duration or duty cycle varying. keeping the frequency same as that of continuous input pulse-train trigger.

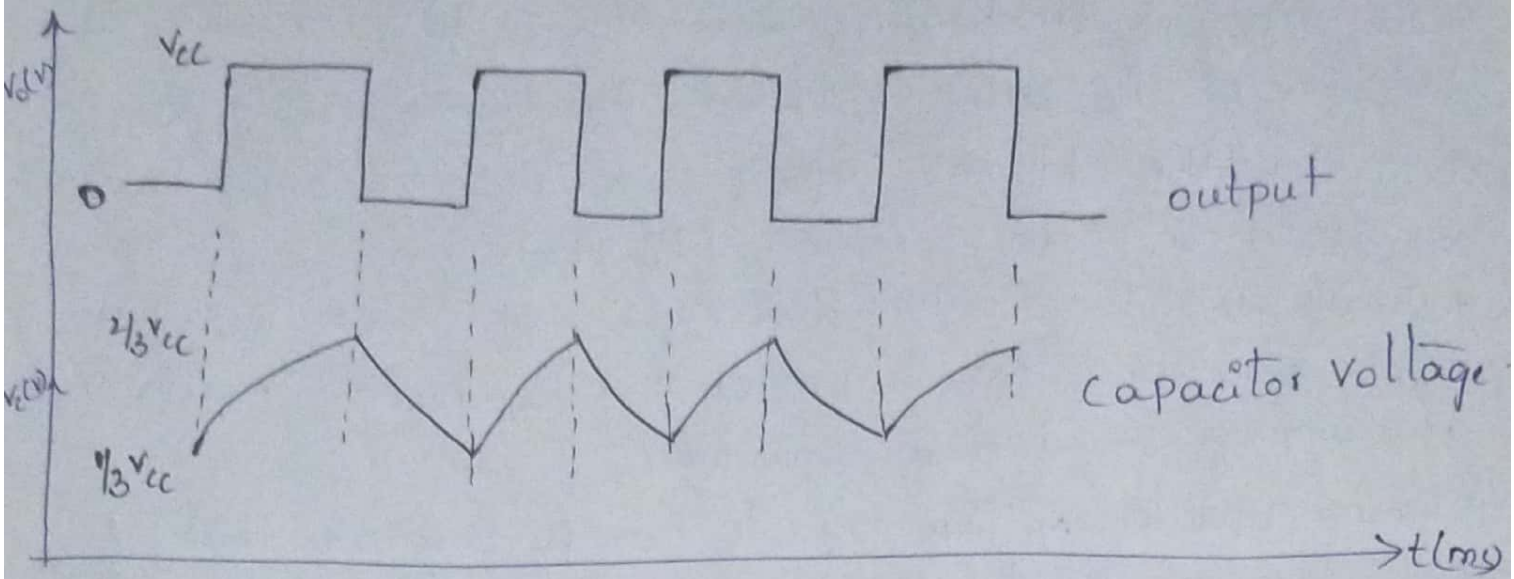


Astable Multivibrator



Functional Diagram.

* The pin 7 of discharging transistor Q_1 is connected to junction of R_A and R_B. When the power supply V_{CC} is connected the external timing capacitor 'c' charges towards V_{CC} with a time constant $(R_A + R_B)C$.
* During this time, output (Pin 3) is high [equal to V_{CC}] as reset $R=0$ and set $S=1$ and this combination makes $\bar{Q}=0$ unclamping the timing capacitor C.
* When capacitor voltage equals [or just greater than] $\frac{2}{3}V_{CC}$ the upper comparator triggers the control flip flop so that $\bar{Q}=1$.
* This in turn makes transistor Q_1 ON and capacitor C starts discharging towards ground through R_B and transistor Q_1 with time constant R_BC. The current also flows into transistor Q_1 through R_A.
* Resistors R_A and R_B must be large enough to limit this current and prevent damage to discharge transistor Q_1.
* During the discharge of timing capacitor C, as it reaches [just less than] $\frac{V_{CC}}{3}$ the lower comparator is triggered and at this stage $S=1$, $R=0$ which turns $\bar{Q}=0$.
* $\bar{Q}=0$ unclamps the external timing capacitor C. The capacitor is periodically charged and discharged between $\frac{2}{3}V_{CC}$ and $\frac{1}{3}V_{CC}$ resp.
* The length of time that output remains High is the time for capacitor to charge from $1/3\ V_{CC}$ to $2/3\ V_{CC}$.



Timing sequence of Astable Multivibrator.

The capacitor voltage for low pass RC ckt subjected to step input of V_{cc} is given by

$$V_c = V_{cc}\left[1 - e^{-t/RC}\right]$$

The time t_1 taken by the ckt to charge from 0 to $\frac{2}{3}V_{cc}$

$$\frac{2}{3}V_{cc} = V_{cc}\left[1 - e^{-t_1/RC}\right]$$

$$\boxed{t_1 = 1.09RC}$$

The time t_2 taken by the ckt to charge from 0 to $\frac{1}{3}V_{cc}$ is

$$\frac{1}{3}V_{cc} = V_{cc}\left[1 - e^{-t_2/RC}\right]$$

$$\boxed{t_2 = 0.405RC}$$

So time to charge from $\frac{1}{3}V_{cc}$ to $\frac{2}{3}V_{cc}$ is

$$t_{high} = t_1 - t_2$$

$$= 1.09RC - 0.405RC$$

$$t_{high} = 0.69RC$$

for given ckt

$$\boxed{t_{high} = 0.69\left[R_A + R_B\right]C}$$

*The output is low, while the capacitor discharges from $\frac{2}{3}V_{cc}$ to $\frac{1}{3}V_{cc}$ and voltage across the capacitor is given by

$$V_c(t) = V_{cc} e^{-t/RC}$$

$$\frac{1}{3}V_{cc} = \frac{2}{3}V_{cc} e^{-t/RC}$$

$$t = 0.69RC$$

for given ckt $\boxed{t_{low} = 0.69R_BC}$

Both R_A and R_B are in charge path but only R_B in discharge path.

Total time, $T = t_{High} + t_{low}$

$$T = 0.69(R_A + R_B)C + 0.69R_BC$$

$$T = 0.69(R_A + 2R_B)C.$$

$$\boxed{f = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}}$$

The duty cycle is defined as the ratio of ON time to total time period (T). [$T = T_{ON} + T_{off}$]

$$D = \frac{t_{ON}}{t_{ON} + t_{off}}$$

When transistor Q_1 is ON output goes low.

$$D\% = \frac{t_{low}}{T} \times 100 \quad \Rightarrow D\% = \frac{0.69R_B}{0.69(R_A + 2R_B)} \times 100$$

$$D\% = \frac{R_B}{R_A + 2R_B} \times 100.$$

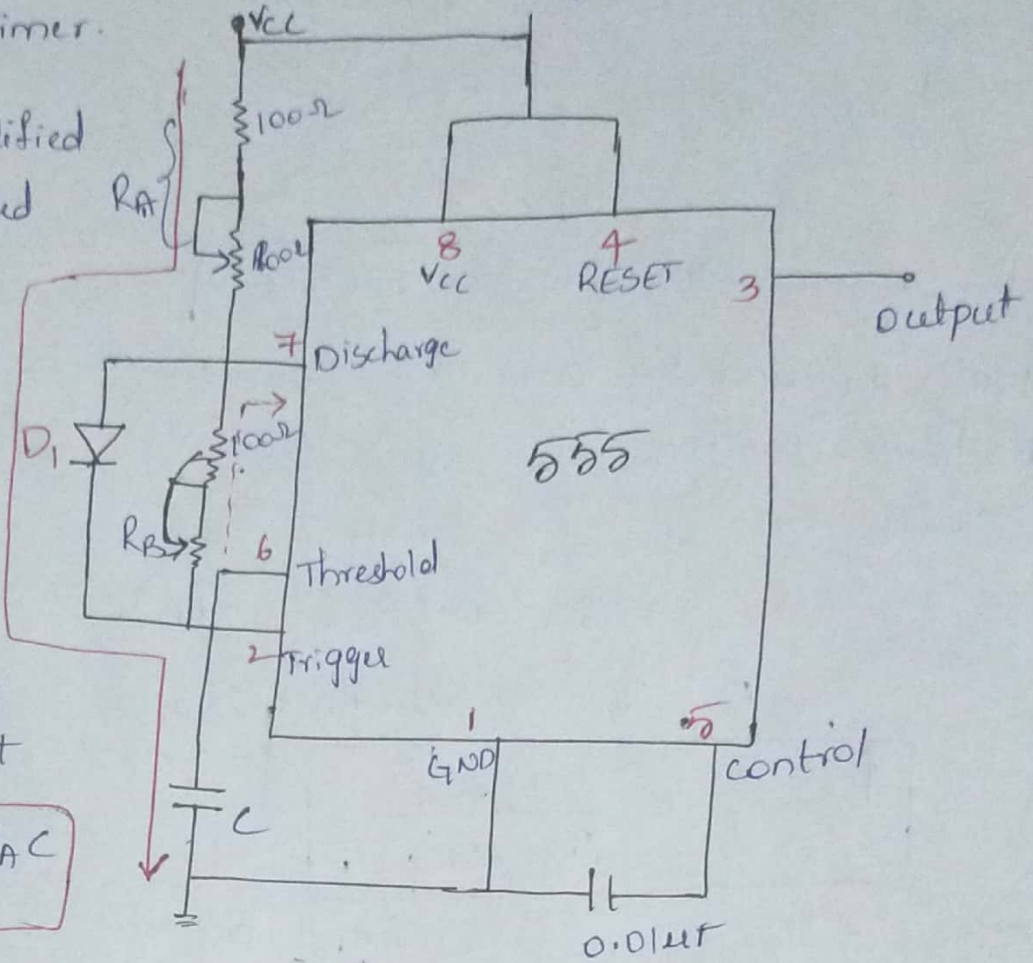
*Hence with existing ckt it is not possible to have duty cycle more than 50% since $t_{High} = 0.69C(R_A + R_B)$ will always be greater than $t_{low} = 0.69R_BC$.

*In order to obtain symmetrical square wave i.e D = 50%, the resistance R_A must be reduced to zero However pin 7 is connected directly to V_{cc} and extra current flows through Q_1 when Q_1 is turned ON. This may damage Q_1 and hence the timer.

*Thus the modified ckt is considered

During the charging portion of cycle, diode D_1 is F.B effectively short circuiting R_B such that

$$t_{High} = 0.69 R_A C$$



Adjustable Duty cycle rectangular wave generator

*However during the discharging portion of cycle, transistor Q_1 turns ON thereby grounding pin 7 and hence diode D_1 turns RB.

$$t_{low} = 0.69 R_B C$$

$$T = t_{High} + t_{low}$$

$$T = 0.69(R_A + R_B)C$$

$$f = \frac{1}{T} = \frac{1.45}{0.69(R_A + R_B)C}$$

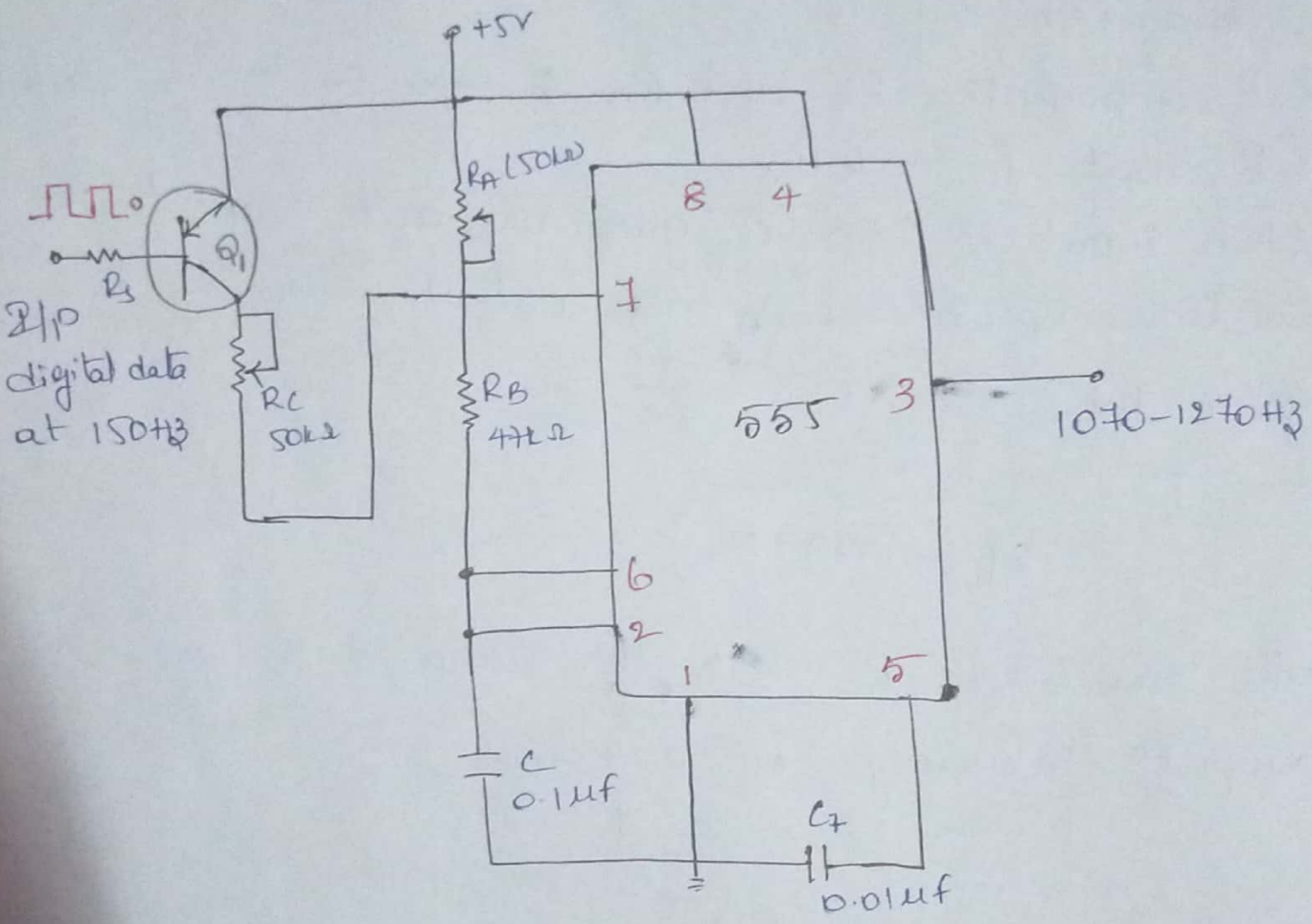
and duty cycle $D = \frac{R_B}{R_A + R_B}$

* Resistors R_A and R_B should be made variable to allow adjustment of freq and pulse width.
* A series resistor of atleast 100Ω [fixed] must be added to each R_A and R_B this will limit peak current to discharge transistor Q_1 when variable resistors are of min value.

If $R_A = R_B$ then 50% of duty cycle is achieved.

* Applications in Astable Mode :-

i. fsk Generator :-



* In digital data communication binary code is transmitted by shifting carrier freq. b/w two present frequencies This type of transmission is called frequency shift keying (fsk) technique.

* A 555 timer in astable mode can be used to generate fsk signal. The standard digital data input frequency is 150 Hz.
• When input is High, transistor Q is off and 555 timer works in normal astable mode of operation. freq. of o/p waveform given by.

$$f_o = \frac{1.45}{(R_A + 2R_B)C}$$

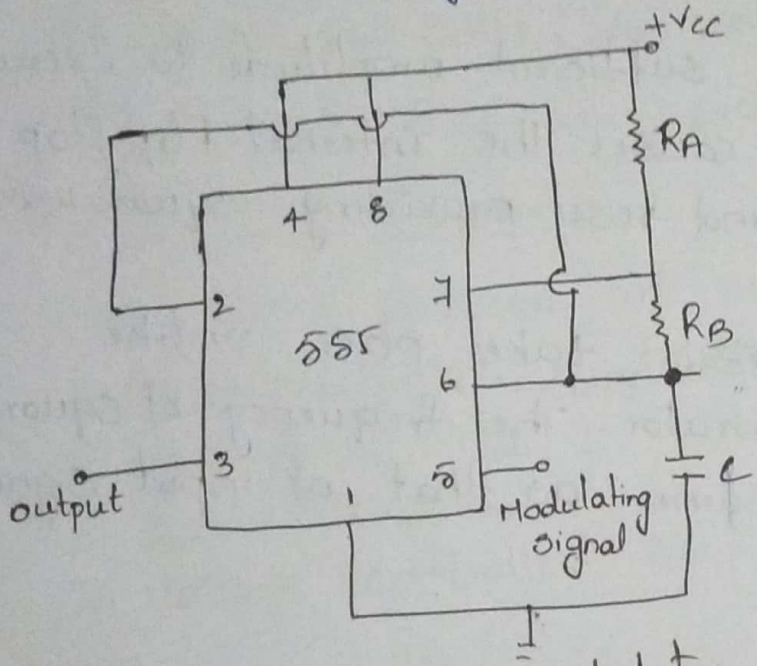
* In tele-typewriter using modular-demodulator [MODEM] freq. b/w 1070 Hz to 1270 Hz is used to as one of standard fsk signals.
The components R_A and R_B & capacitor C is selected such that $f_o = 1070$ Hz.
* When input is low Q goes ON and connects the resistance R_L across R_A. The output frequency is given by

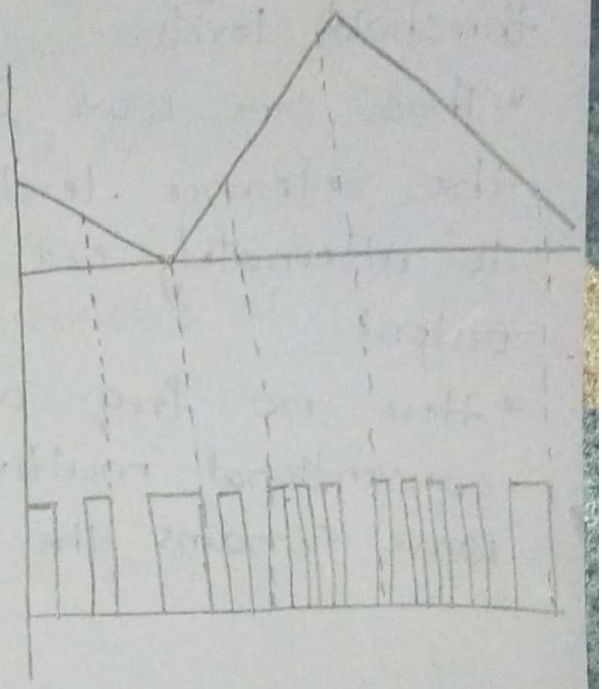
$$f_o = \frac{1.45}{C[(R_A \| R_L) + 2R_B]}$$

* The resistance, R_L can be adjusted to get an output frequency of 1270 Hz.

(2) Pulse position Modulator :-

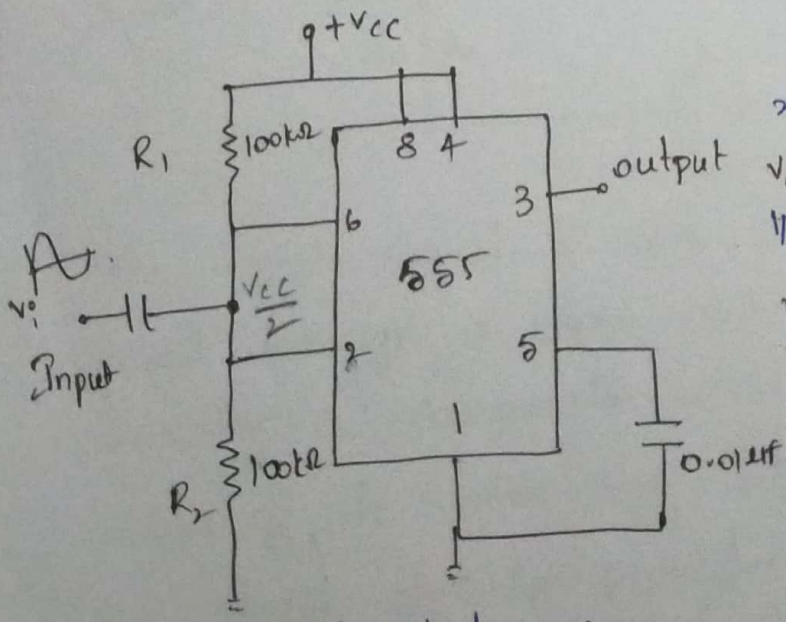
- The pulse position modulator can be constructed by applying a modulating signal to pin 5 of 555 timer connected for Astable Multivibrator.
- The output of pulse position varies with the modulating signal, since the threshold voltage and hence time delay is varied.



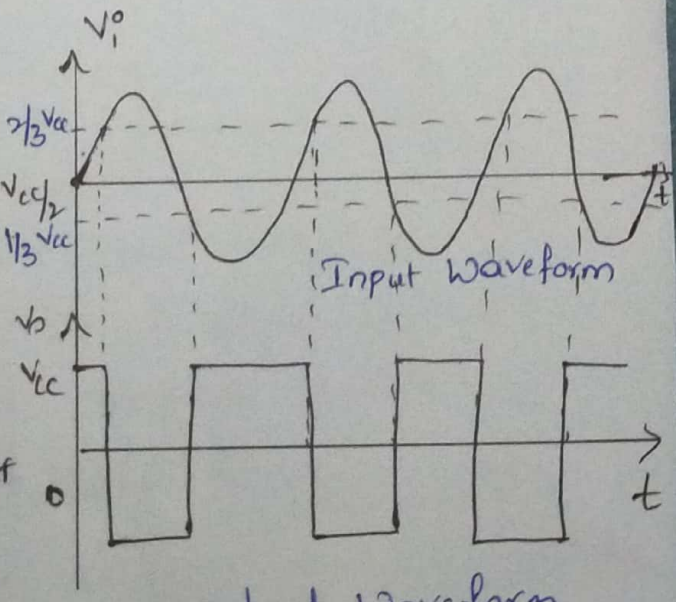


Pulse position Modulator.

* Schmitt Trigger :-



Schmitt trigger.



output Waveform

* A 555 timer can be used as Schmitt Trigger or 18 Squaring circuit.

Here two internal comparators are tied together and externally biased at $V_{cc}/2$ through R_1 & R_2.

* Since the upper comparator will be trip at $\frac{2}{3}V_{cc}$ and lower comparator will trip at $\frac{1}{3}V_{cc}$ the bias provided by R_1 & R_2 is centered within these two threshold levels.

* Thus, sine wave of sufficient amplitude to exceed the reference levels causes the internal flip flop to alternately set and reset providing square wave output.

* Here no freq. division takes place, unlike conventional multivibrator. The frequency of square wave remains the same as that of input signal.

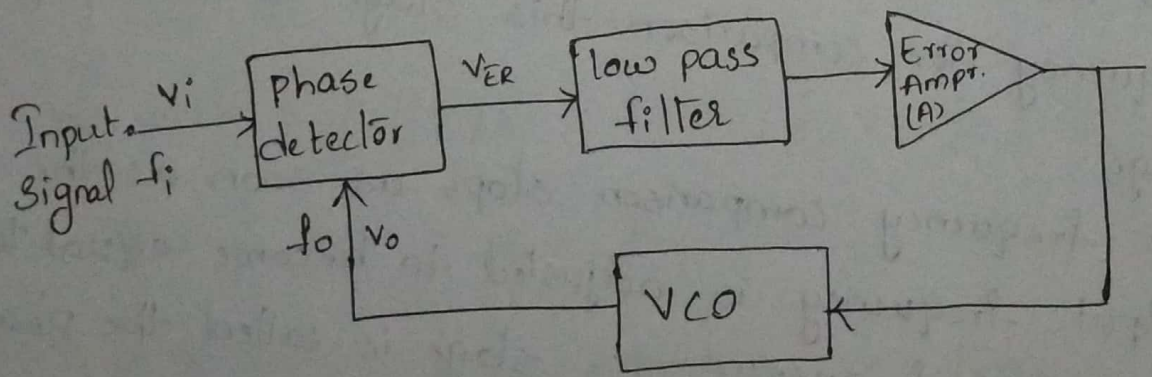
*phase locked loop:-

- The advancement in the field of integrated circuits, PLL has become one of the main building blocks in the electronics technology.
- The phase locked loop (PLL) is an important building block of linear systems.
- In present, the PLL is available as a single IC in the SE/NE 560 series [560, 561, 562, 564, 565 and 567)
- The discrete IC's are used to construct a PLL.

*PLL Block Diagram:-

The block diagram of PLL consists of:

i) phase detector / comparator
ii) Low pass filter.
iii) Error Amplifier
iv) Voltage controlled oscillator [VCO].



The input signal V_i with an input frequency f_i is passed through a phase detector. A phase detector basically a comparator which compares the input frequency f_i with the feedback frequency f_o.

*The phase detector provides an output error voltage $V_{ER} = (f_i + f_o)$ which is a DC voltage.

* This Dc voltage is then passed on to an LPF. The LPF removes the high frequency noise and produces a steady Dc level. $V_f (= f_i - f_o)$ V_f also represents the dynamic characteristics of the PLL.
* The Dc level is then passed on to a VCO. The output frequency of the VCO (f_o) is directly proportional to the input signal. Both the input frequency and output frequency are compared and adjusted through feedback loops until the output frequency equals to the input frequency.
- Thus the PLL works in these stages - free running, capture and phase lock.
- The free running stage refers to the stage when there is no input voltage applied.
- As soon as the input frequency is applied the VCO starts to change and begin producing an output frequency for comparison this stage is called capture stage.
- The frequency comparison stops as soon as the output frequency is adjusted to become equal to the input frequency. This stage is called the phase locked state.

i. Lock-in-Range :- once PLL is locked, it can track freq. changes in incoming signals. The range of freq's over which PLL can maintain lock with incoming signal is called lock-in-range or tracking range. It is expressed as percentage of f_o, VCO frequency.

(ii) Capture Range :- The range of freq's over which PLL can acquire lock with an input signal is called capture range. It is expressed as percentage of f_0.

(iii) Pull in time :- The total time taken by PLL to establish lock is called pull in time. This depends on initial phase and freq. difference b/w two signals as well as on overall loop gain and loop filter characteristics.

* Voltage Controlled oscillator (VCO) :-

. The main function of the VCO is to generate an output frequency that is directly proportional to the input voltage.

* VCO is a circuit at which output signal frequency is controlled by the input voltage.

* The frequency of oscillation for the RC oscillator is $f = \frac{1}{2\pi RC}$ $\therefore f \propto \frac{1}{C}$

"If we increase f, C decreases, If f decreases, C increases

The frequency of oscillation for the LC oscillator

$$f = \frac{1}{2\pi\sqrt{LC}} \quad \therefore f \propto \frac{1}{C}$$

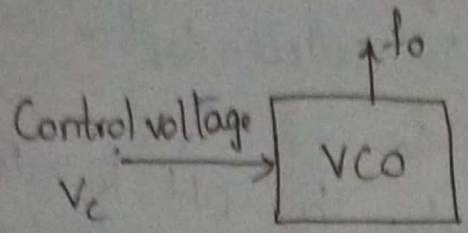
$$V_{in} \text{ (or) } V_c = \frac{1}{C}\int i\,dt. \qquad \left[V = \frac{1}{C}\int i\,dt\right]$$

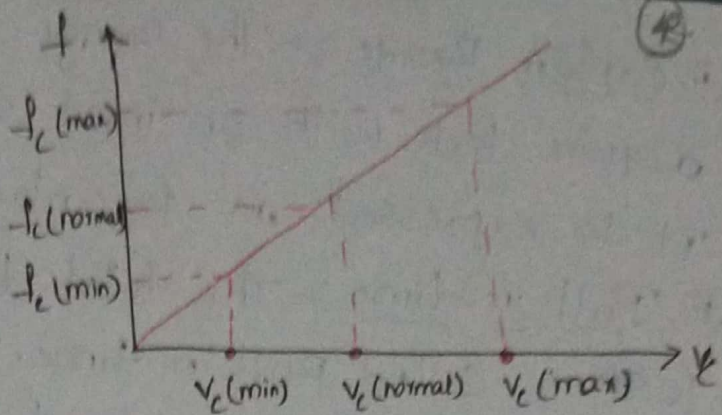
$$V_c = \frac{i}{C}\int dt \Rightarrow V_c = \frac{I}{C}t.$$

$$V_c \propto \frac{1}{C} \qquad [V_{in} \text{ increases } C \text{ decreases}]$$

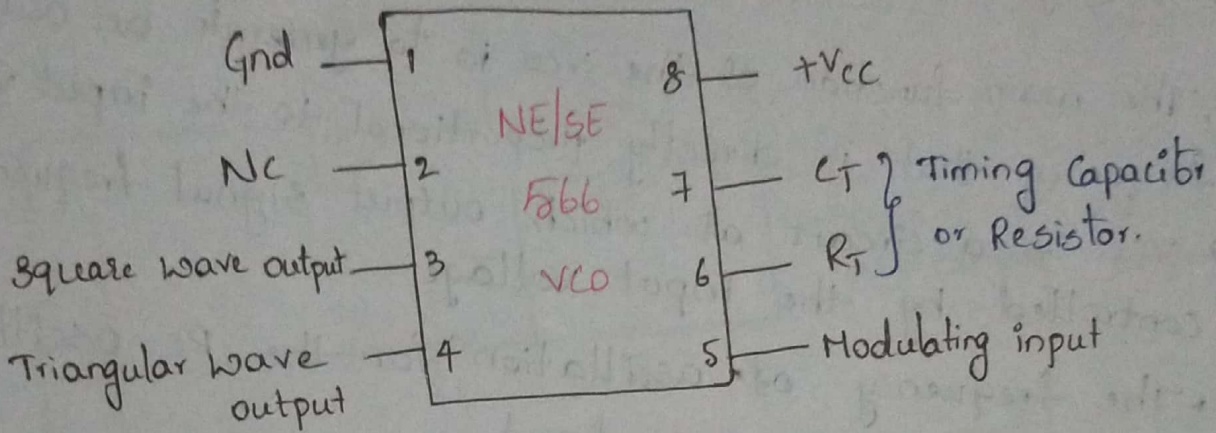
$$\boxed{V_{in} \text{ (or) } V_c \propto f \propto \frac{1}{C}}$$

$\therefore$ Hence the input voltage or control voltage and frequency of oscillation are directly proportional.



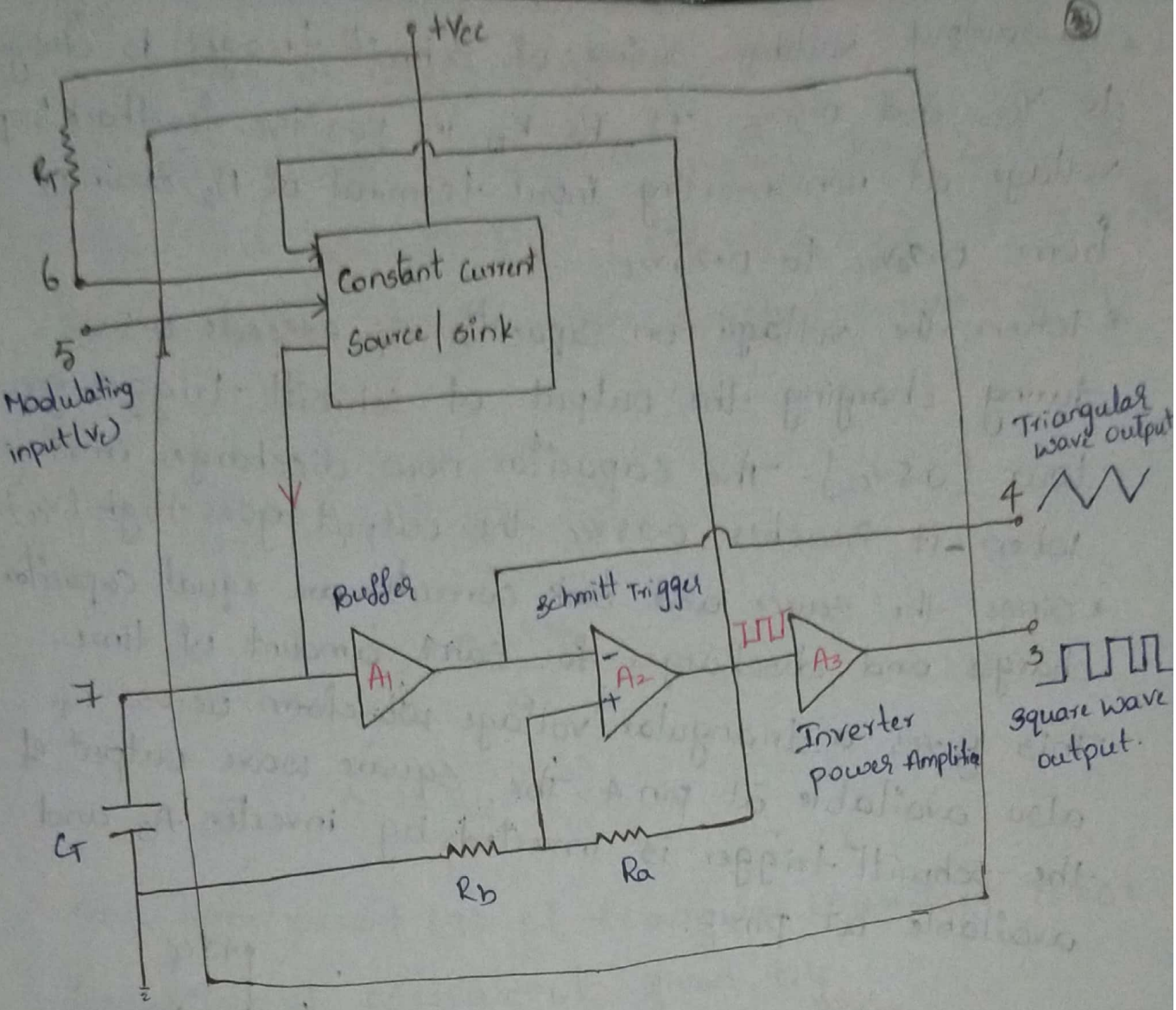


* Pin diagram :-



* VCO provides simultaneous square wave and triangular wave outputs as a function of the input voltage. The frequency of oscillation is determined by the resistor R and capacitor C along with the voltage V_c applied to the control terminal.

- A timing capacitor C_T is linearly charged (or) discharged by constant current source / sink. The amount of current can be controlled by charging the voltage V_c applied at the modulating input (pin 5) (or) by changing the timing resistor R_T external to IC chip.



Block diagram.

* Constant current source/sink will provides the constant current to buffer if they is increase or decreases in the depending on that capacitor, charges or discharges.
* Same voltage should be applied to modulating input (V_c) pin 5 and to pin 6.

Then it forms loop. Apply KVL

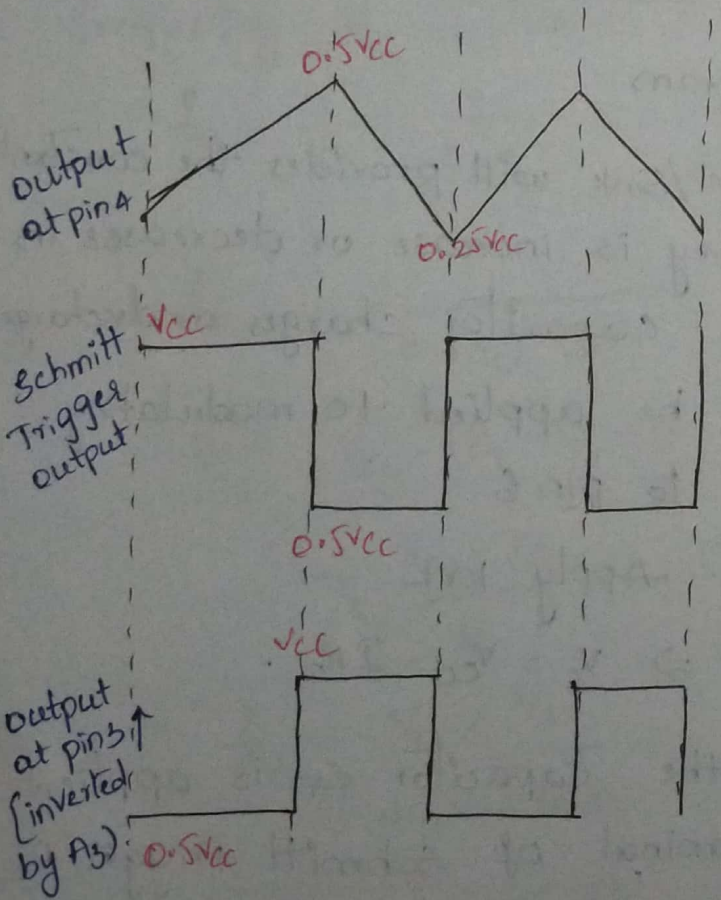
$$V_{CC} - I R_T - V_c = 0 \Rightarrow V_c = V_{CC} - I R_T .$$

* The voltage across the capacitor C_T is applied to inverting input terminal of schmitt trigger A_2 via buffer amplifier A_1.

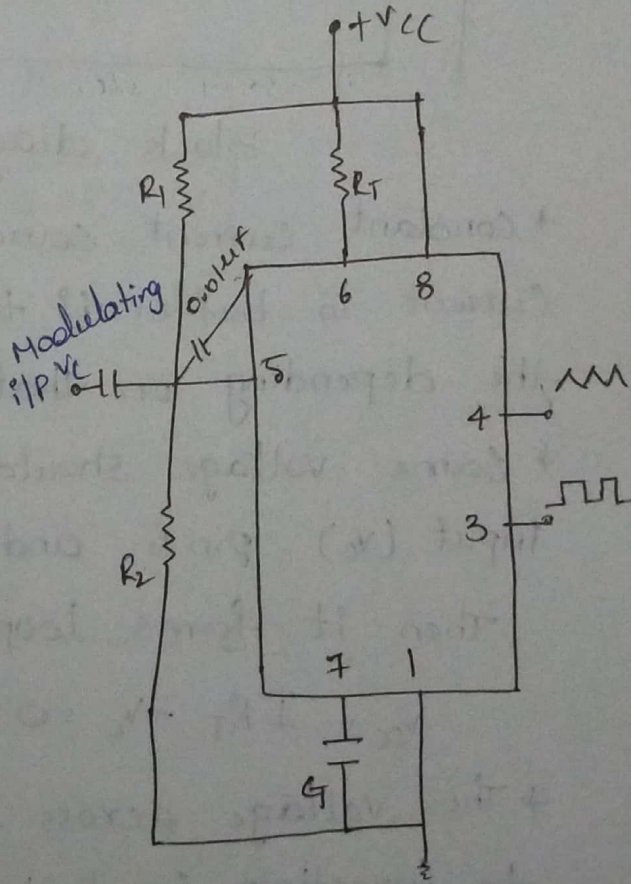
* The output voltage swing of schmitt trigger is designe to V_{cc} and $0.5V_{cc}$. If $R_a = R_b$ in positive feedback loop voltage at non-inverting input terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$

* When the voltage on capacitor C_T exceeds $0.5V_{cc}$ during charging the output of schmitt trigger goes low $[0.5V_{cc}]$. The capacitor now discharges and when it reaches $0.25V_{cc}$ the output goes high (V_{cc}).

* Since the source and sink currents are equal capacitor charges and discharges for same amount of time. This gives a triangular voltage waveform across C_T also available at pin 4. The square wave output of the schmitt trigger is inverted by inverter A_3 and available at pin 3.



Output Waveform



Connection Diagram

* Calculation of output frequency :-

The total voltage on capacitor changes from $0.25V_{cc}$ to $0.5V_{cc}$. Thus $\Delta V = 0.25V_{cc}$ [$\Delta V_c = V_2 - V_1 = 0.5 - 0.25 = 0.25V_{cc}$]

The capacitor charges with constant current source.

$$V_c = \frac{1}{C}\int i\,dt$$

$$C\frac{dV_c}{dt} = i \Rightarrow \frac{i}{C} = \frac{dV_c}{dt}$$

$$\frac{\Delta V}{\Delta t} = \frac{i}{C_T} \Rightarrow \frac{0.25V_{cc}}{\Delta T} = \frac{i}{C_T}$$

$$\Delta T = \frac{0.25V_{cc}\,C_T}{i}$$

The time period (T) of triangular waveform $T = 2\Delta t$.

frequency of oscillator f_o given by

$$f_o = \frac{1}{T} = \frac{1}{2\Delta T} = \frac{1}{2\left[\frac{0.25V_{cc}\,C_T}{i}\right]}$$

$$f_o = \frac{i}{0.5V_{cc}\,C_T}$$

But $V_{cc} - iR_T - V_c = 0$

$$i = \frac{V_{cc} - V_c}{R}$$

$$f_o = \frac{V_{cc} - V_c}{0.5V_{cc}\,C_T R_T}$$

$$\boxed{f_o = \frac{2[V_{cc} - V_c]}{V_{cc}\,C_T R_T}}$$

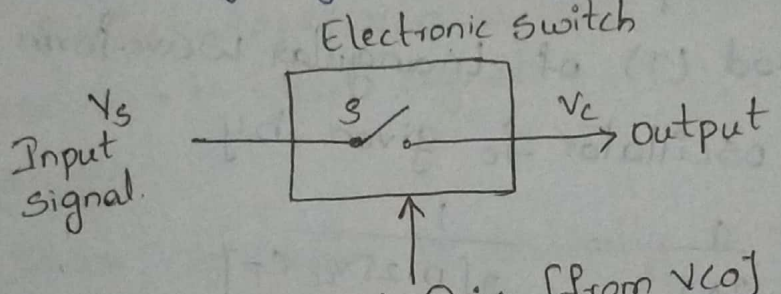
* The output frequency of VCO can be changed either by changing (i) R_T (ii) C_T or (iii) voltage V_c at modulating input terminal pin 5. The voltage V_c can be varied by connecting R_1, R_2 ckt.

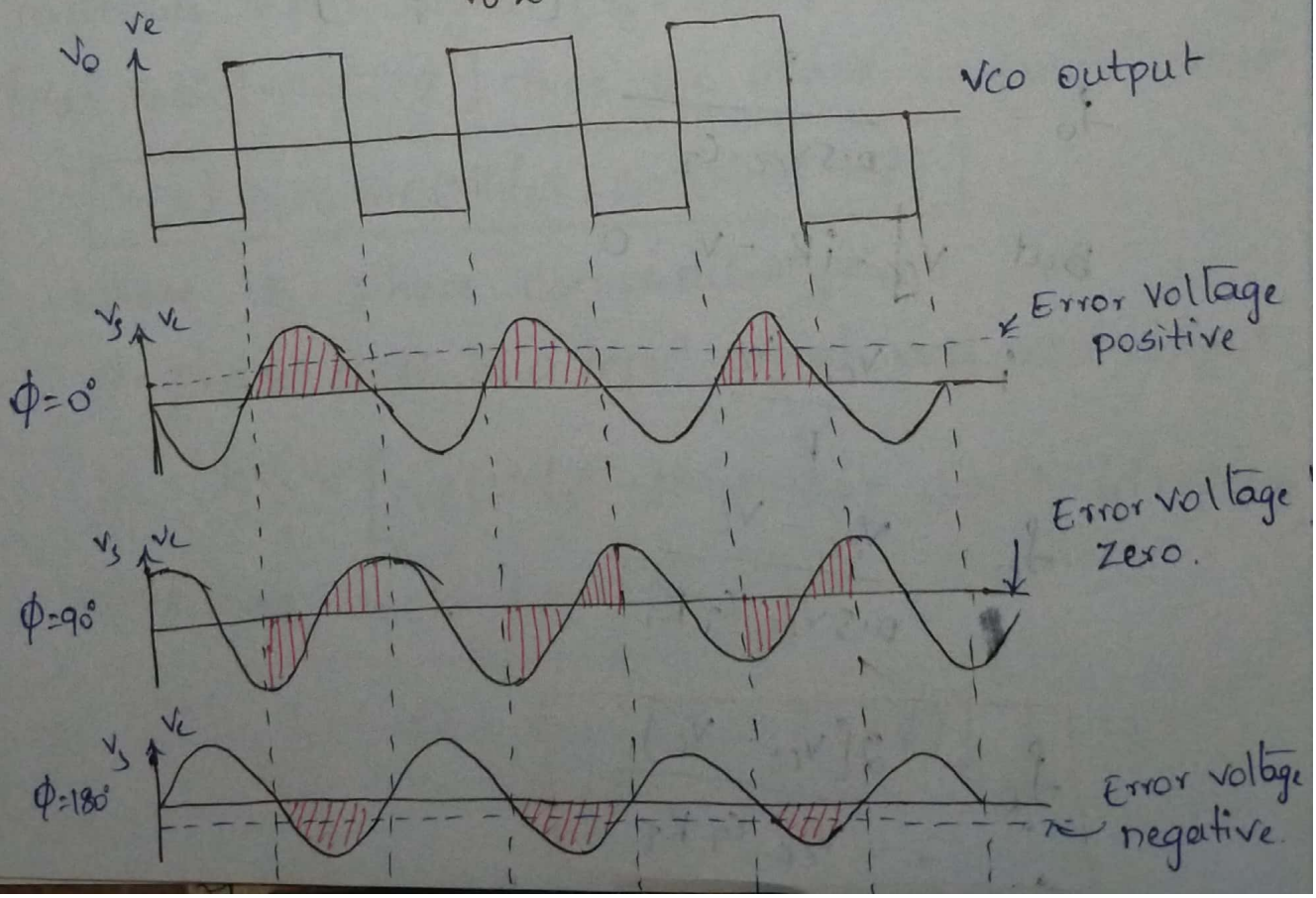
* Phase Detector / Comparator :-

The phase detection is most important part of PLL system There are two types of phase detectors used - Analog and digital detectors.

(i) Analog phase Detector :-

The principle of analog phase detection uses switch type phase detector. An electronic switch 'S' is opened and closed by signal coming from VCO [square wave].





* The input signal is chopped at repetition rate determined by VCO frequency. The input signal V_s assumed to be in phase ($\phi = 0°$) with VCO output V_o.
* Since the switch 'S' is closed only when VCO output is +ve, the output waveform V_e will be half sinusoids. Similarly the output waveform for $\phi = 90°$ and $\phi = 180°$. This type of phase detector is called half wave detector. Since the phase information for only one half of input waveform is detected and averaged.
* The output of phase comparator when filtered through low pass filter gives an error signal which is average value of output waveform. Also the error voltage (V_e) is zero when the phase shift blw two inputs is 90°. Thus for perfect lock, VCO output should be 90° out of phase w.r.t input signal.

Analysis :-

A Phase comparator is basically a multiplier which multiplies input signal $[V_s = V_s \sin(2\pi f_s t)]$ by VCO signal $[V_o = V_o \sin[2\pi f_o t + \phi]]$ Thus the phase comparator output.

$$V_e = K V_s V_o \sin(2\pi f_s t) \sin(2\pi f_o t + \phi)$$

where K - phase comparator gain

ϕ - phase shift blw input signal and VCO output

$$V_e = \frac{K V_s V_o}{2} [\cos(2\pi f_s t - 2\pi f_o t - \phi] - \cos(2\pi f_s t + 2\pi f_o t + \phi]$$

when at lock i.e $f_s = f_o$

$$V_e = \frac{K V_s V_o}{2} [\cos(-\phi) - \cos(2\pi \times 2 f_o t + \phi)]$$

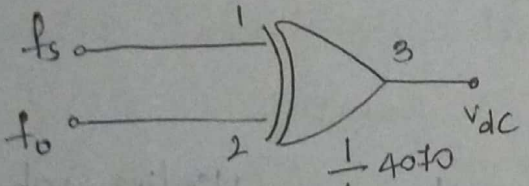
* This shows that phase comparator output contains double frequency term and dc term $\left[\frac{K V_s V_o}{2}\right] \cos\phi$ which varies as function of phase ϕ $[\cos\phi]$

• The double freq term is eliminated by LPF and dc signal is applied to modulating i/p terminal of VCO

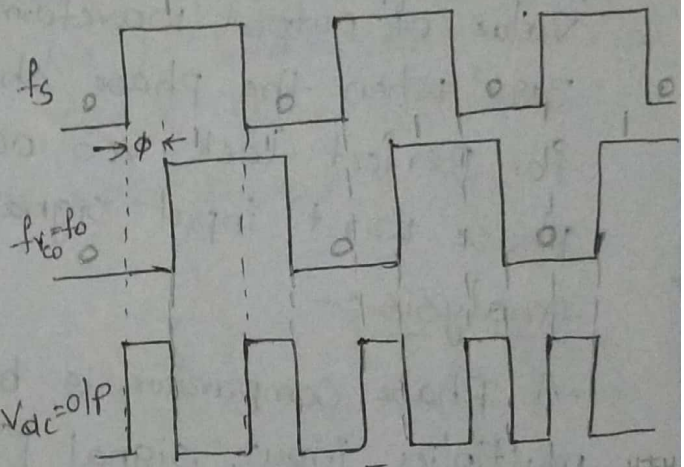
In perfect locked state $[f_s = f_o]$ $\phi = 90°$ $[\cos 90 = 0]$ such that we get zero error signal $[V_e = 0]$

* Digital Phase Detector :-

It uses CMOS type 4070 Quad 2-input XOR gate. The output of XOR gate is high when only one of input signal f_s or f_o is high. This type of detector is used when both input signals are square waves.



Ex-OR phase detector



Input & o/p waveforms

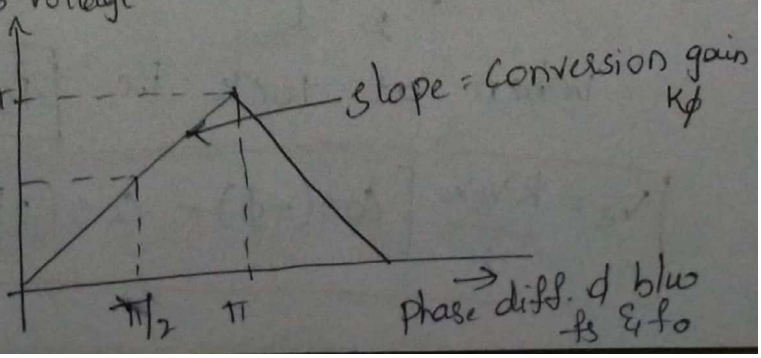
X-OR Truth table

0	0
0	1
1	0
1	0

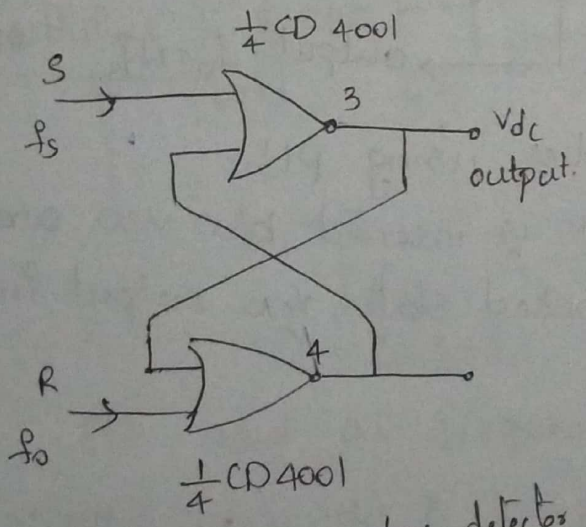
* The maximum dc o/p output voltage occurs when phase difference is π because the o/p of gate remains high throughout.

The slope of curve gives the conversion gain K_ϕ of the phase detector. So the conversion ratio K_ϕ for a supply voltage $V_{cc} = 5V$.

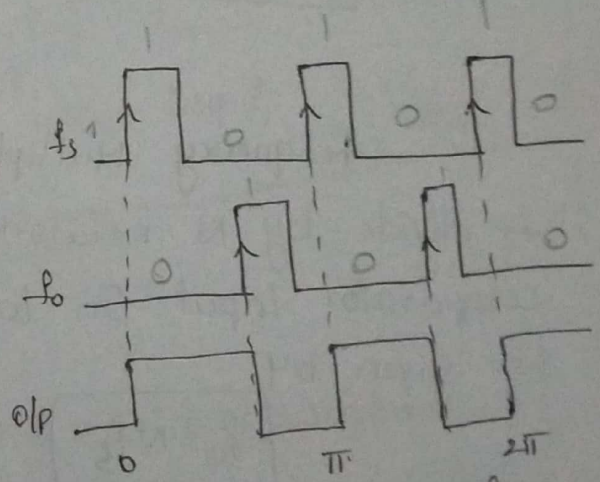
$$K_\phi = \frac{5}{\pi} = 1.59\ V/rad.$$



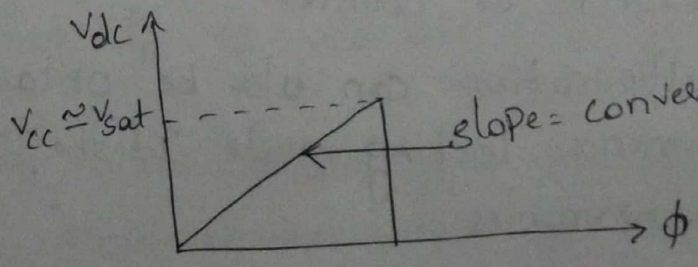
* Another type of phase digital phase detector is an Edge triggered phase detector. The ckt is an R-S flip flop made by NOR gates [CD 4001]
* This ckt is useful when f_s [incoming signal] and f_o [output signal] of VCO] are both pulse waveform with duty cycle less than 50%.
* The o/p of RS flip flop changes its state on leading edge of f_s and f_o. The variation of dc output voltage V_s phase difference b/w f_s & f_o is observed.
* This type of detector has better capture tracking and locking characteristics as dc output voltage is linear upto 360° compared to 180° in case of digital Ex-OR detector.
* This detector is also available in independent Monolithic Ic form. Ex: MC4344/4044. This Ic gives input/output transfer characteristics linear upto 4π rad or 720°.



Edge triggered phase detector



I/P & O/P waveform



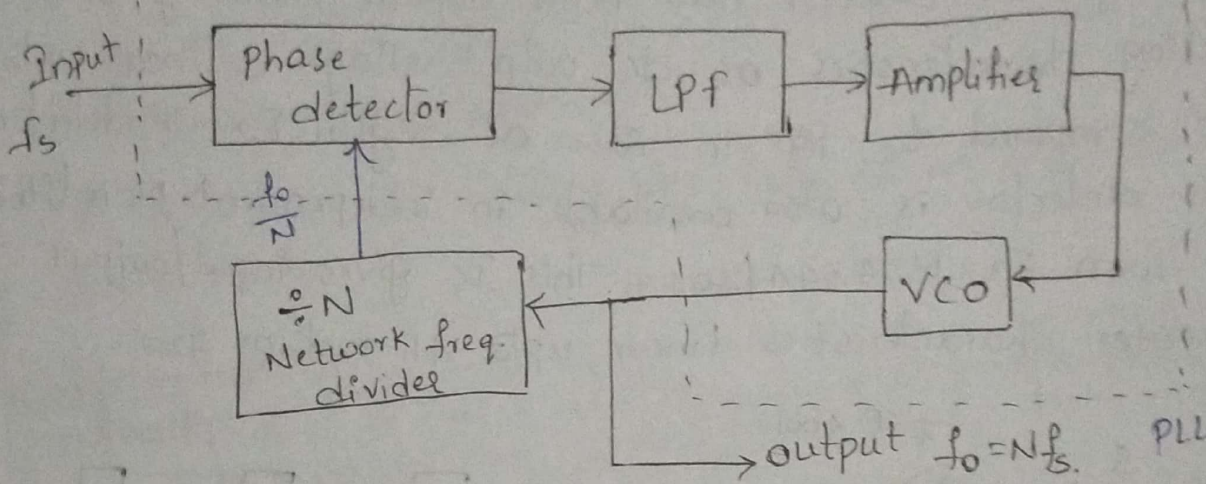
phase diff. b/w f_s & f_o.

*Application of PLL :-

The output from PLL system can be obtained either as voltage signal $V_c(t)$ corresponding to error voltage in feedback loop or as frequency signal at VCO output terminal.

*The voltage output is used in freq. discriminator application while the freq. o/p is used in signal conditioning, freq. synthesis or clk recovery applications.

*Frequency Multiplication / Division :-



Frequency Multiplier using PLL

A divide by 'N network is inserted b/w VCO and phase comparator input. In locked state, VCO output freq. f_o is given by

$$f_o = N f_s$$

The multiplication factor can be obtained by selecting proper scaling factor N of counter.

*freq. Multiplication can also be obtained by using PLL in its harmonic locking mode. If the input signal is rich in harmonics

Ex: Square wave, pulse train etc. Then VCO can be directly locked to n^{th} harmonic of i/p signal without

connecting any freq. divider in between.

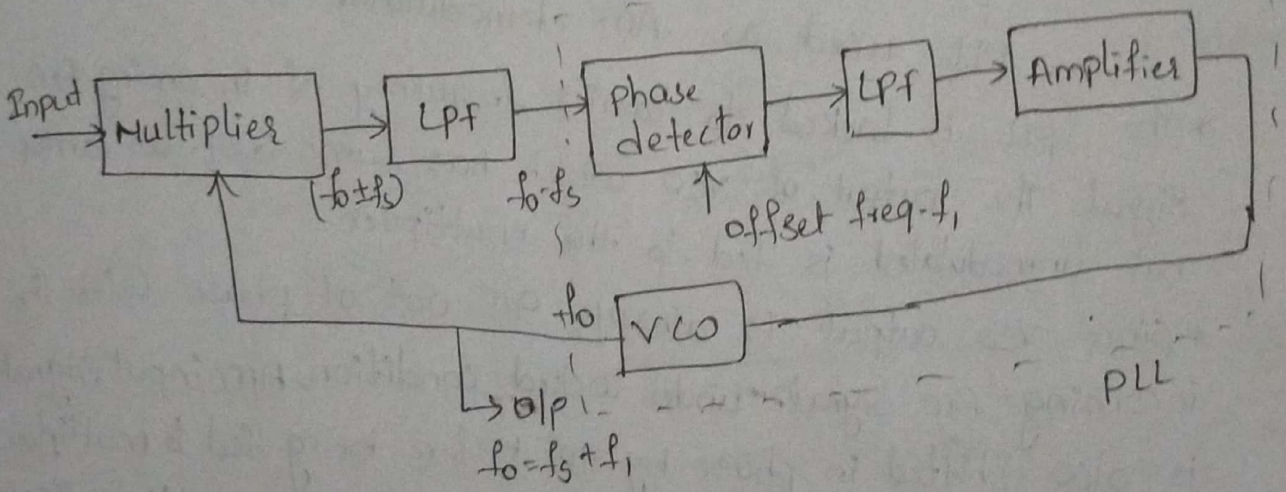
* As amplitude of higher order harmonics becomes less effective locking may not take place for higher values of 'n'. Typically n<10.

* The ckt can be used for freq. division. Since VCO o/p [square wave] is rich in harmonics it is possible to lock mth harmonic of VCO o/p with I/p signal f_s. The o/p f_o of VCO is given by:

$$f_o = \frac{f_s}{m}$$

* Frequency Translation :-

A schematic for shifting the freq. of an oscillator by small factor.



PLL used as frequency divider/Translator.

* A mixer (multiplier) & low pass filter are connected externally to PLL. The signal f_s which has to be shifted and output freq f_o of VCO are applied as inputs to mixer.

* The output of mixer contains the sum and difference of f_s and f_o. However the output of LPF contains only difference signal $(f_o - f_s)$.

* The translation (or) offset frequency ($f_1 << f_s$) is applied to phase comparator. When PLL is in locked state.

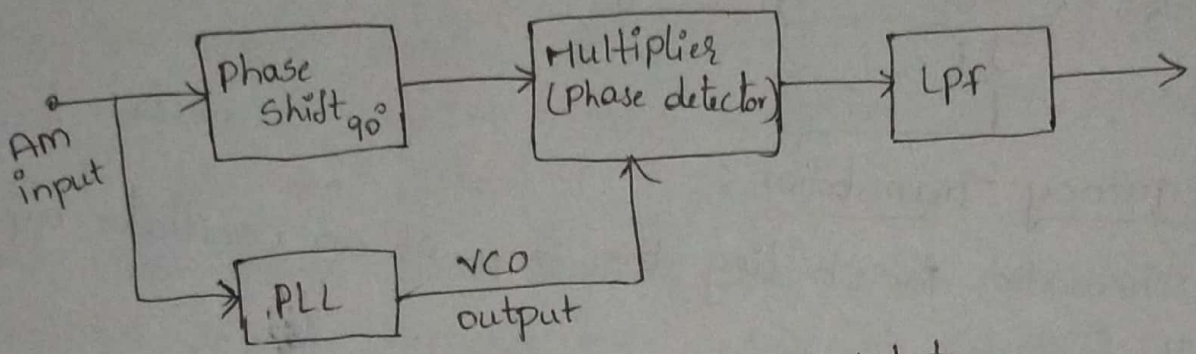
$$f_o - f_s = f_1$$

$$\boxed{f_o = f_s + f_1}$$

It is possible to shift incoming freq. f_s by f_1

(iii) AM Detection:-

A PLL Maybe used to demodulate AM signals.

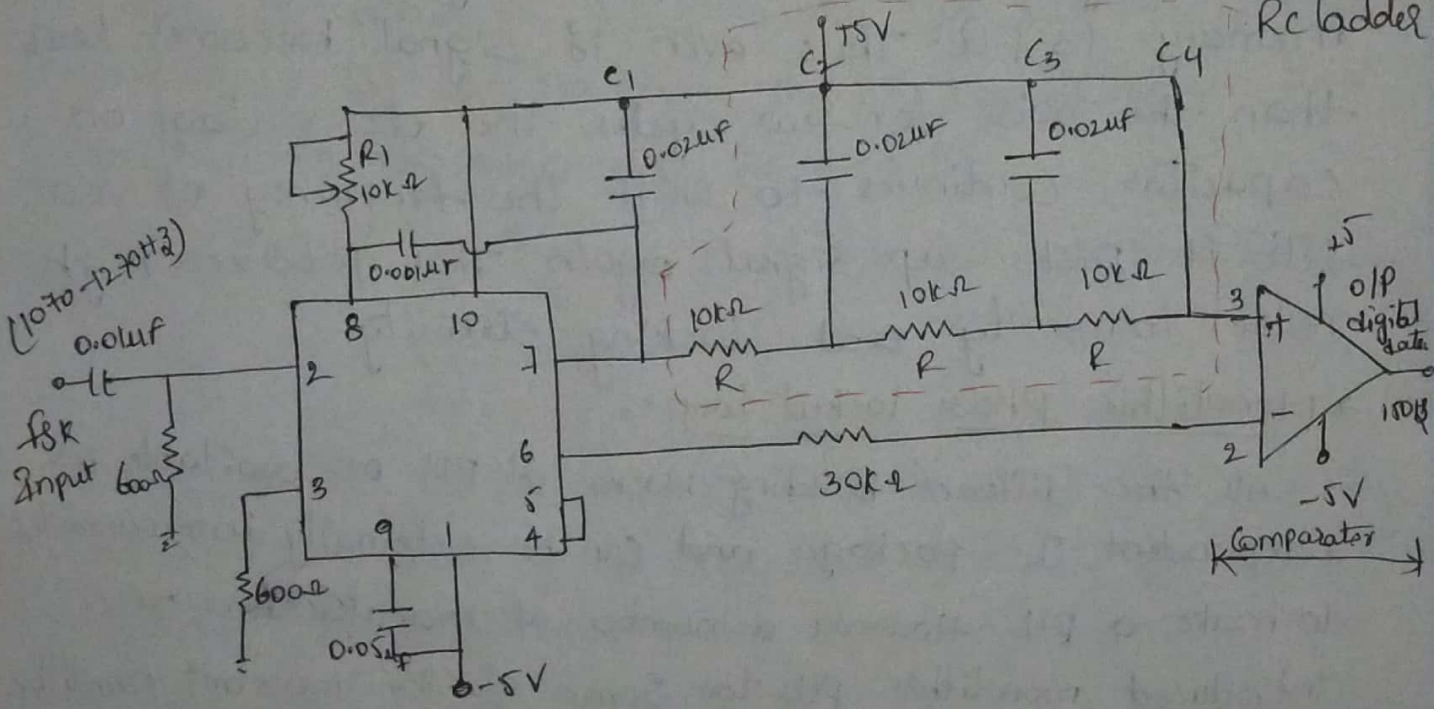


PLL used as AM demodulator.

* The PLL is locked to carrier frequency of incoming AM signal. The output of VCO which has same freq. as carrier but unmodulated is fed to the multiplier.
* Since VCO output is always 90° out of phase with the incoming AM signal under locked condition, AM input signal is also shifted in phase by 90° before being fed to multiplier.
* This makes both the signals applied to the multiplier in same phase. The output of the multiplier contains both the sum and difference signals, the demodulated output is obtained after filtering high freq. components by LPF.
* Since PLL responds only to carrier freq's close to VCO output, PLL AM detector exhibits high degree of selectivity and noise immunity which is not possible with the conventional peak detector type AM modulator.

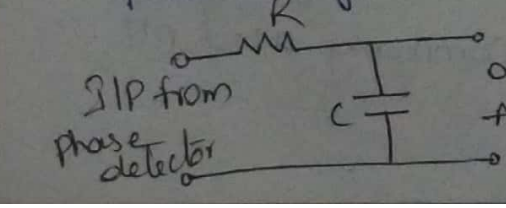
(iv) Frequency shift keying [FSK] Demodulator:-

* In digital data communication and computer peripheral, binary data is transmitted by means of carrier frequency which is shifted between two preset frequencies.
* This type of data transmission is called frequency shift keying (FSK) technique. The binary data can be retrieved using FSK demodulator at receiving end. 565 PLL is very useful as FSK demodulator.
* As the signal appears at input, the loop locks to i/p freq. and tracks it between two frequencies with corresp. dc shift at the output.
* A three stage filter removes the carrier component and output signal is made logic compatible by voltage comparator.

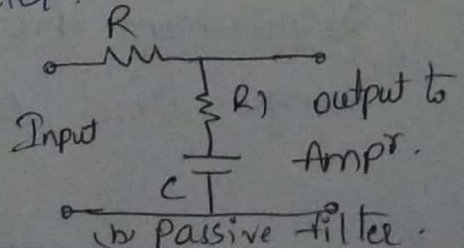


FSK Modulator.

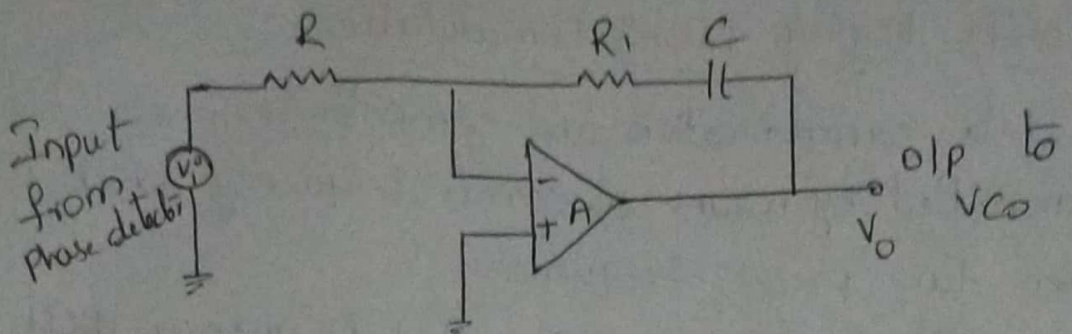
* Low pass filter:- The filter used in PLL may be either passive type or active type of filter.



(a) Low pass filter



(b) Passive filter.



(c) Active filter.

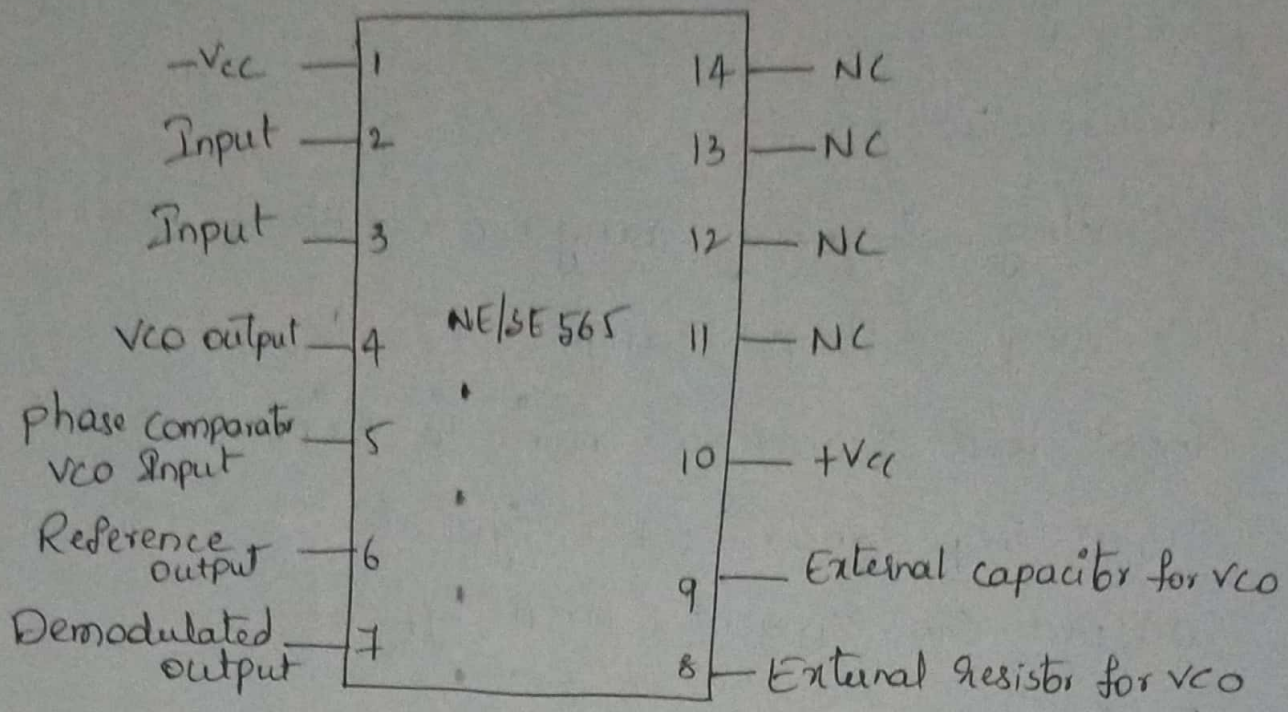
*The low pass filter not only removes the high frequency components and noise, but also controls the dynamic characteristics of PLL. These characteristics include capture and lock range, bandwidth and transient response.

*If filter bandwidth is reduced the response time increases But reducing the bandwidth of the filter also reduces the capture range of the PLL.

*The charge on filter capacitor gives short time memory to PLL. Thus, even if signal becomes less than the noise for few cycles, the dc voltage on capacitor continues to shift the frequency of VCO till it picks up signal again. This produces high noise immunity and locking stability.

*Monolithic phase locked loop:-

All the different building blocks of PLL are available as independent IC packages and can be externally interconnected to make a PLL. However a number of manufacturers have introduced monolithic PLLs too. Some of the important monolithic PLLs are SE/NE 560, 561, 562, 564, 565 and 569 mainly differ in operating frequency range, power supply requirement, frequency and bandwidth adjustment ranges. Since 565 is the most commonly used PLL.



Pin diagram.

565 is available as a 14-pin DIP package and as 10-pin metal can package. The pin configuration and the block diagram are shown in fig.

The output of frequency of the VCO can be rewritten as

$$f_0 = \frac{0.25}{R_T C_T} \text{ Hz}.$$

* The value of R_T is b/w 2kΩ to 20kΩ. The VCO free running frequency is adjusted with R_T & C_T to be at the centre of the input frequency range.
* The phase locked loop is internally broken b/w the VCO output and the phase comparator input.
* A short circuit b/w pin 4 & 5 connects the VCO o/p to the phase comparator so as to compare f_0 with input signal f_s.

A capacitor C is connected b/w pin 7 and pin 10 to make a low pass filter with the integral resistance of 3.6kΩ.

Characteristics:

Operating frequency rang: 0.001 Hz to 500 kHz

Operating voltage range: ±6V to ±12V

Input level: 10mV rms min. to 3V pp max.

Input impedance: 10kΩ typical

Output sink current: 1mA typical

~~Drift~~

Bandwidth adjustment range: ∠±1 to ± 60%.

Triangular wave amplitude: 2.4 V_{pp} at ±6V supply voltage

Square wave amplitude: 5.4 V_{pp} at ±6V supply voltage.

MODULE - IV

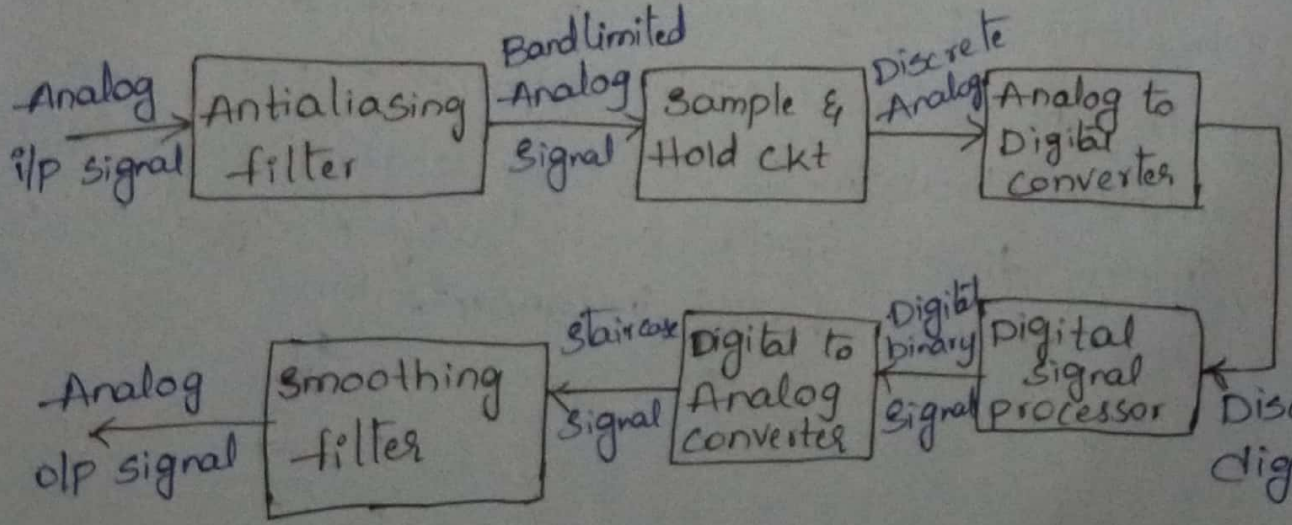
D-A and A-D Converters

Introduction:-

Most of the physical quantities such as voltage, current, temperature, Pressure and time etc. are available in analog form. An analog signal is difficult to process, store or transmit without noise.

* Hence for processing, transmission and storage purposes it is convenient to express in digital form. It gives better accuracy and reduces noise.
* The operation of any digital communication is based upon Analog to digital (A/D) to digital to Analog (D/A) conversion.
* The ckt that perform analog to digital conversion is called Analog to Digital (A/D) converter and circuit that performs digital to Analog (D/A) converter is called digital to Analog (D/A) converter.

ADC - Analog to Digital conversion.
DAC - Digital to Analog conversion.



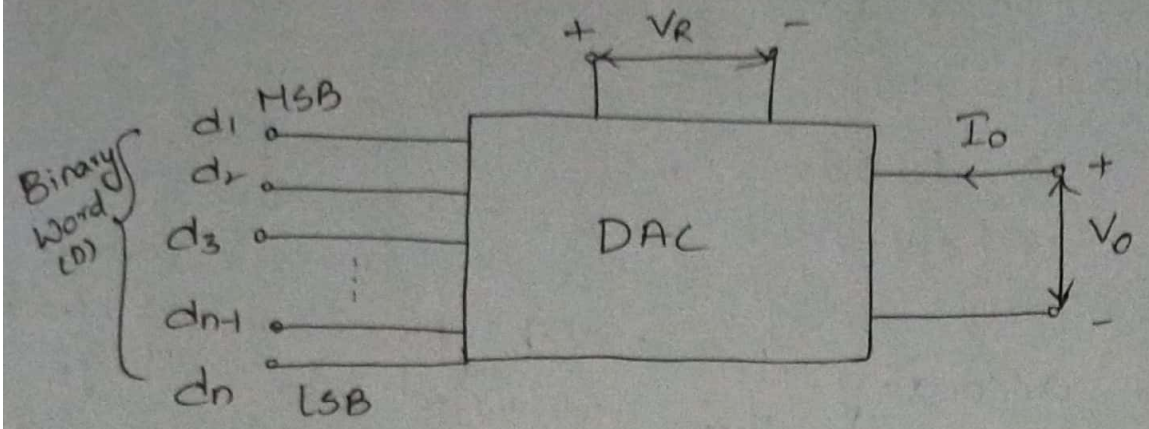
Application with A/D & D/A conversion

* The analog signal obtained from the transducer is bandlimited by the antialiasing filter.
* The signal is then sampled at frequency rate more than twice the max. freq. of bandlimited signal.
* The sampled signal has to be held constant while Conversion is taking place in A/D converter. This requires that ADC should be preceeded by sample and hold (S/H) circuit.
* The ADC output is a sequence in binary digit. The micro computer or digital signal processor performs the numerical calculations of desired control algorithm.
* The D/A converter is to convert the digital signal into analog and function of DAC is opposite to that of ADC. The D/A converter is operated at same freq. as that of ADC.
* The output of D/A converter is a staircase. This staircase like digital output is passed through smoothing filter to reduce the effect of quantization noise.

Applications:- Digital Audio recording, and playback Computer, Music and Video synthesis, Pulse code modulation transmission, data acquistion, digital multimeter, direct digital control, digital signal processing etc. microprocessor based instrumentation.

* ~~Basic~~

* Basic DAC Techniques:-



schematic of DAC

* The DAC (Digital to Analog converter) accepts an n-bit input word in binary form $D \rightarrow d_1, d_2 \ldots d_{n-1}, d_n$ and combined with reference voltage V_R to given an analog output signal.

* The output of DAC can be either voltage or current.

* for voltage output DAC the D/A converter is mathematically described as.

$$V_o = kV_{fs}\left[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}\right]$$

where V_o - output voltage

V_{fs} - full scale output voltage

k - scaling factor adjusted to unity

$d_1, d_2 \ldots d_n$ - n-bit binary fractional word with decimal point located at left.

d_1 - MSB [Most significant bit] with weight of $V_{fs}/2$

d_n - LSB [Least significant bit] with weight of $V_{fs}/2^n$.

* There are three basic DAC Techniques:

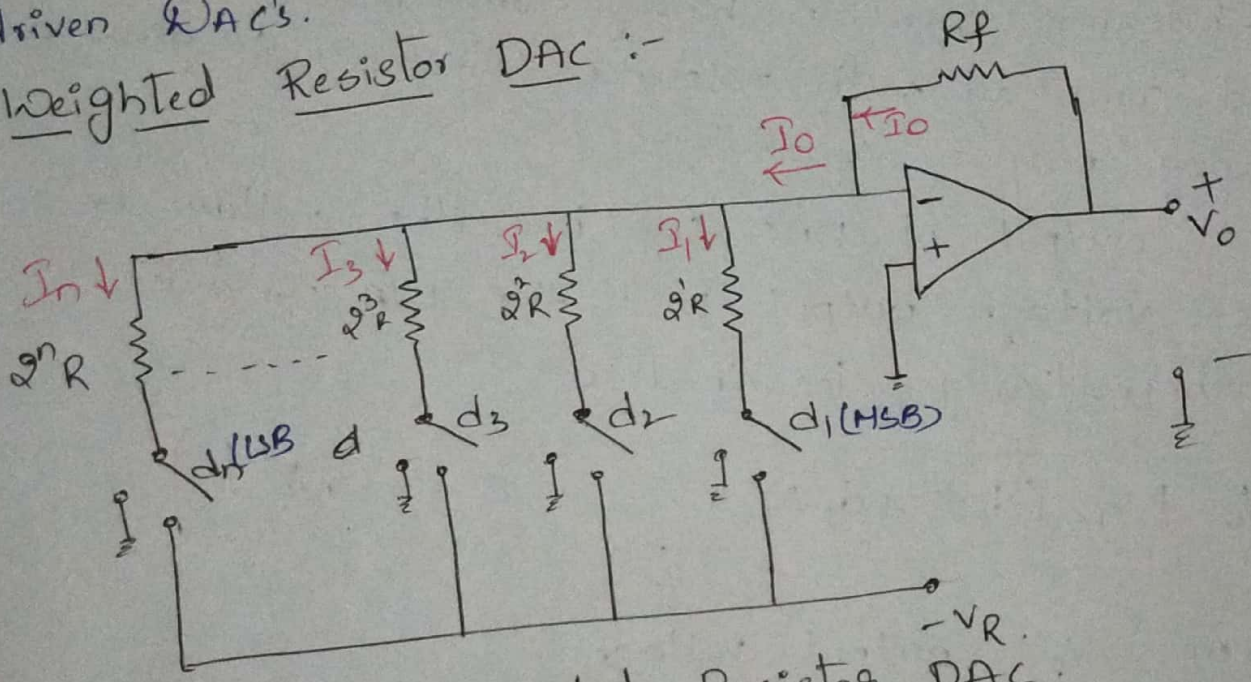
(i) Weighted Resistor DAC.

(ii) R-2R ladder DAC.

(iii) Inverted R-2R ladder DAC.

In these techniques the shunt resistors are used to generate n-binary weighted currents. These currents are added according to switch positions controlled by digital input and then converted into voltage. Such digital to Analog converters are called current driven DAC's.

* Weighted Resistor DAC :-



Binary Weighted Resistor DAC.

* This ckt uses inverting summing amplifier with binary weighted resistor network. It has n-electronic switches $d_1, d_2, d_3 \cdots d_n$ controlled by binary input word.

* This switches are of single-pole-double throw (SPDT) type. If binary (digital) input to particular switch is '1'. It connects the resistance to reference voltage ($-V_R$) and if binary input is '0'.

The switch connects the resistors to ground. (3)

Switch — ON , $I = V_R/R$

Switch - off $I = 0$.

* OP-Amp used as summing amplifier Due to high input resistance of OP-Amp summing current flows through R_f.

The Total [output] current given by:

$$I_0 = I_1 + I_2 + I_3 + \cdots + I_n$$

$$= \frac{V_R}{2R} d_1 + \frac{V_R}{2^2 R} d_2 + \frac{V_R}{2^3 R} d_3 + \cdots + \frac{V_R}{2^n R} d_n$$

$$I_0 = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]$$

output voltage [voltage across R_f] given by

$$V_0 = -I_0 R_f.$$

$$V_0 = -\left[I_1 + I_2 + I_3 + \cdots + I_n\right] R_f$$

$$= -\frac{V_R}{R} \cdot R_f \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]$$

for $R_f = R$ i.e $K = 1$ then

$$V_0 = -V_R \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right]$$

As negative reference voltage used.

$$\boxed{V_0 = V_R \left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}\right].}$$

Here the analog output voltage is proportional to Input digital word.

* the analog output voltage is positive staircase approximation for 3-bit weighted resistor DAC.

$V_0 = V_R [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$

$d_1 d_2 d_3$

001

$V_0 = V_R [0 + 0 + 1 \cdot 2^{-3}]$

$V_0 = \frac{V_R}{8}$

$d_1 d_2 d_3$

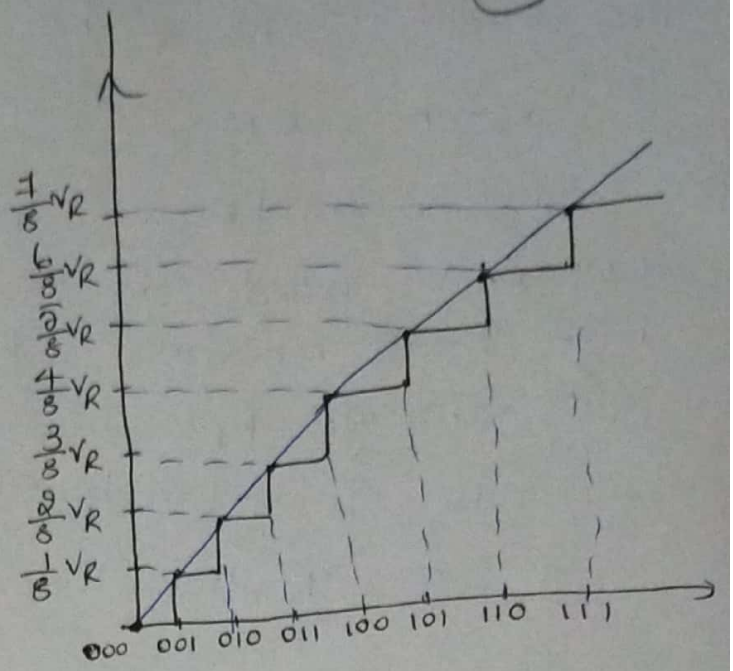
010

$V_0 = V_R [0 + 1 \cdot 2^{-2} + 0] \Rightarrow V_0 = \frac{V_R}{4}$

011

$V_0 = V_R [0 + 1 \cdot 2^{-2} + 1 \cdot 2^{-3}] \Rightarrow V_0 = \frac{V_R}{4} + \frac{V_R}{8}$

$V_0 = \frac{3}{8} V_R.$



$100 \Rightarrow V_0 = V_R [2^{-1} + 0 + 0] \Rightarrow V_0 = \frac{V_R}{2}.$

$101 \Rightarrow V_0 = V_R [2^{-1} + 0 + 2^{-3}] \Rightarrow V_0 = V_R \left[\frac{1}{2} + \frac{1}{8}\right] \Rightarrow V_0 = \frac{5}{8} V_R$

$110 \Rightarrow V_0 = V_R [2^{-1} + 2^{-2} + 0] \Rightarrow V_0 = V_R \left[\frac{1}{2} + \frac{1}{4}\right] \Rightarrow V_0 = \frac{3}{4} V_R$

$111 \Rightarrow V_0 = V_R [2^{-1} + 2^{-2} + 2^{-3}] \Rightarrow V_0 = V_R \left[\frac{1}{2} + \frac{1}{4} + \frac{1}{8}\right] \Rightarrow V_0 = \frac{7}{8} V_R.$

* Although OP-Amp used in inverting mode, it can also be used in non-Inverting mode.
* The OP-Amp works as current-to-voltage converter. The polarity of reference voltage is chosen in accordance with type of switch used.
* for TTL switches reference voltage used as +5V and o/p will be negative.

Drawbacks:-

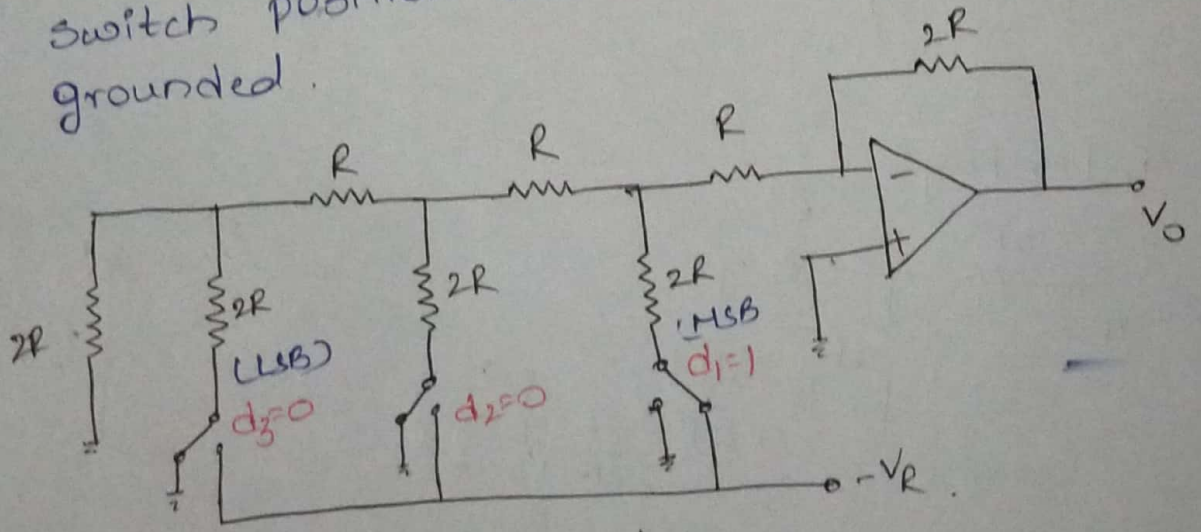
1. Wide range of resistor values are required used for 8-bit DAC the resistors required are $2^0R, 2^1R, 2^2R, \ldots 2^7R$. The largest resistor is 128 times the smallest one.
2. As no. of bits increases range of resistance value also increases.

(ii) It is impracticable to fabricate large values of resistors in IC and voltage drop across large resistor due to bias current also affects the accuracy. for smaller values of resistors, loading effect will occur.

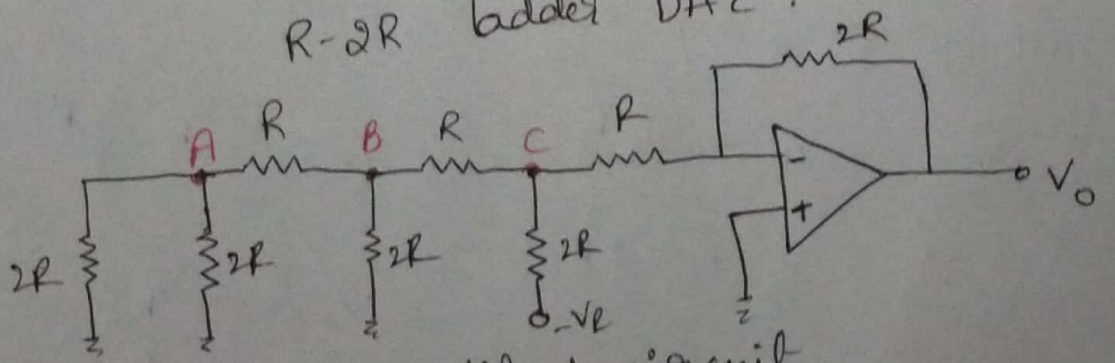
(iii) The finite resistance of switches disturbe the binary weighted relationship among various currents, particularly in most significant bit positions where the current setting resistances are required.

* R-2R ladder DAC :-

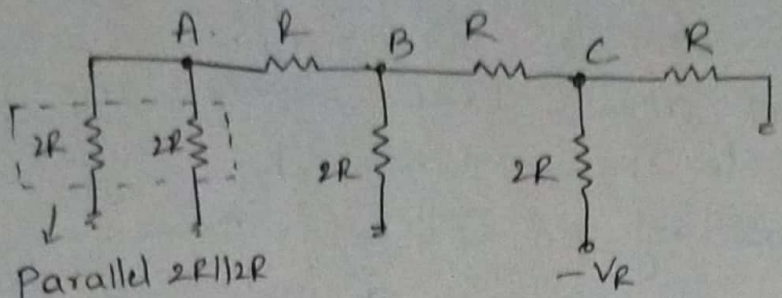
- The wide range of resistors are required in binary weighted resistor type DAC.
- This can be avoided by using R-2R ladder type DAC where only two values of resistors are required.
- This is well suited for IC realization. The typical value of R ranges from 2.5kΩ to 10kΩ. In this type, reference voltage is applied to one of switch position and other switch position is grounded.



R-2R ladder DAC.

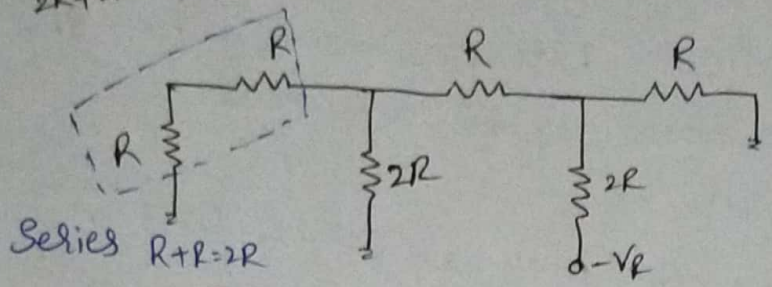


Simplified circuit

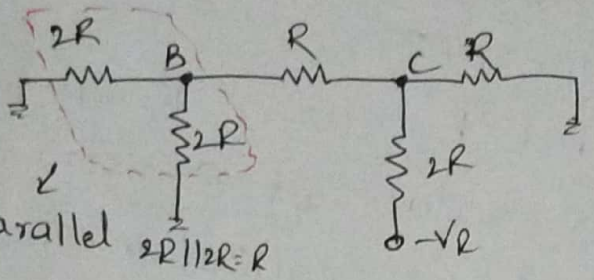


Parallel $2R \| 2R$

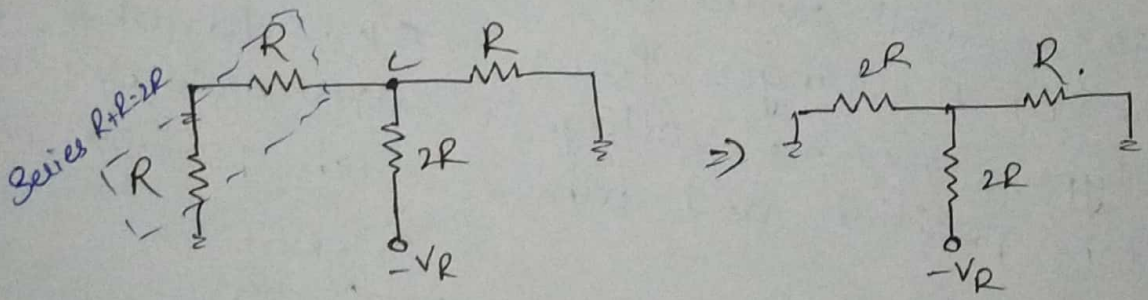
$\frac{2R \times 2R}{2R+2R} = \frac{4R^2}{4R} = R$



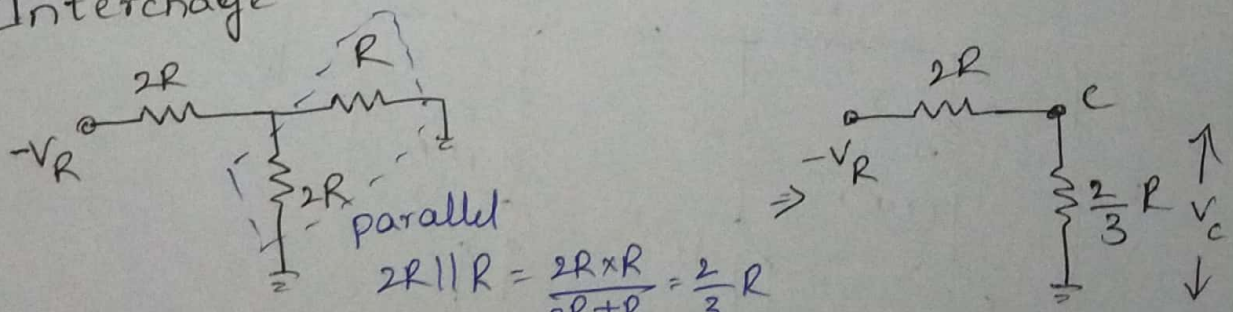
Series $R+R=2R$



Parallel $2R \| 2R = R$



Interchage



Apply ~~po~~ voltage potential divides.

$$V_C = \frac{-V_R \times \frac{2}{3}R}{\frac{2}{3}R + 2R} \Rightarrow V_C = -V_R \times \frac{2}{3}R \times \frac{3}{8R}$$

$$V_C = \frac{-V_R}{4}$$

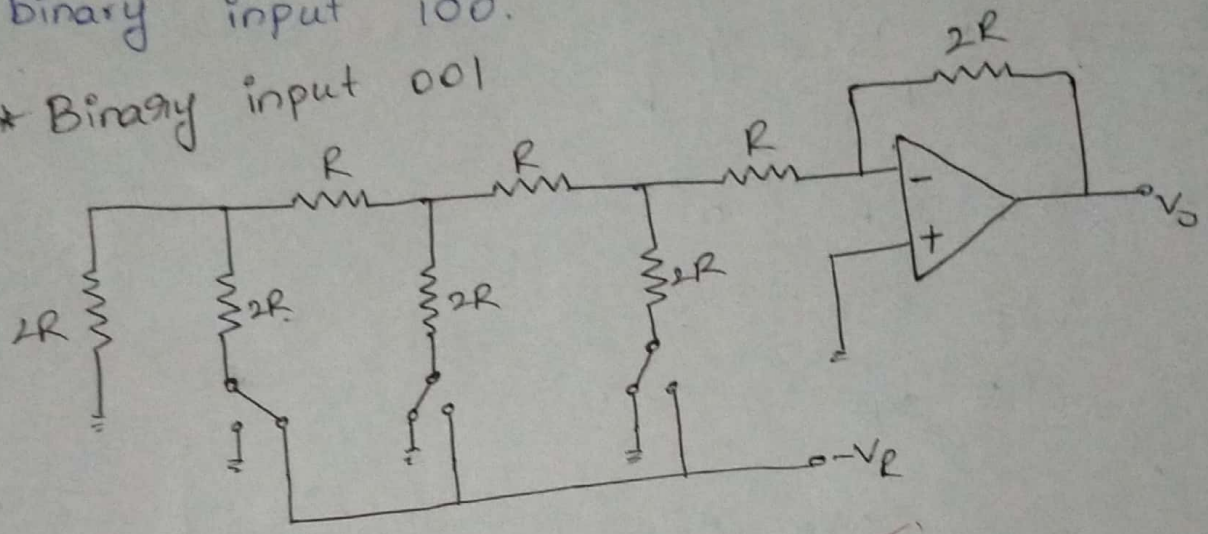
output voltage given by $\left[A = -\frac{R_f}{R}\right]$

$$V_0 = \left[-\frac{2R}{R}\right] V_c$$

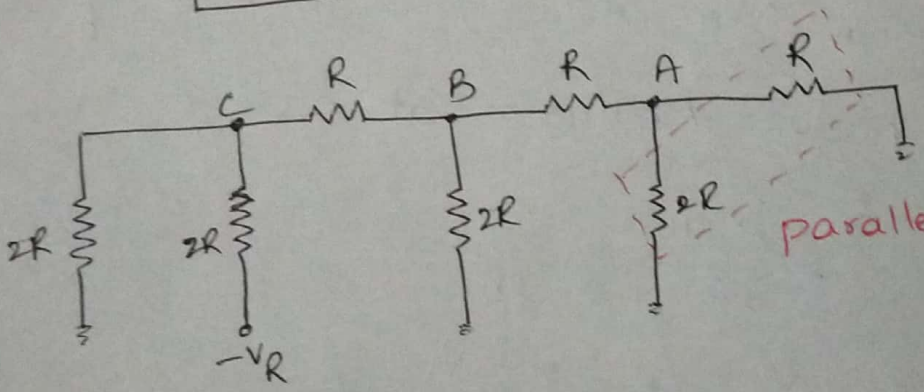
$$V_0 = \left[-\frac{2R}{R}\right]\left[-\frac{V_R}{2}\right] = \frac{V_R}{2} \qquad \boxed{V_0 = \frac{V_{FS}}{2}}$$

Thus output voltage is $\frac{V_R}{2}$ for an equivalent binary input 100.

* Binary input 001

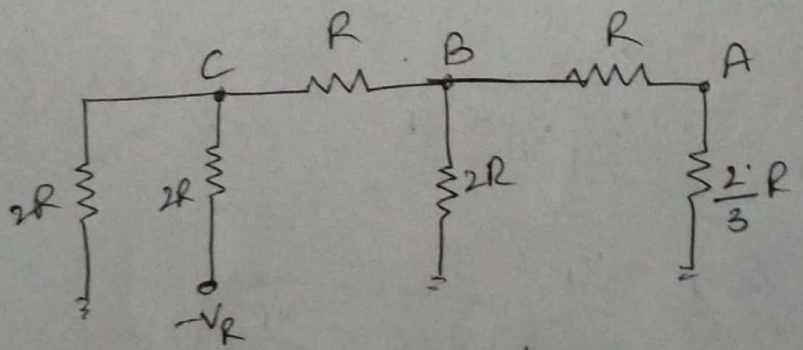


Sol



parallel $2R \| R$

$\frac{2R \times R}{2R+R} = \frac{2}{3}R$



Apply nodal Analysis

At node 'A'

$$\frac{V_A}{\frac{2}{3}R} + \frac{V_A - V_B}{R} = 0$$

$$\frac{3V_A}{2R} + \frac{V_A - V_B}{R} = 0$$

$$3V_A + 2V_A - 2V_B = 0$$

$$5V_A - 2V_B = 0 \Rightarrow 5V_A = 2V_B \Rightarrow \boxed{V_B = \frac{5}{2} V_A}$$

Apply nodal Analysis at node B.

$$\frac{V_B}{2R} + \frac{V_B - V_A}{R} + \frac{V_B - V_C}{R} = 0$$

$$V_B + 2V_B - 2V_A + 2V_B - 2V_C = 0$$

$$5V_B - 2V_A = 2V_C$$

$$5\left[\frac{5}{2}\right] V_A - 2V_A = 2V_C$$

$$25V_A - 4V_A = 4V_C \Rightarrow 21V_A = 4V_C \Rightarrow \boxed{V_C = \frac{21}{4} V_A}$$

Apply nodal Analysis at node C

$$\frac{V_C - V_B}{R} + \frac{V_C - [-V_R]}{2R} + \frac{V_C}{2R} = 0$$

$$2V_C - 2V_B + V_C + V_R + V_C = 0$$

$$4V_C - 2V_B + V_R = 0$$

$$4\left[\frac{21}{4}\right] V_A - 2\left[\frac{5}{2}\right] V_A + V_R = 0$$

$$21V_A - 5V_A + V_R = 0$$

$$16V_A + V_R = 0 \Rightarrow \boxed{V_A = \frac{-V_R}{16}}$$

voltage gain of Inverting Amplifier.

$$A = \frac{V_o}{V_i} = \frac{-R_f}{R}.$$

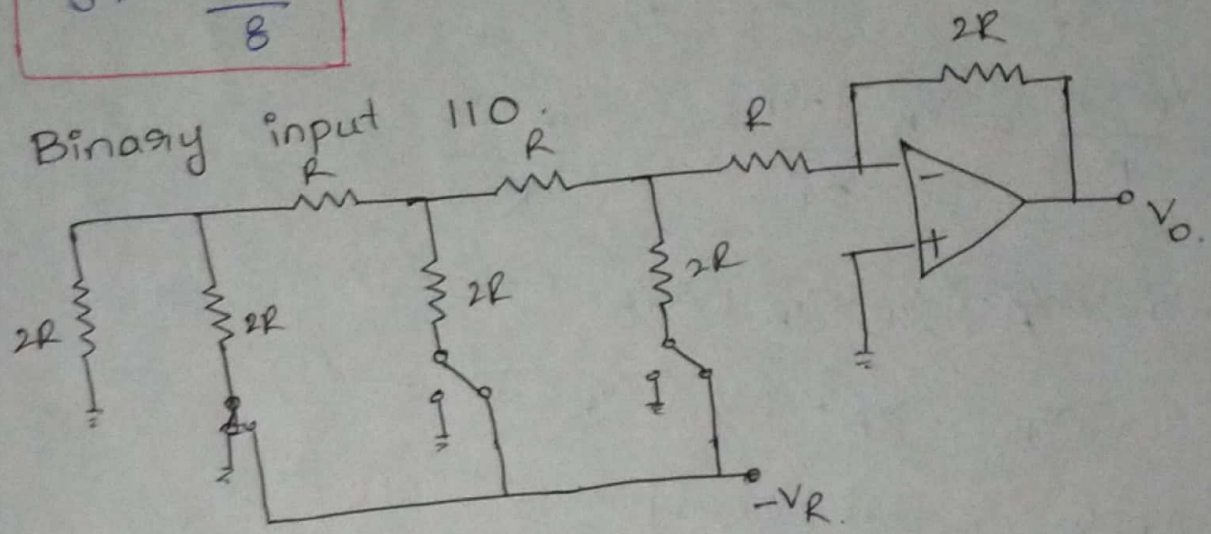
$$V_o = -\frac{R_f}{R} V_A .$$

$$[R_f = 2R]$$

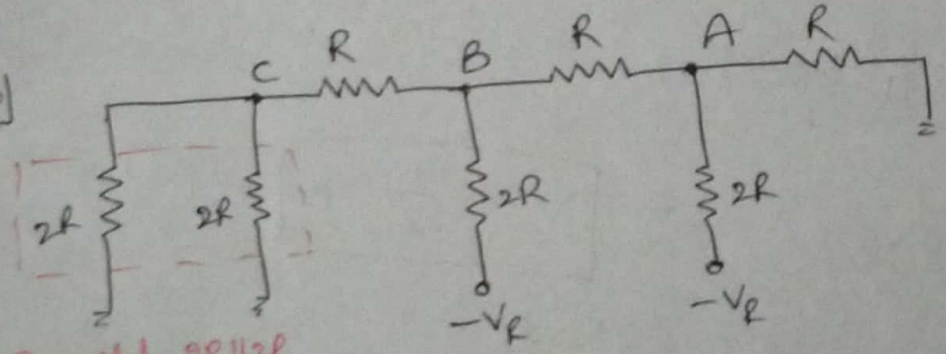
$$V_o = \frac{8R}{R} \times \frac{[-V_R]}{16}$$

$$\boxed{V_o = \frac{V_R}{8}}$$

* Binary input 110.

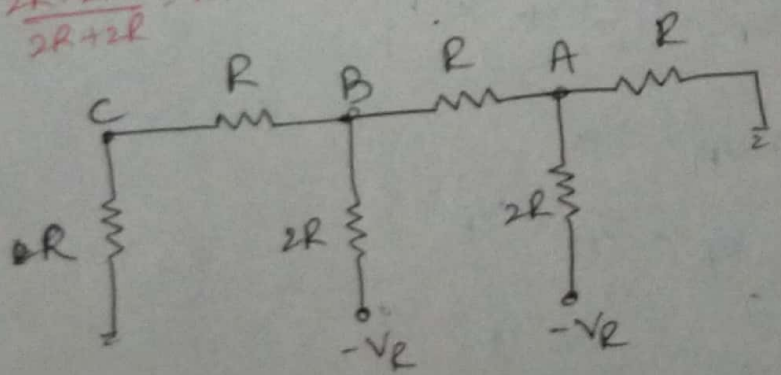


Sol:



Parallel $8R \| 2R$

$$\frac{2R \times 2R}{2R + 2R} = R.$$



Apply nodal Analysis at node A

$$\frac{V_A}{R} + \frac{V_A + V_R}{2R} + \frac{V_A - V_B}{R} = 0$$

$$2V_A + V_A + V_R + 2V_A - 2V_B = 0$$

$$5V_A - 2V_B + V_R = 0$$

$$V_R = 2V_A - 5V_B \quad \text{— (1)}$$

Apply nodal Analysis at node B

$$\frac{V_B - V_A}{R} + \frac{V_B - [-V_R]}{2R} + \frac{V_B - V_C}{R} = 0$$

$$2V_B - 2V_A + V_B + V_R + 2V_B - 2V_C = 0$$

$$5V_B - 2V_A - 2V_C + V_R = 0 \quad \text{— (2)}$$

Apply nodal Analysis at node C

$$\frac{V_C - V_B}{R} + \frac{V_C}{R} = 0$$

$$2V_C - V_B = 0 \Rightarrow \boxed{V_C = \frac{1}{2} V_B} \quad \text{— (3)}$$

Sub. V_C in Eqn 2,

$$5V_B - 2V_A - 2\left(\frac{1}{2}\right)V_B + V_R = 0$$

~~$10V_B - 4V_A - V_B$~~

$$5V_B - 2V_A - V_B + V_R = 0.$$

$$4V_B - 2V_A + V_R = 0 \quad \text{— (4)}$$

Sub. Eqn 1, in Eqn 4.

~~$5V_B$~~ $4V_B - 2V_A + 2V_A - 5V_B = 0$

$$6V_B - 7V_A = 0 \Rightarrow \boxed{V_B = \frac{7}{6} V_A}$$

Sub. V_B in Eqn (1),

$$V_R = 2V_B - 5V_A$$

$$V_R = 2\left[\frac{7}{8}\right]V_A - 5V_A$$

$$V_R = \frac{7V_A - 15V_A}{3}$$

$$V_R = -\frac{8}{3}V_A \Rightarrow \boxed{V_A = -\frac{3}{8}V_R}$$

Voltage gain of Inverting Amplifier

$$A = \frac{V_o}{V_i} = -\frac{R_f}{R}$$

$$V_o = -\frac{R_f}{R} \times V_A$$

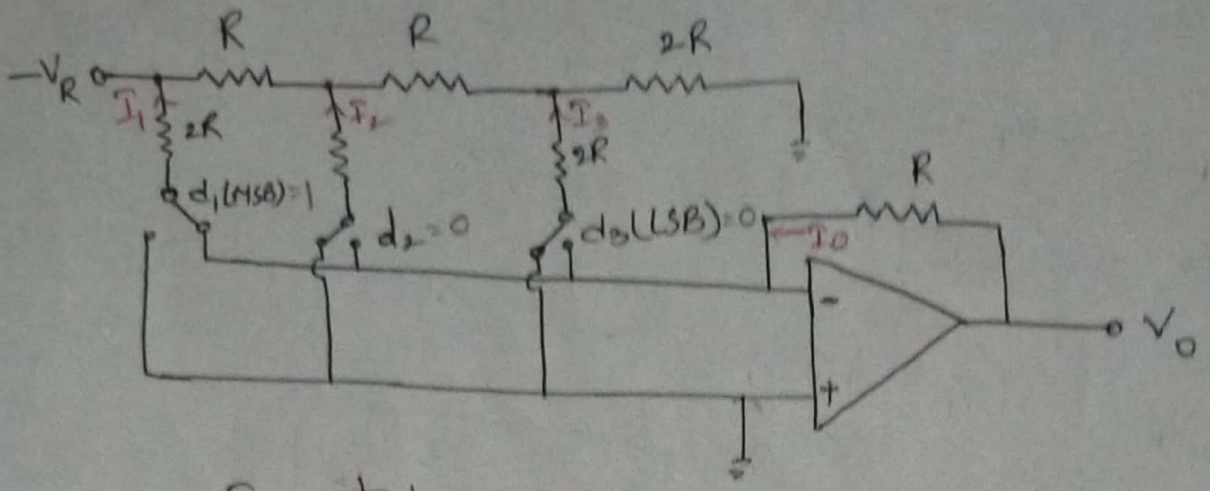
$$V_o = -\frac{2R}{R} \times \left[\frac{-3}{8}\right]V_R \quad [\because R_f = 2R]$$

$$\boxed{V_o = \frac{3}{4}V_R}$$

(iii) Inverted R-2R Ladder:-

In weighted Resistor type DAC and R-2R ladder type DAC, current flowing in the resistors changes as input data changes. The excess power dissipation causes heating causing and non-linearity in DAC.

* This problem can be avoided completely in inverted R-2R ladder type DAC.



Inverted R-2R ladder DAC.

A 3-bit Inverted ladder type DAC is shown in fig. where the position of MSB and LSB is interchanged. Here each input binary word connects the corresponding switch either input bit to ground or to the inverting input terminal of the op-Amp which is also at virtual ground. since both the terminals of switch d_i are at ground potential. current flowing in the resistances is constant and independent of switch position.

$$I_1 = \frac{V_R}{2R}, \quad I_2 = \frac{\frac{V_R}{2}}{2R} = \frac{V_R}{4R}, \quad I_3 = \frac{V_R}{4}\Big|_{2R} = \frac{V_R}{8R}$$

$$I_T = I_1 + I_2 + I_3$$

$$I_T = d_1 \frac{V_R}{2R} + d_2 \frac{V_R}{4R} + d_3 \frac{V_R}{8R}$$

$$I_T = \frac{V_R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

$$I_T = \frac{V_0 - 0}{R_f} \Rightarrow V_0 = I_T R_f$$

$$V_0 = V_R \cdot \frac{R_f}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right]$$

$$V_0 = V_R \cdot \frac{R}{R}\left[d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}\right] \quad [\because R_f = R]$$

$$V_o = V_R [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3}]$$

In general

$$V_o = V_R \frac{R_f}{R} [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}]$$

* The basic step of a 9-bit DAC is 10.3mv. If 000000000 represents 0v, what hap. output is produced if the input is 101101111 ?

The output voltage for input 101101111 is

$$V_o = V_R \cdot \frac{R_f}{R} [d_1 2^{-1} + d_2 2^{-2} + d_3 2^{-3} + \cdots + d_n 2^{-n}]$$

$$V_o = 10.3mv [1\times2^8 + 0\times2^7 + 1\times2^6 + 1\times2^5 + 0\times2^4 + 1\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0]$$

$$= 3.78\ V.$$

* Calculate the values of the LSB, MSB and full scale output for an 8-bit DAC for the 0 to 10 v range.

Sol $\quad LSB = \frac{10V}{2^8} = 39mV$

$$MSB = \frac{10}{2} = 5V$$

full scale output = full scale voltage − LSB

$$= 10V - 39mV = 9.961V.$$

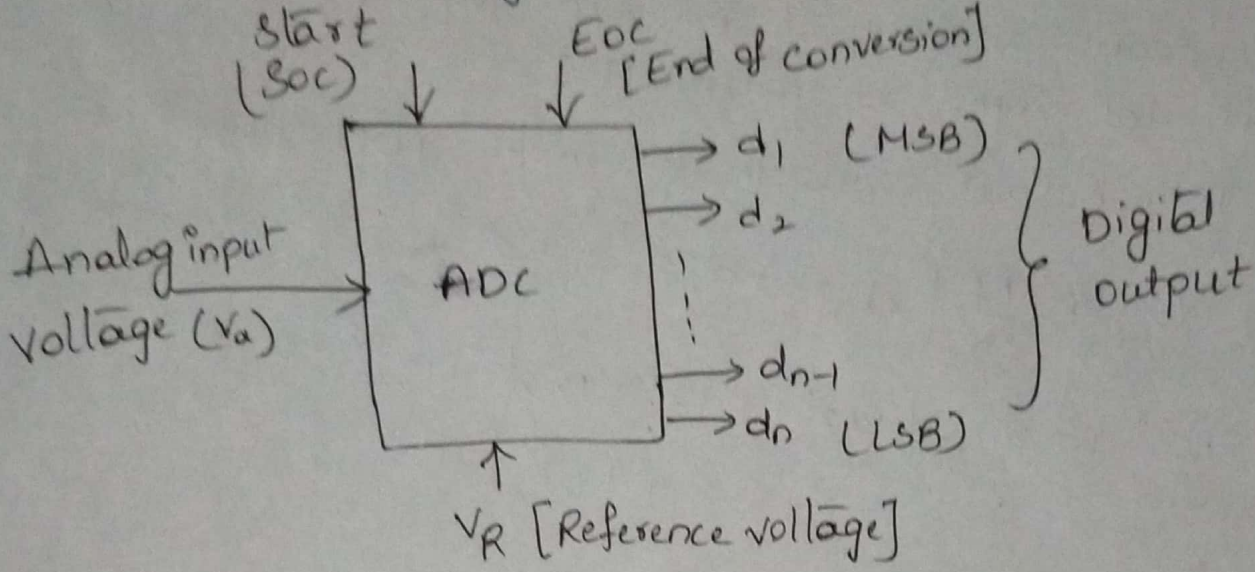
* A-D Converters :-

The function of ADC [Analog to Digital converter] is just opposite to that of DAC. It accepts analog input voltage V_a and produces an output binary word (D).

$d_1\ d_2 \cdots d_{n-1}\ d_n$

$$D = d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}$$

where d_1 - Most significant Bit.
and d_n - Least significant Bit



Schematic of ADC.

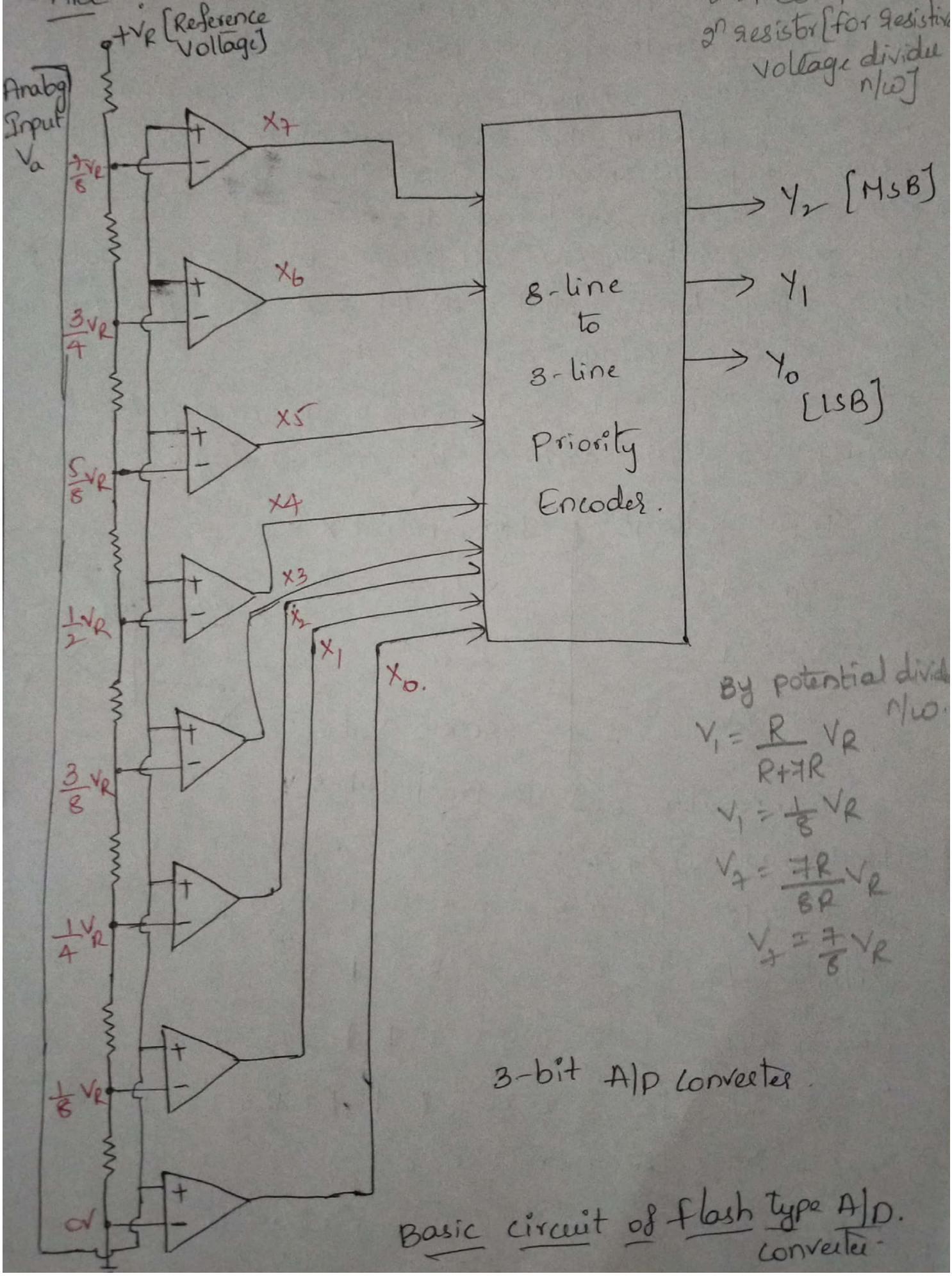
* An ADC usually has two additional control lines the Soc [start of conversion] START input to tell the ADC when to start the conversion and EOC [End of conversion] output to announce when the conversion is complete.
* Depending on type of application, ADCs are designed for microprocessor interfacing (or) to directly drive LCD or LED display.
* classification:-

The various ADC techniques are as follows:

(i) flash [comparator] type ADC.
(ii) Counter type ADC.
(iii) Successive Approximation type ADC.
(iv) Dual - slope ADC.

*flash (comparator) type ADC (or) parallel comparator type ADC :-

$2^n - 1$ comparator
2^n resistor [for resistive voltage divider n/w]



By potential divider n/w.

$V_1 = \frac{R}{R+7R} V_R$

$V_1 = \frac{1}{8} V_R$

$V_7 = \frac{7R}{8R} V_R$

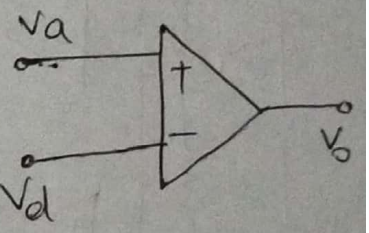
$V_7 = \frac{7}{8} V_R$

3-bit A/D converter.

Basic circuit of flash type A/D converter.

* This is the simplest possible A/D converter. It is the fatest and most expensive technique. The circuit consists of resistive divider network, & op-Amp comparators and 8-line to 3-line encoder [3-bit priority Encoder]
* A small amount of hysteresis is built into comparator to resolve any problem that might occur if both inputs are of equal voltage as shown in truth table.
* At each node of resistive divider network a comparison voltage is available since all resistors are of equal valued. the voltage levels available at the node are equally divided blw reference voltage and ground.
* The purpose of ckt is to compare the analog input voltage V_a with each of the node voltages.

Input voltage	logic output x
$V_a > V_d$	x = 1
$V_a < V_d$	x = 0
$V_a = V_d$	previous value



Comparator and its truth table.

Input voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
0 to $V_R/8$	0	0	0	0	0	0	0	1	0	0	0
$V_R/8$ to $V_R/4$	0	0	0	0	0	0	1	ϕ	0	0	1
$V_R/4$ to $3V_R/8$	0	0	0	0	0	1	ϕ	ϕ	0	1	0
$3V_R/8$ to $V_R/2$	0	0	0	0	1	ϕ	ϕ	ϕ	0	1	1
$V_R/2$ to $5V_R/8$	0	0	0	1	1	1	1	1	1	0	0
$5V_R/8$ to $3V_R/4$	0	0	1	1	1	1	1	1	1	0	1

Input Voltage (V_a)	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	Y_2	Y_1	Y_0
$3V_R/4$ to $7V_R/8$	0	1	1	1	1	1	1	1	1	1	0
$7V_R/8$ to V_R	1	1	1	1	1	1	1	1	1	1	1

Truth Table for flash type A/D Converter.

*Advantages:-

*It has high speed as conversion take place simultaneously rather than sequentially. Typically conversion time is 100ns or less.

*Disadvantages:-

* The no. of comparators required doubles for each added bit.

Ex:- A 2-bit ADC requires 3 comparators.

3-bit ADC needs 7 comparator and 4-bit ADC needs 15 comparators.

* The number of comparators required are $2^n - 1$ where $n \rightarrow$ no. of bits.

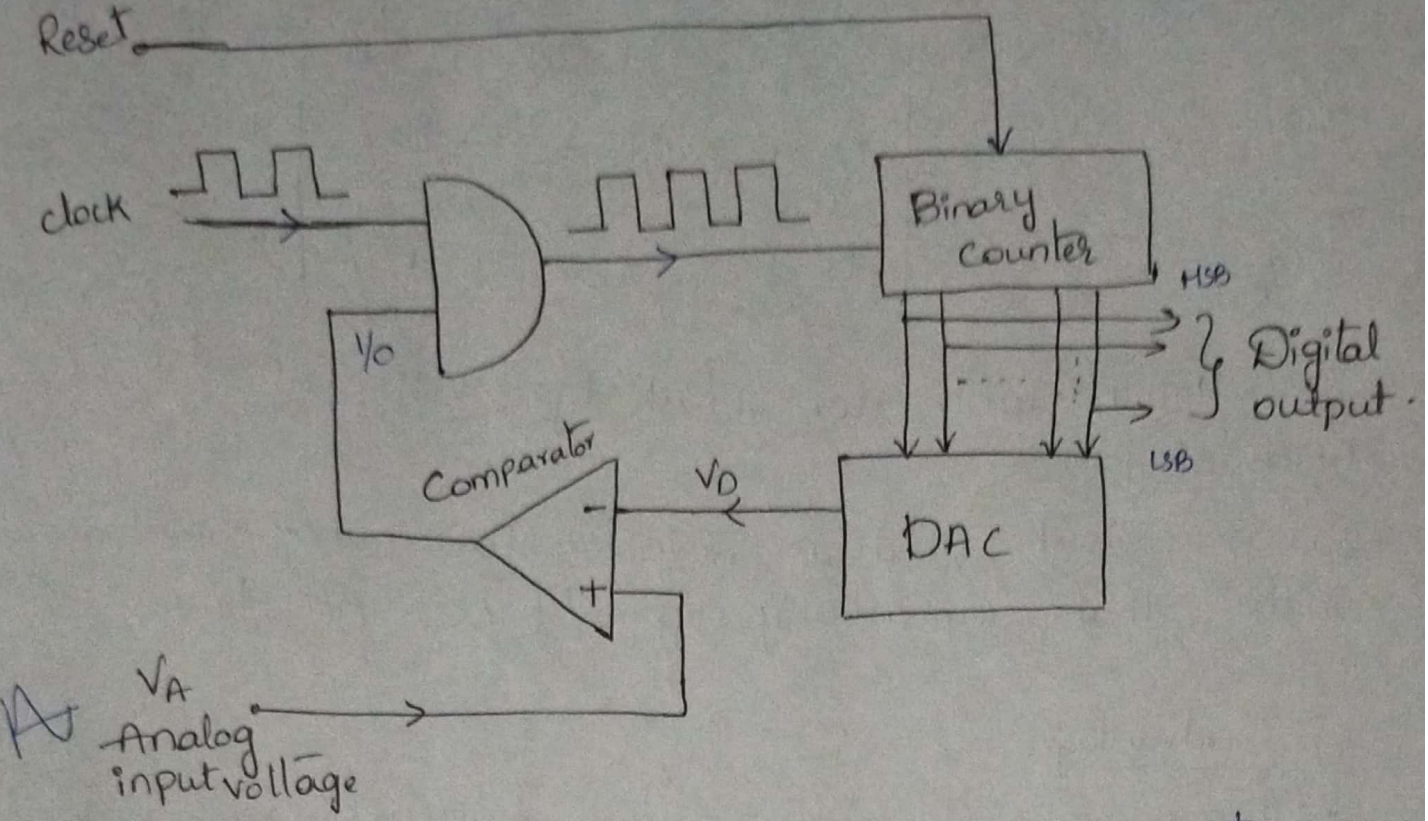
* Larger the value of 'n' more complex is the priority Encoder.

* Counter type ADC :-

The ADC uses DAC for Analog to Digital conversion. The output of DAC is continuously compared with the Analog input which is to be converted into digital output.

Principle:-

The DAC's input code is adjusted until DAC's output comes within $\pm\left[\frac{1}{2}\right]$ LSB to analog input V_a which is converted to binary digital form.

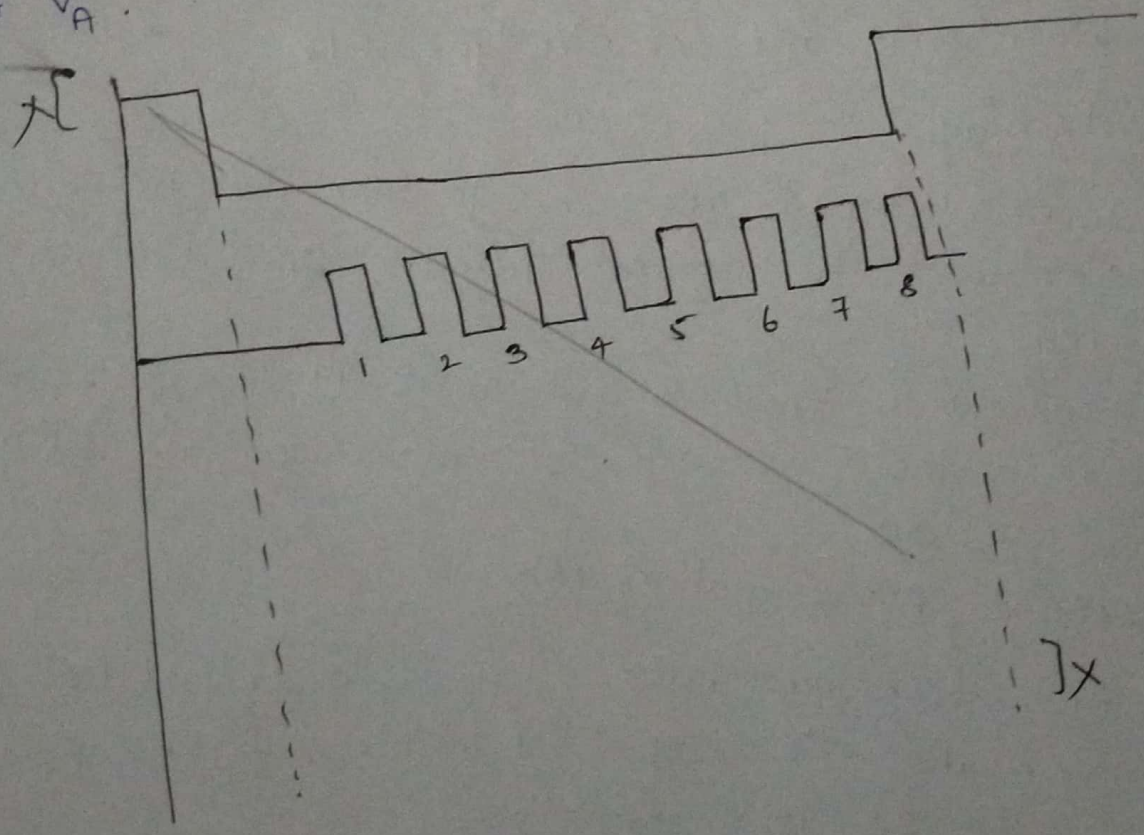


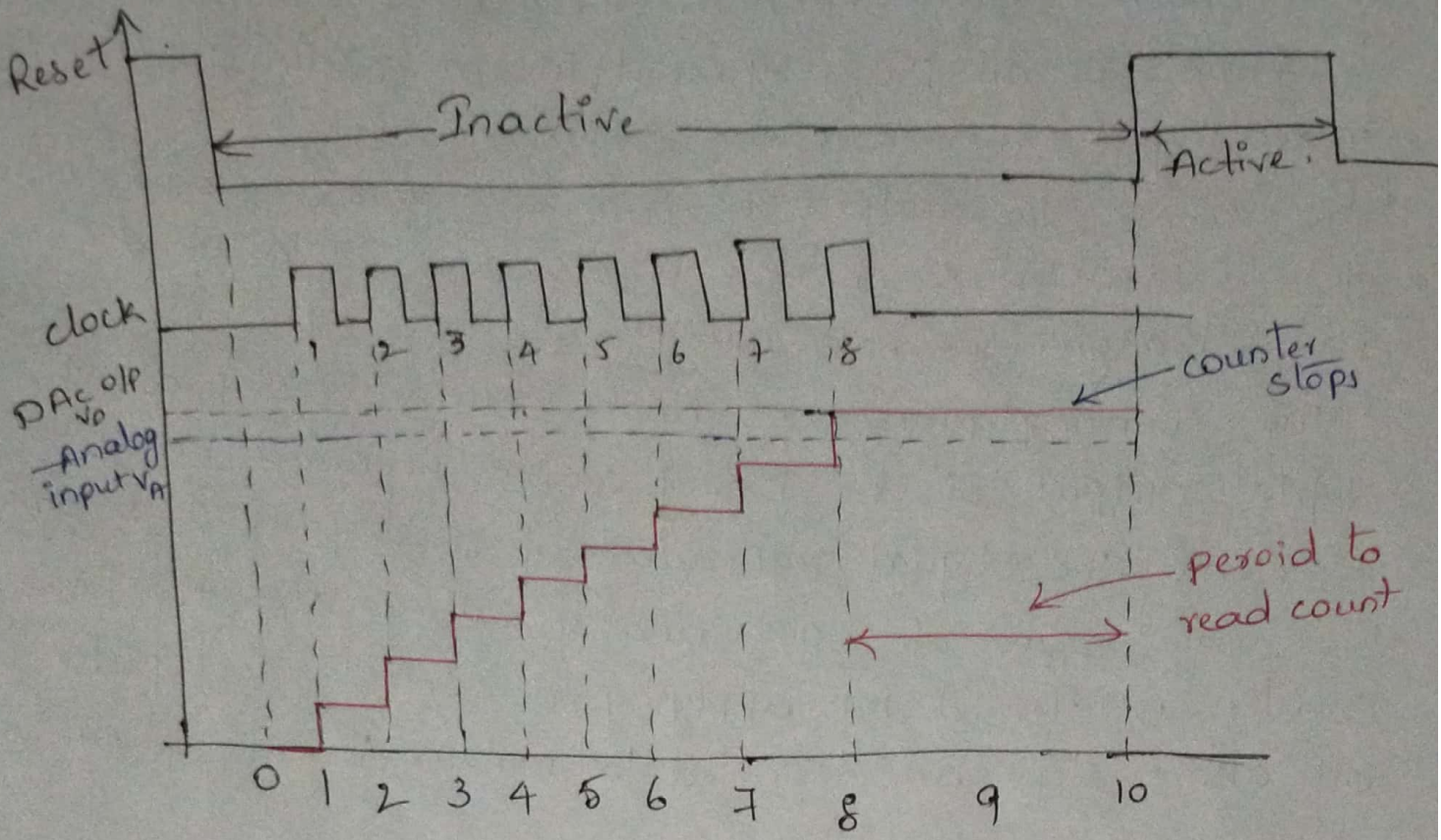
Counter type ADC consists of binary counter, DAC, comparator and AND gate.

* Operation :-

- Initially the counter is reset i.e its output is set to zero by applying a reset pulse.
- The output of counter is given as digital input to DAC. Since input to DAC is zero. its output V_D is zero.
- When analog input voltage V_A is applied to comparator it becomes greater than V_D. The Analog output V_d of DAC is been compared with the analog input V_a by the comparator.
- for $V_A > V_D$ the output of comparator goes high. for AND gate one input is clock pulses and another input is output of comparator. Due to high output of comparator, AND gate enabled and allows the transmission of clock pulses to counter.

* The counter starts counting these clock pulses According to number of clk pulses, the output of counter goes on increasing. this increases the output of DAC.
* for $V_A < V_D$ the output of comparator goes low and AND gate is disabled. so the clk pulses are not allowed to pass through the AND gate.
* The counting process of binary counter is stopped. The digital output of the binary counter is noted which represents the digital equivalent of analog input voltage V_A.
* for new value of input analog voltage V_A. the binary counter is cleared by applying a second reset pulse and all above steps are repeated to obtain the digital equivalent of V_A.





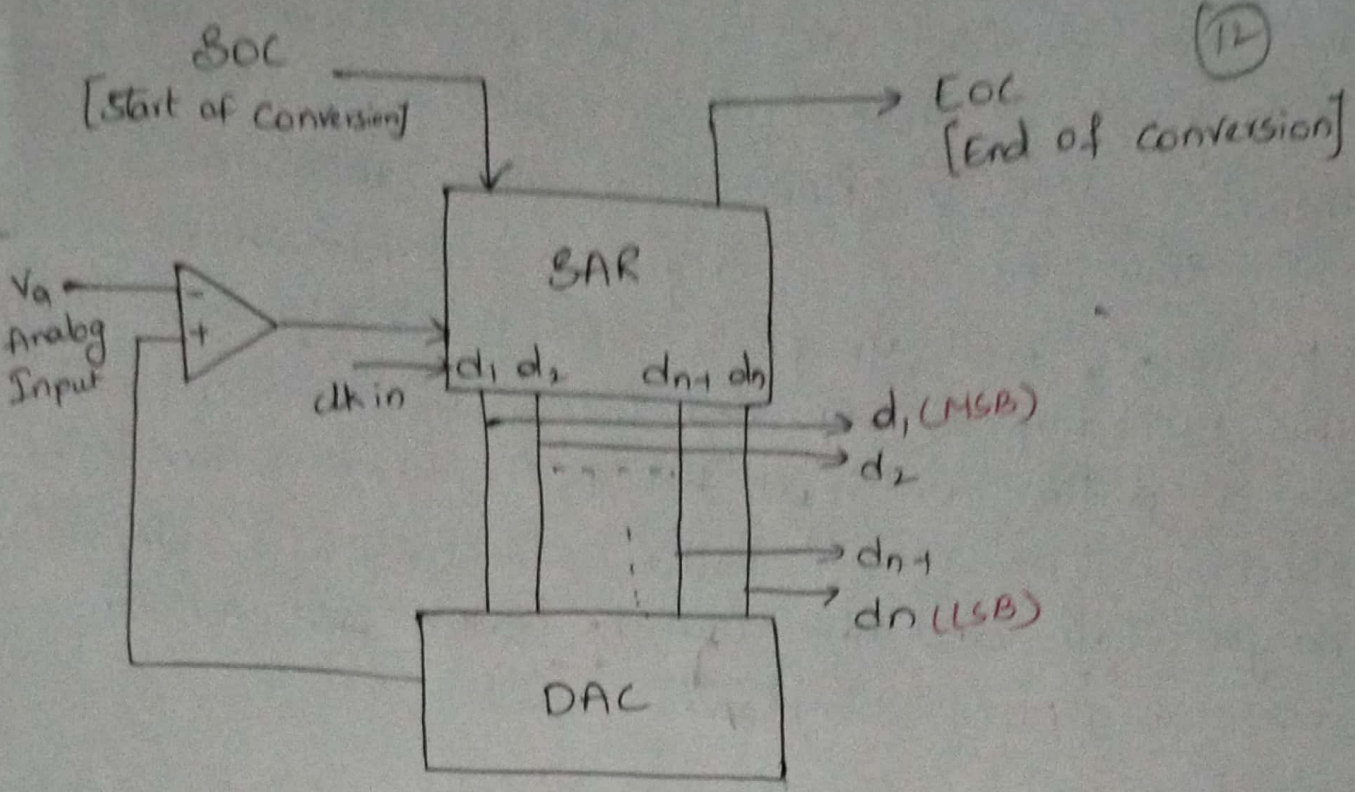
Waveforms for counter type ADC

* Disadvantages:-

* It is necessary to give enough time for DAC conversion and comparator to respond. There is limitation on clk frequency.
* The conversion time is not count. It increases with increase in input voltage. The conversion time is high at high i/p voltage.

* Successive Approximation ADC :-

* In this technique basic idea is to adjust DAC's input code such that its output is within $\pm \frac{1}{2}$ LSB of analog input V_i to be A/D converted.
* The code that achieves this represents the desired ADC output. This is very efficient code search stralegy used to complete n-bit conversion in just n-clk periods. An 8-bit converter would require eight clock pulses to obtain a digital output.



Block Diagram.

*The block diagram of successive approximation A/D converter consists of DAC, comparator and successive Approximation Register [SAR].

*The external clock input sets the internal timing parameters. The control signal start of conversion [SOC] initiates an A/D conversion process and end of conversion [EOC] signal activated when the conversion is completed.

* The SAR is used to find the required value of each bit by trial and error.

Operation :-

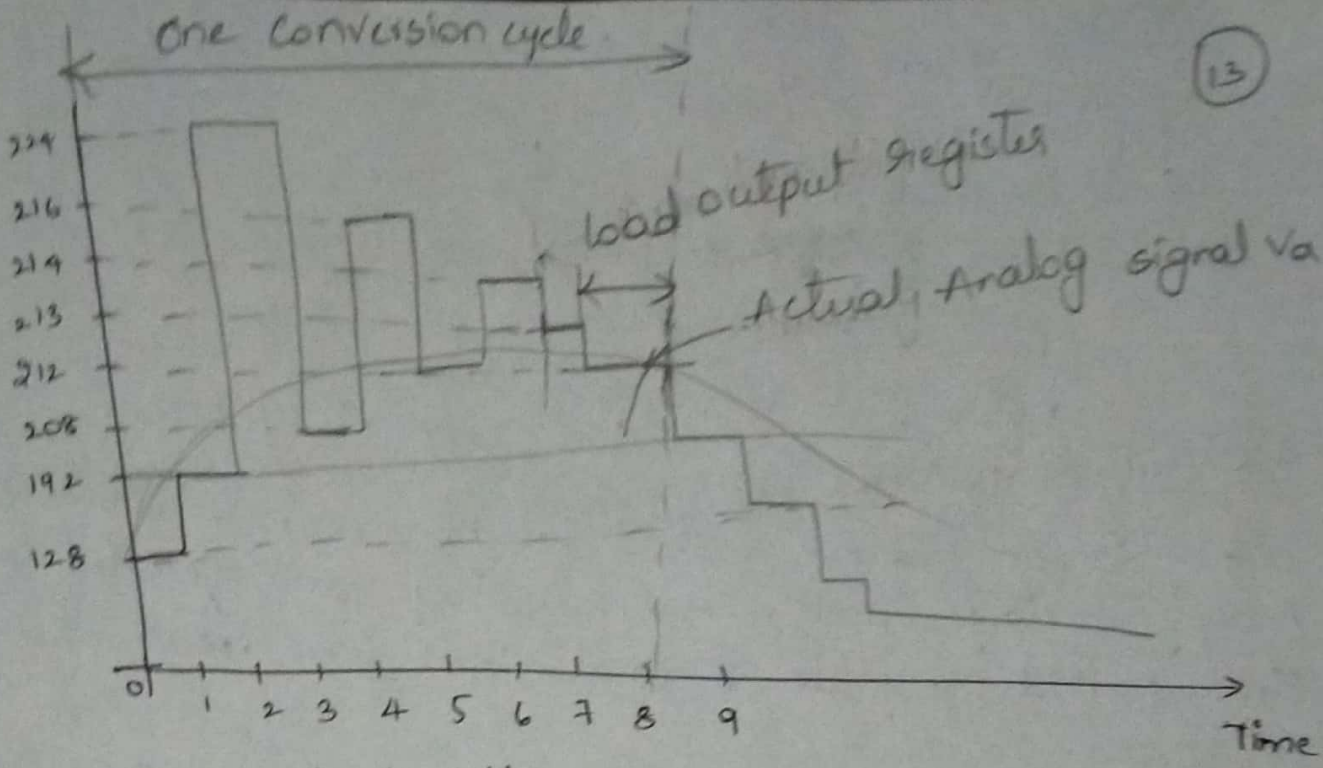
. With the arrival of start of conversion [SOC] command the SAR sets the MSB [d_1=1] with all other bits to zero. so that trial code is 10000000.

. The output Vd of DAC is now compared with Analog input V_a. If $V_a > V_d$ [DAC] output then 10000000 is less than the correct digital representation.

* The MSB is left at '1' and next lower significant bit is made '1' and further tested.
* However if $V_a < (DAC\ o/p)\ V_d$ then 10000000 is greater than the correct digital representation so reset MSB to '0' and go on to next lower significant bit.
* This procedure is repeated for all subsequent bits, one at a time until all bit positions have been tested.
* Whenever DAC output (V_d) crosses V_a, the comparator changes state and this can be taken as end of conversion [EOC] command.

Correct digital Representation.	successive approximation register output V_d at different stage in conversion		Comparator output.
11010100	10000000 : 128	$V_a > V_d \rightarrow o/p \rightarrow 1$ $V_a < V_d \rightarrow o/p \rightarrow 0$	1 [Inital o/p]
	11000000 : 192		1
	11100000 : 224		0
	11010000 : 208		1
	11011000 : 216		0
	11010100 : 212		1
	11010110 : 214		0
	11010101 : 213		0
	11010100 : 212		

Successive Approximation conversion sequence for typical Analog input.



D/A output voltage seen to become successively closer to actual Analog input voltage.

- The D/A output voltage becomes successively closer to actual Analog input voltage It requires eight pos'clk pulses to establish the accurate output regardless of value of analog input.
- one analog
- one additional clk pulse is used to load the output (regardless of value of analog input register and reinitialize the ckt).
- This is more versatile - and superior compared to all other ckts.

AD 7592 - 28 pin DIP CMOS package
12-bit A/D converter using successive Approximation technique.

- one clk pulse is required for SAR to compare each bit. An additional clk pulse required to reset the register prior to conversion.
- The time for one analog to digital conversion must depend on both clk's period (T) and no. of bits (n)

It is given by

$$T_c = T(n+1)$$

where T_c - Conversion Time

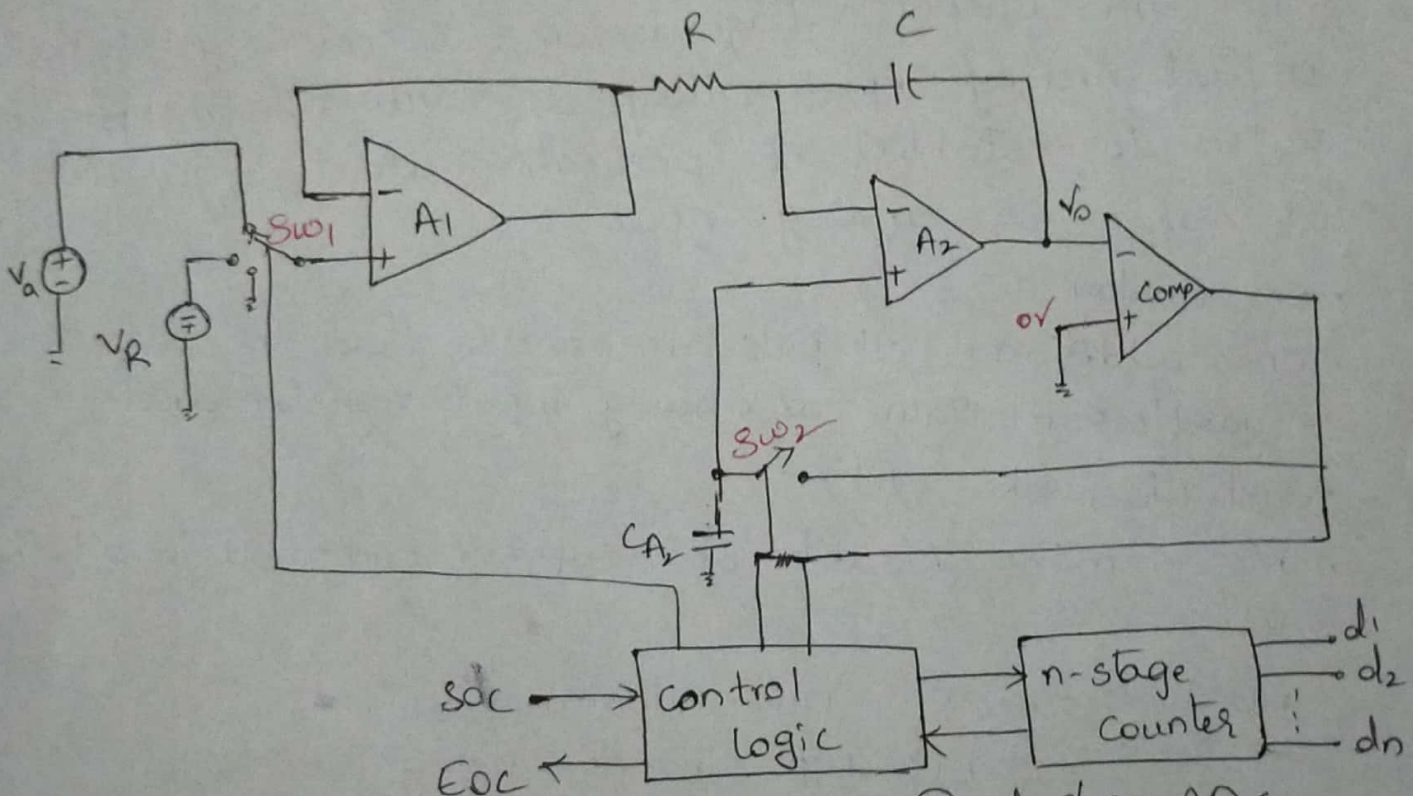
T - clk period

n - no. of bits

* **Dual Slope ADC :-**

This is an indirect method for A/D conversion where an Analog voltage and reference voltage are converted into time periods by an integrator and then measured by a counter.

* The speed of this conversion is slow but the accuracy is high.



functional Diagram of Dual slope ADC

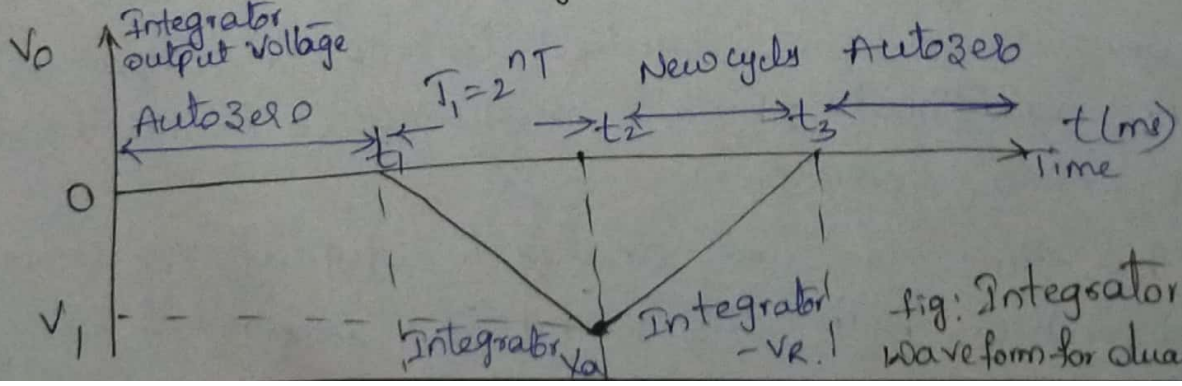


fig: Integrator o/p waveform for dual slope ADC

* The analog part of ckt consists of high impedance buffer (A_1), precision integrator (A_2) and voltage comparator while digital part consists of binary counter, output latch [control logic] and reference voltage V_R.

operation :-

- The converter first integrates the Analog input signal V_a for a first duration of 2^n clk periods. Then it integrates an integra internal reference voltage (V_R) of opposite polarity until the integrator output is zero.
- The number (N) of clock cycles required to return the integrator to zero is prop. to value of V_a averaged over the integration period.
- Before the SOC command arrives, the switch SW_1 is connected to gnd and SW_2 is closed. Any offset voltage present in A_1, A_2, comparator loop after integration appears across the capacitor C_{A_2} till the threshold of the comparator is achieved.
- The capacitor C_{A_2} provides automatic compensation for input-offset voltages of all the three amplifiers
- When SW_2 opens, C_{A_2} acts as memory elements to hold the voltage required to keep the offset nulled.
- At the arrival of SOC command at $t = t_1$, the control logic opens SW_2 and connects SW_1 to V_a and enables the counter starting from zero.
- The ckt used an n-stage ripple counter and therefore the counter reset to zero after counting 2^n pulses.

* The analog voltage V_a is integrated for a fixed number of 2^n counts of clk pulses after which counter resets to zero. If the clk period is T the integration takes place for time $T_1 = 2^n \times T$ and output is negative going ramp.
* The counter reset itself to zero at the end of interval T_1 and switch sw, is connected to reference voltage $(-V_R)$. The output voltage V_o have positive going ramp.
* As long as V_o is negative, output of comparator is positive and control logic allows the clk pulse to be counted.
* But when V_o becomes just zero at time $t = t_3$ the control logic issues an end of conversion [EOC] command and no futhers clk pulses enter the counter.
* The reading of counter at $t = t_3$ is proportional to analog i/p voltage.

$$T_1 = t_2 - t_1 = \frac{2^n \text{ counter}}{\text{clk rate}}$$

$$t_3 - t_2 = \frac{\text{digital count (N)}}{\text{clk rate}}$$

for an integrator

$$\Delta V_o = \left[\frac{-1}{RC}\right] V [\Delta t]$$

output voltage V_o will be equal to V_1 at instant t_2 and given as

$$V_1 = \left[\frac{-1}{RC}\right] V_a (t_2 - t_1)$$

voltage V_1 is also given as

$$V_1 = \left[\frac{-1}{RC}\right](-V_R)(t_2 - t_3)$$

$$\left[\frac{-1}{RC}\right] V_a (t_2 - t_1) = \left[\frac{-1}{RC}\right](-V_R)(t_2 - t_3)$$

$$V_a(t_2 - t_1) = V_R(t_3 - t_2)$$

Sub. values of

$(t_2 - t_1) = 2^n$ and $(t_3 - t_2) = N$ we get

$$V_a(2^n) = V_R(N)$$

$$\boxed{V_a = V_R\left[N/2^n\right]}$$

* DAC / ADC Specifications :-

Both D/A and A/D converters are available with with wide range of specifications.

(i) Resolution :-

It is defined as the ratio of a change in output voltage resulting for a change of 1 LSB at the digital input.

$$\text{Resolution (in volts)} = \frac{V_{fs}}{2^n - 1}$$ for n-bit DAC

V_{fs} - full scale output voltage.

* The resolution of an A/D converter is defined as smallest change in analog input for one-bit change at the output.

Ex :- I/P range of 8-bit A/D converters is divided into 255 intervals.

Resolution for 10V input voltage range.

$$R = \frac{10}{(2^8-1)} = \frac{10}{255} = 39.22\,mV/LSB$$

* The resolution can be determined by no. of bits in input binary word.

8-bit DAC: Resolution = $2^n = 2^8 = 256$.

* From the resolution, obtain the input-output equation for DAC.

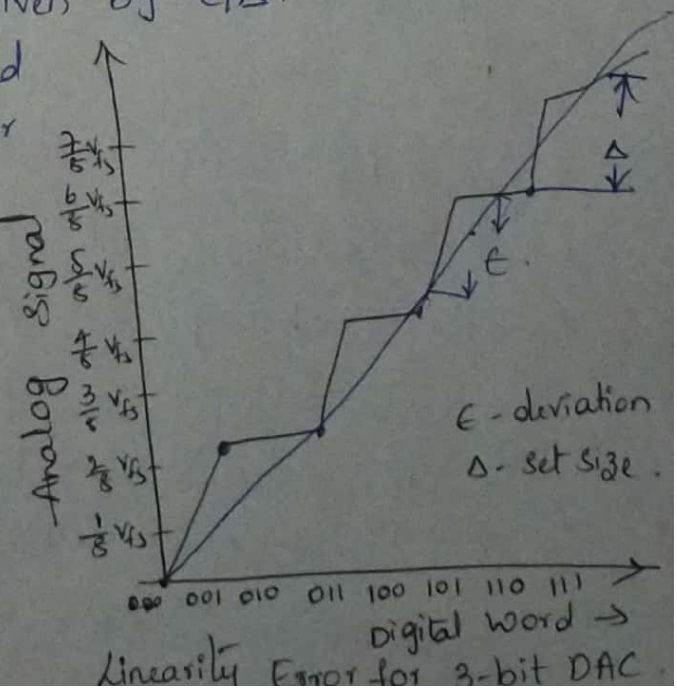
$$V_0 = \text{Resolution} \times D$$

D - Decimal value of digital input.

V_0 - output voltage.

* Linearity :-

- The linearity of A/D or D/A converter is an important parameter for measure of accuracy.
- In an ideal DAC, equal increment in digital input should produce equal increment in analog output and transfer curve should be linear.
- In actual DAC, output voltage doesn't fall on straight line due to gain and offset error. The linearity error measures the deviation of actual output from the ideal straight line output and given by ϵ/Δ.
- The Error is usually expressed as fraction of LSB increment or Percentage of full scale voltage.
- A good converter exhibits linearity error of less than $\left[\pm \frac{1}{2} LSB\right]$



Linearity Error for 3-bit DAC.

* Accuracy:- It gives the comparison of actual output voltage with the expected output. It is expressed in percentage.
- Absolute accuracy is max. deviation blw actual converter output and ideal converter output.
- Relative accuracy is maximum deviation after gain and offset errors have been removed. The accuracy of a converter is also specified in terms of LSB increments (or) Percentage of full scale voltage.

$$\text{Accuracy} = \frac{V_{fs}}{(2^n - 1)2}$$

* Monotonicity:-
A monotonic DAC is one whose analog output increases for an increase in the digital input.
- A converter said to have good monotonicity if it does not miss any step backward when stepped through its entire range by a counter.
- If a DAC has to be monotonic, the error should be less than $\pm \frac{1}{2}$ LSB at each output level.

* Conversion time:-
It is time required for conversion of analog signal into its digital equivalent. It is also called setting time. It depends on response time of switches and output of the amplifier.

* Settling time:-
It is the time required for the output to settle within a specified band $\pm \frac{1}{2}$ LSB of its final value for a given digital input i.e zero to full scale.

*stability :-

The performance of converter changes with temp, age and power supply variation. Hence all the relevant parameters such as offset, gain, linearity error and monoton -ocity must be specified over full temp. and power supply variations.

Problems :-

1. An 8-bit DAC has an output voltage of 0-2.55V. Define its resolution in two ways.

for given DAC

$n \rightarrow$ no. of bits $= 8$

(i) Resolution $= 2^n = 2^8 = 256$ levels

i.e o/p voltage can have 256 different values including zero.

V_{ofs} - full scale output voltage

$V_{fs} = 2.55V$

(ii) Resolution $= \frac{V_{ofs}}{2^n - 1} = \frac{2.55}{2^8 - 1} = \frac{10mV}{1LSB}$

Thus an input change of 1LSB causes the o/p to change by 10mV

*The digital input for 4-bit DAC is 0110 calculate its final output voltage.

for given DAC $n = 4$

$V_{ofs} = 15V$

Resolution $= \frac{V_{ofs}}{2^n - 1} = \frac{15}{2^4 - 1} = 1V/LSB$

$V_o =$ Resolution $\times D$.

$D \rightarrow$ decimal of $(0110)_2 = 6$.

$V_o = 1V/LSB \times 6 = 6V$.

* An 8-bit DAC has resolution of 20mV/LSB. find V_{fs} and V_o if input is $(10000000)_2$

Resolution $= \frac{V_{ofs}}{2^n - 1}$

$20 \times 10^{-3} = \frac{V_{ofs}}{2^8 - 1} \Rightarrow V_{ofs} = 20 \times 10^{-3} \times 255$

$V_{of} = 5.1V$

$D = (10000000)_2 = 128$.

$V_o = \text{Resolution} \times D$

$V_o = 20 \times 10^{-3} \times 128 = 2.56V$.

* find out stepsize and analog output for 4-bit R-2R ladder DAC when input is 1000 & 1111. Assume $V_r = 5V$

for given DAC $n = 4$. $V_{ofs} = +5V$

Resolution $= \frac{V_{ofs}}{2^n - 1} = \frac{5}{2^4 - 1} = \frac{5}{15} = \frac{1}{3} V/LSB$

$V_o = \text{Resolution} \times D$.

for D = Decimal of $(1000)_2 = 8$

$V_o = \frac{1}{3} \times 8 = 2.67V$

for D = Decimal of $(1111)_2 = 15$

$V_o = \frac{1}{3} \times 15 = 5V$.

* The basic step of 9-bit DAC is 10.3mV. If 00000000 represents 0V what o/p produced if i/p is 101101111?

o/p voltage for input → 101101111

$V_o = V_{fs}[d_1 2^{-1} + d_2 2^{-2} + \cdots + d_n 2^{-n}]$

$V_o = 10.3mv[1\times2^8 + 0\times2^7 + 1\times2^6 + 1\times2^5 + 1\times2^3 + 1\times2^2 + 1\times2^1 + 1\times2^0)$

$= 10.3mv[367)$

$= 3.78V.$

* A dual slope ADC uses 16-bit counter & 4MHz clock rate The max. i/p voltage is +10V. The max. integrator o/p voltage should be -8V when the counter has cycled through 2^n counts. The capacitor used in integrator is 0.1μf find the value of R of integrator.

Time period (T) = $t_2 - t_1$

$t_2 - t_1 = \frac{2^n \text{ counts}}{\text{clk rate}} \Rightarrow t_2 - t_1 = \frac{2^{16}}{4MHz} = 16.38ms$

for Integrator

$\Delta V_o = \left[-\frac{1}{RC}\right] V_a (t_2 - t_1)$

$RC = \frac{(-10V)}{(-8V)} (16.3ms)$

$RC = 20.47ms$

$R = \frac{20.47ms}{0.1\mu f} = 204.7k\Omega \simeq 205k\Omega$

for $V_a = +4.129V$ digital number.

$V_a = V_R[N/2^n] = 65536\left[\frac{4.129V}{8V}\right]$

$= 33825$

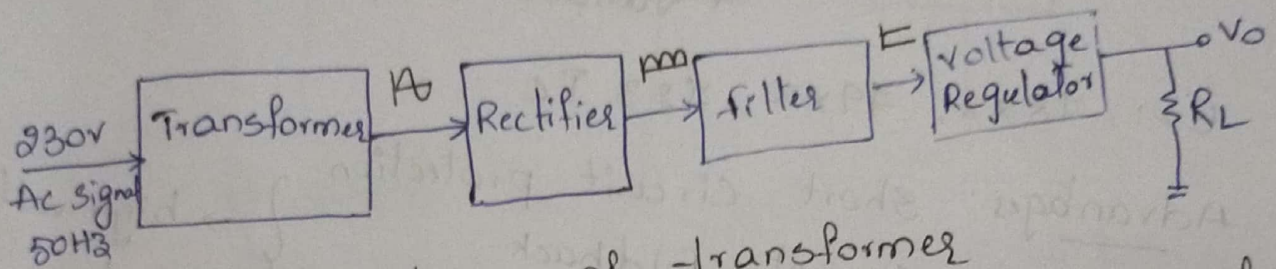
Binary equivalent 1000|0000|0000|0001.

MODULE - IV
Voltage Regulators

* **Voltage Regulator:-**

A voltage regulator is a circuit that provides stable dc voltage regardless of changes in load current. These are used for powering other electronic ckts.

- All the electronic devices requires the dc supply that dc supply can be provided by using batteries or cells this process is expensive. The solution for this process is AC supply is converted into the Dc.



- There are two types of transformer
  * step up transformer [The output of setup transformer is more than the input voltage].
  * step down transformer [The output of set down transformer is less than the input voltage].
* **Rectifier**: Rectifier is used to convert AC signal into pulsating Dc signal ⌇⌇⌇ pulsating dc
* **filter**: Removes or convert pulsating dc to Pure dc. ⎍ pure dc.

- If any changes in the input signal than the changes occurs at the filter. so to regulate that we use use one more block called voltage Regulator.

* The voltage regulator are classified into two types.
  - Shunt voltage Regulator } Linear
  - Series voltage Regulator }
  - Switching Regulator.

* Series regulators use power transistor connected in series between unregulated dc input and load. The output voltage is controlled by using continuous voltage drop taking place across series pass transistor since transistor conducts in linear region these are called linear regulators.

Linear regulators — fixed output voltage
                  — variable output voltage

Ex: 78xx, 79xx, 723 IC

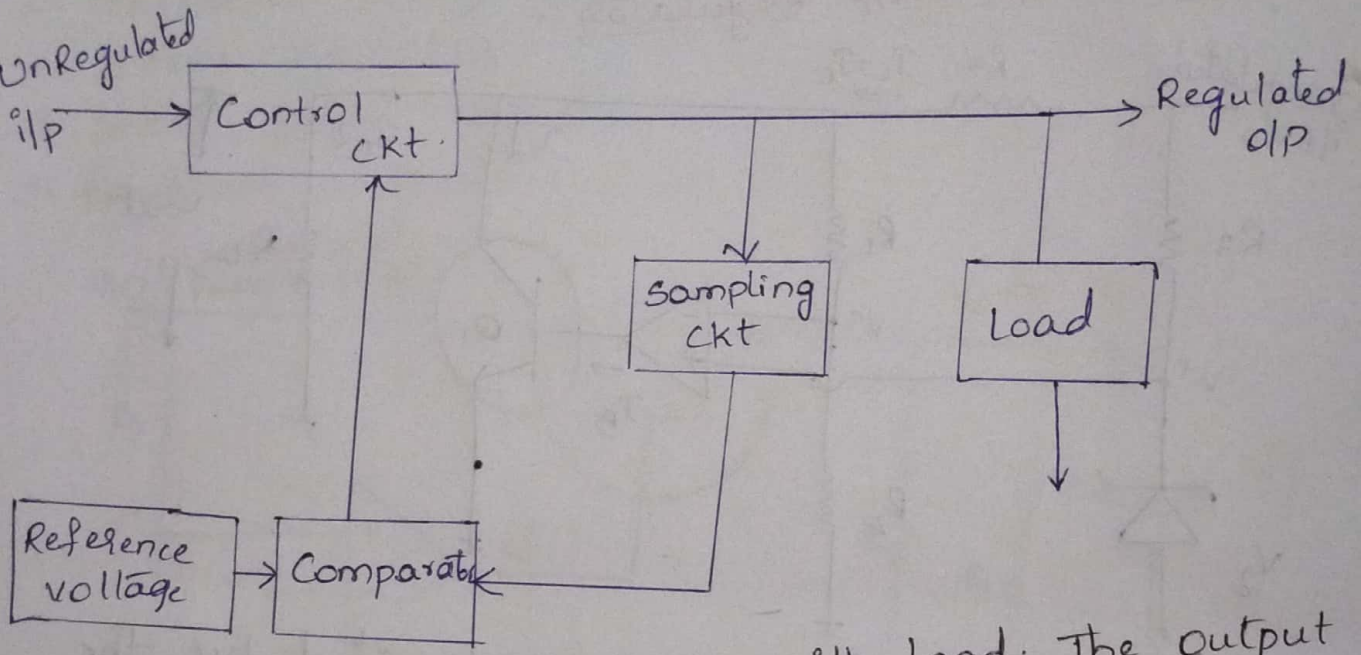
Advantages: short circuit protection
current foldback
current/boosting voltage
thermal shutdown.
} → high voltage Applications.

- Switching regulators operate the power transistor as high frequency ON/off switch so that power transistor does not conduct current continuously.
- Power dissipation is substantial during the switching intervals (ON/off). This gives improved efficiency over series regulator.

* Applications:-
Voltage regulators are used for ON-CARD regulation and laboratory-type power supplies. The switching type voltage regulators are used in pulse width modulation (PWM) push pull bridge and series type switch mode supplies.

* Based on the arrangement of the various components like:
  - Sampling circuit
  - Reference voltage
  - Comparator
  - Control circuit.

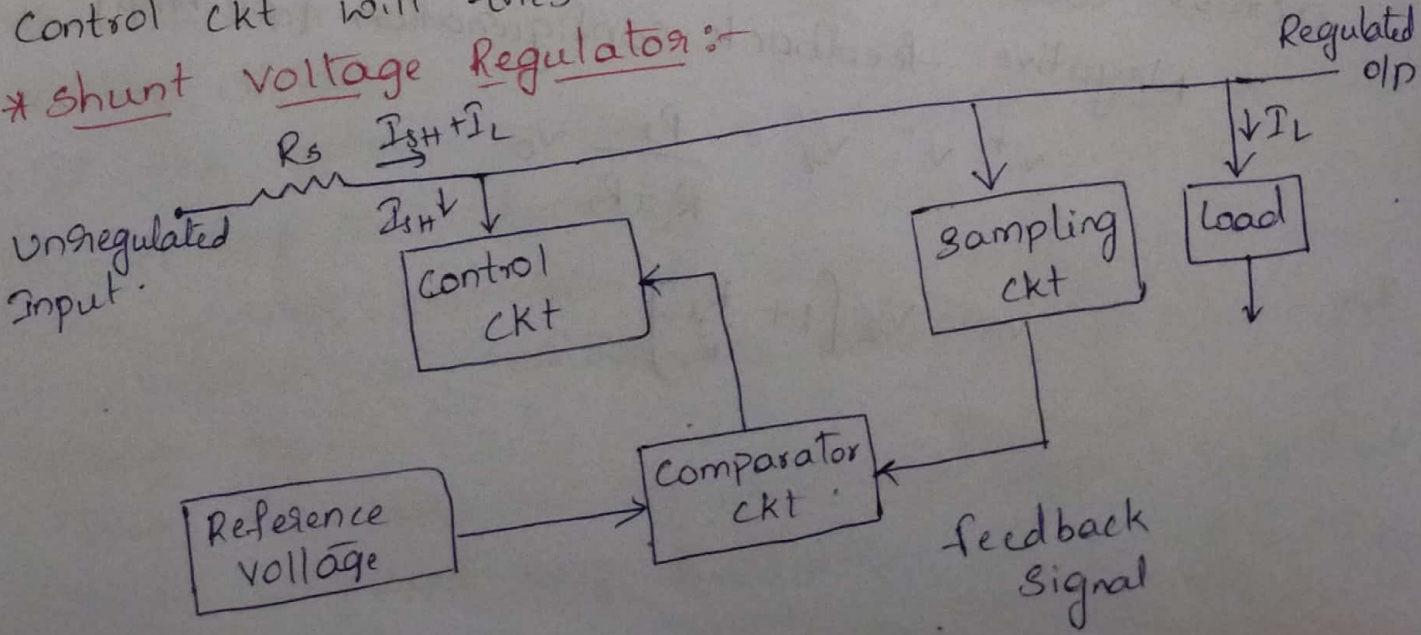
* Series voltage regulator:-



The control ckt is series with load. The output voltage is sampled using sampling ckt and then compared with the reference voltage based on the error voltage is control voltage will take the corrective action.

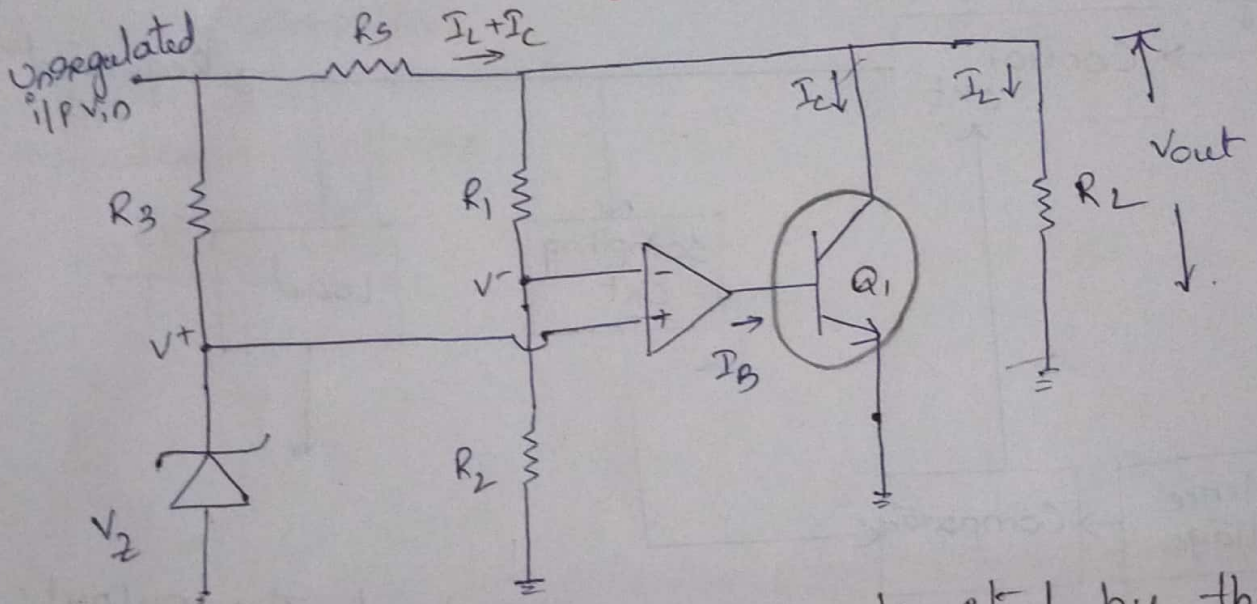
* If the output voltage increases or decreases then the control ckt will tries to make the constant voltage.

* Shunt voltage Regulator:-



* Control circuit is shunt with load. The o/p voltage is sampled with using sampling ckt and compared with the ref. voltage. If they is any change in the o/p voltage then the control ckt will shunt with additional current I_{SH} and it makes the voltage drop across (R_S) increases.

* Shunt OP-Amp Regulator :-



* The excess load current is limited by the transistor (Q_1) which acts as the control element and bypass the excess current to ground Hence stable or regulated dc voltage generated across load.

Negative feedback configuration [op-Amp]

$$V^+ = V^- = V_Z = \frac{R_2}{R_1 + R_2} V_O$$

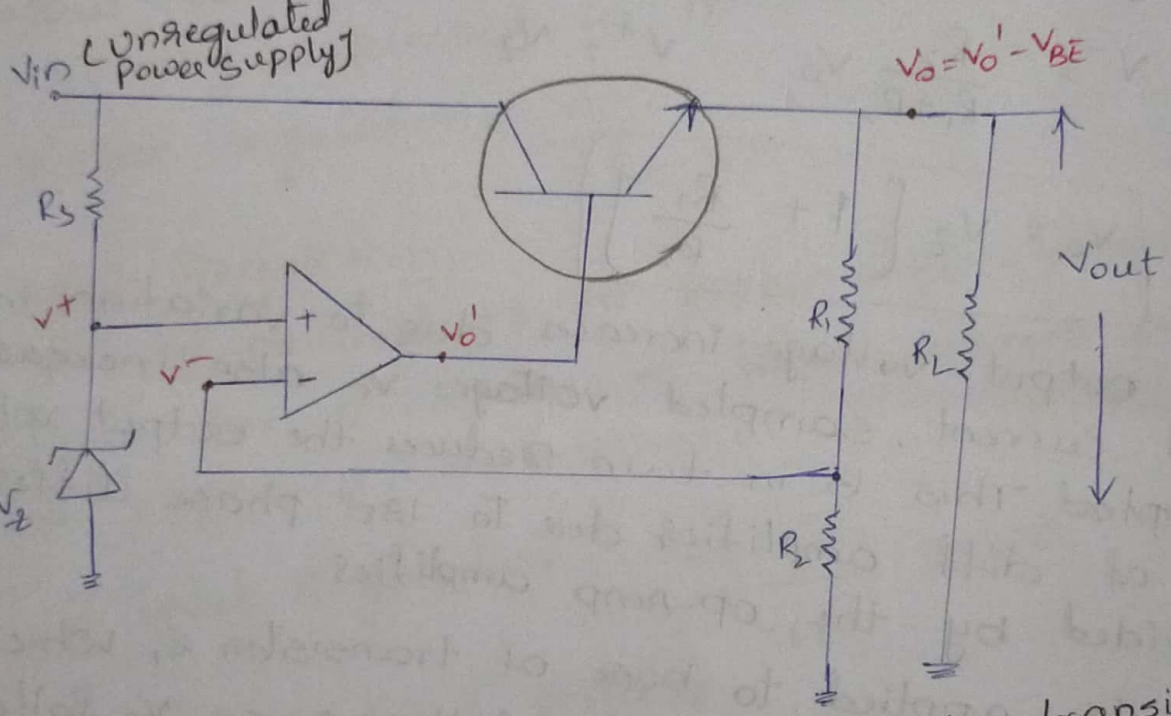
$$V_O = V_Z \left[1 + \frac{R_1}{R_2}\right]$$

* Series Op-Amp Regulator :-

A voltage regulator is an electronic ckt that provides stable dc voltage independent of load current, temperature and ac line voltage variation

* The regulated power supply uses discrete components. The ckt consists of four parts.

(1) Reference voltage ckt.
(2) Error Amplifier
(3) Series pass Transistor
(4) feedback Network.



. The control circuit is comprised of the transistor and the op-Amp and output voltage is sampled by using voltage divider.

. If the output voltage (V_o) increases then the output of op Amp (V_o') decreases.

. The power transistor Q_1 is in series with the unregulated dc voltage V_{in} and regulated output voltage V_o.

. Thus it absorbs the difference between these two voltages whenever any fluctuation in output voltage occurs.

* The transistor Q_1 is also connected as an emitter follower and provides sufficient current gain to drive the load.
* The output voltage is sampled by the $R_1 - R_2$ divider and feedback to (-) input terminal of OP-Amp error amplifier.
* This sampled voltage is compared with the reference voltage V_{ref}. The output V_o' of error amplifier drives the series transistor Q_1.

By virtual Ground concept $V^+ = V^-$

$$V^- = \frac{R_2}{R_1 + R_2} V_o \qquad V^+ = V_z.$$

$$\boxed{V_o = V_z \left[1 + \frac{R_1}{R_2} \right]}$$

* If output voltage increases due to variation in load current, sampled voltage V_o also increases. sampled This is in turn reduces the output voltage V_o' of diff. amplifier due to 180° phase difference provided by the OP-Amp amplifier.
* V_o' is applied to base of transistor Q_1 which is used to as an emitter follower. so V_o follows V_o' (i.e) V_o also reduces. Hence increase in V_o is nullified. similarly reduction in output voltage also gets regulated.

Advantages :- Good efficiency.

Disadvantages :- ~~short~~ No short circuit protection.

- Input voltage = 10 - 20V

$\Delta V = 50mV$

% Linear regulation = 0.5 %

* IC voltage Regulators :-

The advent of microelectronics it is possible to incorporate the complete circuit on a monolithic silicon chip. This gives low cost, high reliability, reduction in size and excellent performance. Examples of monolithic regulators are 78xx / 79xx series and 723 general purpose regulators.

* Line regulation :-

It is defined as the percentage change in the output voltage for a change in input voltage. It is usually expressed in millivolts.

$$\% \text{ Line regulation} = \frac{\Delta V_o}{\Delta (V_i \cdot V_o)} \times 100$$

* Load regulation :-

It is defined as the percentage change in output voltage for a change in load current and it is also expressed in millivolts.

$$\% \text{ Load Regulation} = \frac{V_{NL} - V_{fL}}{V_{fL}} \times 100$$

V_{NL} - No load voltage

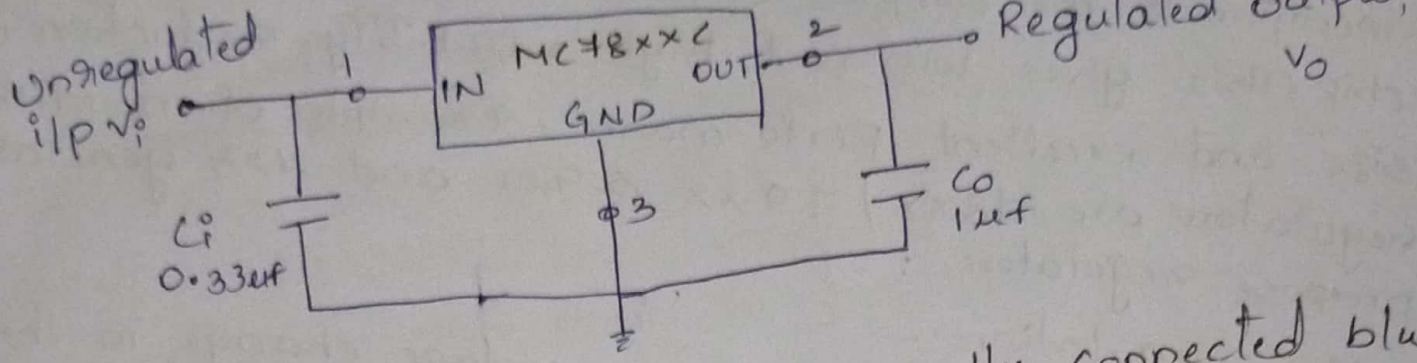
V_{fL} - full load voltage.

* fixed voltage series Regulator :-

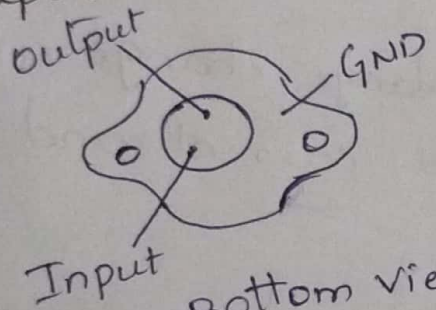
78xx series are three terminal, positive fixed voltage regulators. There are seven output voltage option available such as 5, 6, 8, 12, 15, 18 and 24 V. The last two numbers (xx) indicates the output voltage.

78 xx provides fixed output positive voltage regulator.

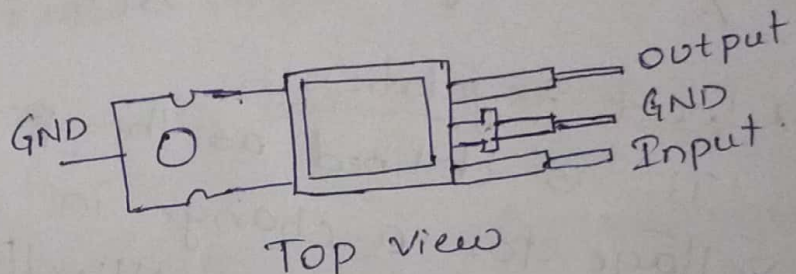
79xx series of fixed output, negative voltage regulator.



A capacitor C_i (0.33uf) is usually connected blw input terminal and ground to cancel the inductive effect due to long distribution leads. The output capacitor C_o (1uf) improves the transient response.



Bottom view



Top view

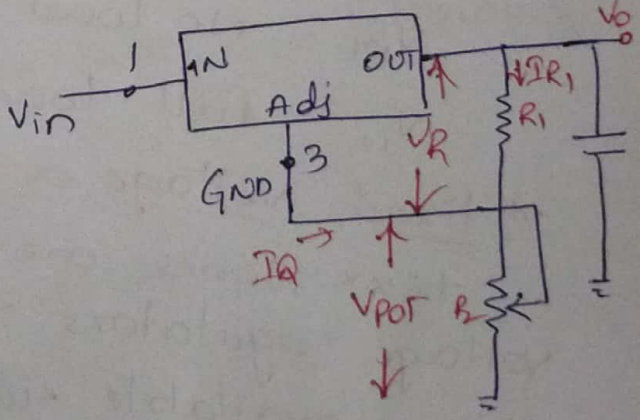
* Adjustable voltage Regulator:-

The variable output voltage achieved by using fixed three terminal regulator, with the grd terminal floating.

output voltage:

$$V_o = V_R + V_{POT}$$
$$= V_R + (I_Q + I_{R_1}) R_2$$
$$= V_R + I_Q R_2 + \frac{V_R}{R_1} R_2$$

$$\boxed{V_o = \left[1 + \frac{R_2}{R_1}\right] V_R + R_2 I_Q.}$$



The effect of I_Q is minimized by choosing R_2 small enough to minimize term $I_Q R_2$. The minimum voltage is value of fixed voltage available from the regulator.

* characteristics :-

1. V_o :- The regulated output voltage is fixed at a value as specified by the manufacturer. There are a number of models available for different output voltage
ex :- 78xx series has output voltage at 5, 6, 8 etc.

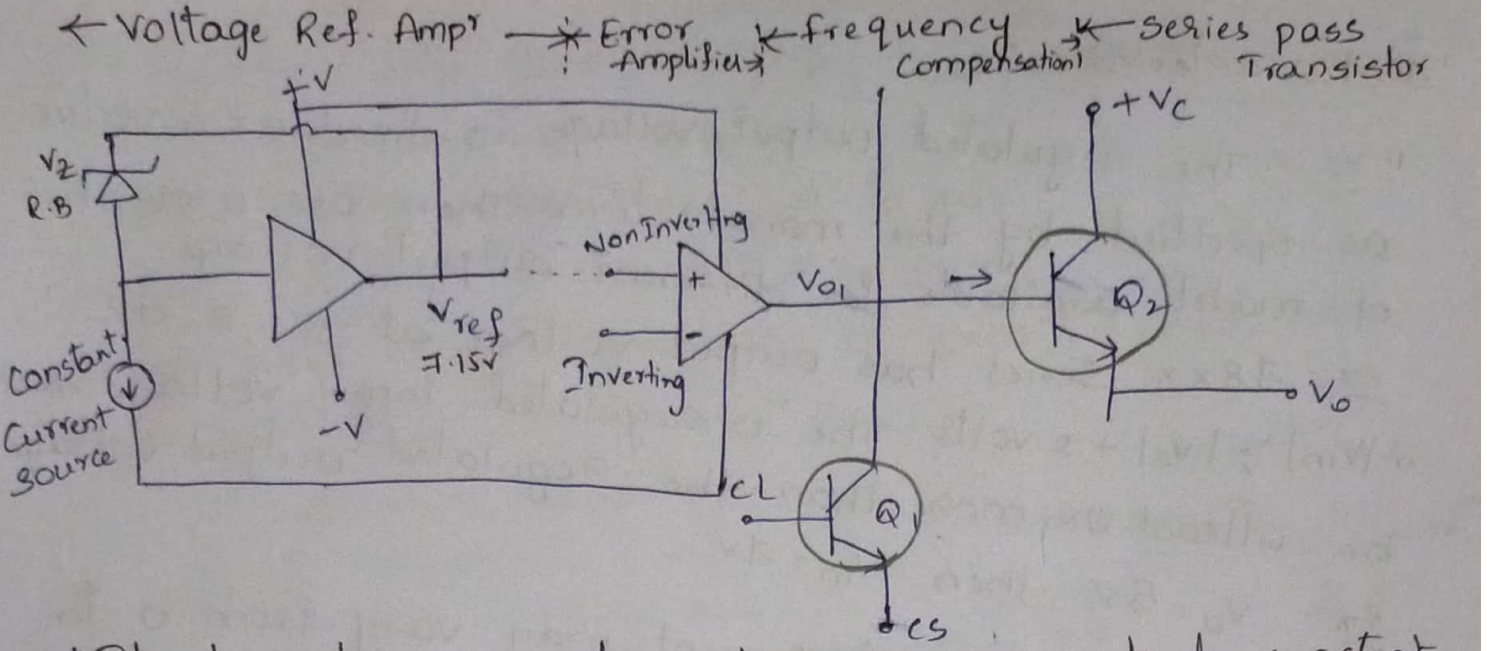
2. $|V_{in}| \geq |V_o| + 2$ volts : The unregulated input voltage must be atleast 2v more than the regulated output voltage
Ex :- $V_o = 5V$ then $V_{in} = 7V$

3. I_o (max) :- The load current may vary from 0 to rated maximum output current. The Ic is usually provided with a heat sink, otherwise it may not provide the rated maximum output current.

4. Thermal shutdown :- The Ic has a temperature sensor (built-in) which turns off the Ic when it becomes too hot (usually 125°c to 150°c). The output current will drop and remains there until the Ic has cooled significantly.

* Ic 723 General Purpose Regulator :-

. The three terminal regulators have the following limitation.
(i) No short circuit protection
(ii) output voltage [positive or Negative].
* These limitations are overcomed in 723 general purpose regulator, which can be adjusted over wide range of both positive and negative regulated voltage.



*It has two separate sections. The Zener diode, constant current source and reference amplifier produces fixed voltage of about ∓V at terminal V_{ref}. The constant current source forces the Zener to operate at fixed point such that Zener outputs fixed voltage.

* The other section of IC consists of an error amplifier, a series pass transistor Q_1 and current limit transistor Q_2.

* The Error amplifier compares a sample of output voltage applied at inverting input terminal to reference voltage V_{ref} applied at the non Inverting input terminal.

*The Error signal controls the conduction of Q_1. These two sections are not internally connected but the various points are brought out on the IC package. ∓123 regulated IC is available in 14-pin dual-in line package and 10 pin metal can.

Features:-

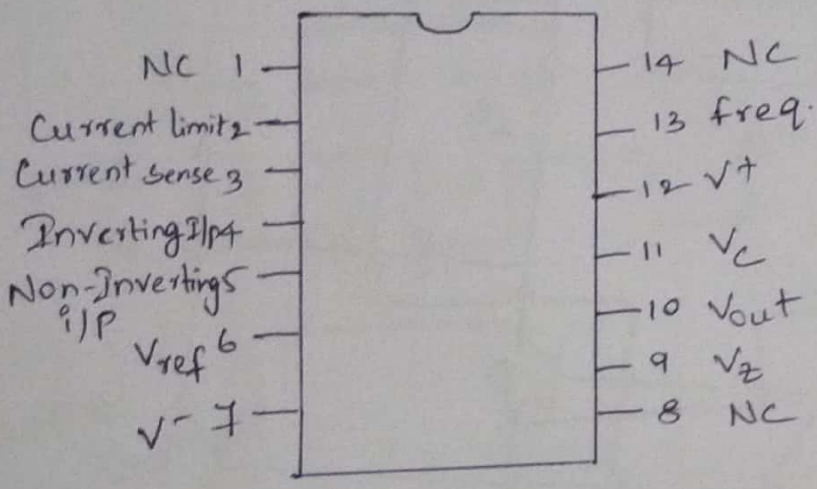
• It is the Series voltage regulator provides +ve and -ve voltage

• It provides current upto 150mA [without

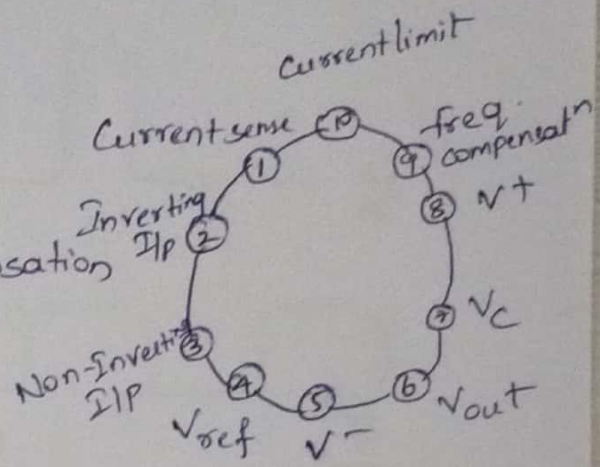
connecting any resistors] by with external resistor current provides upto 10A.

- Input voltage between 9 to 40V
- output voltage between 2 to 37V
- Load and line regulation is 0.01%. [It provide high stability].

Dual-in-line package



Top view.

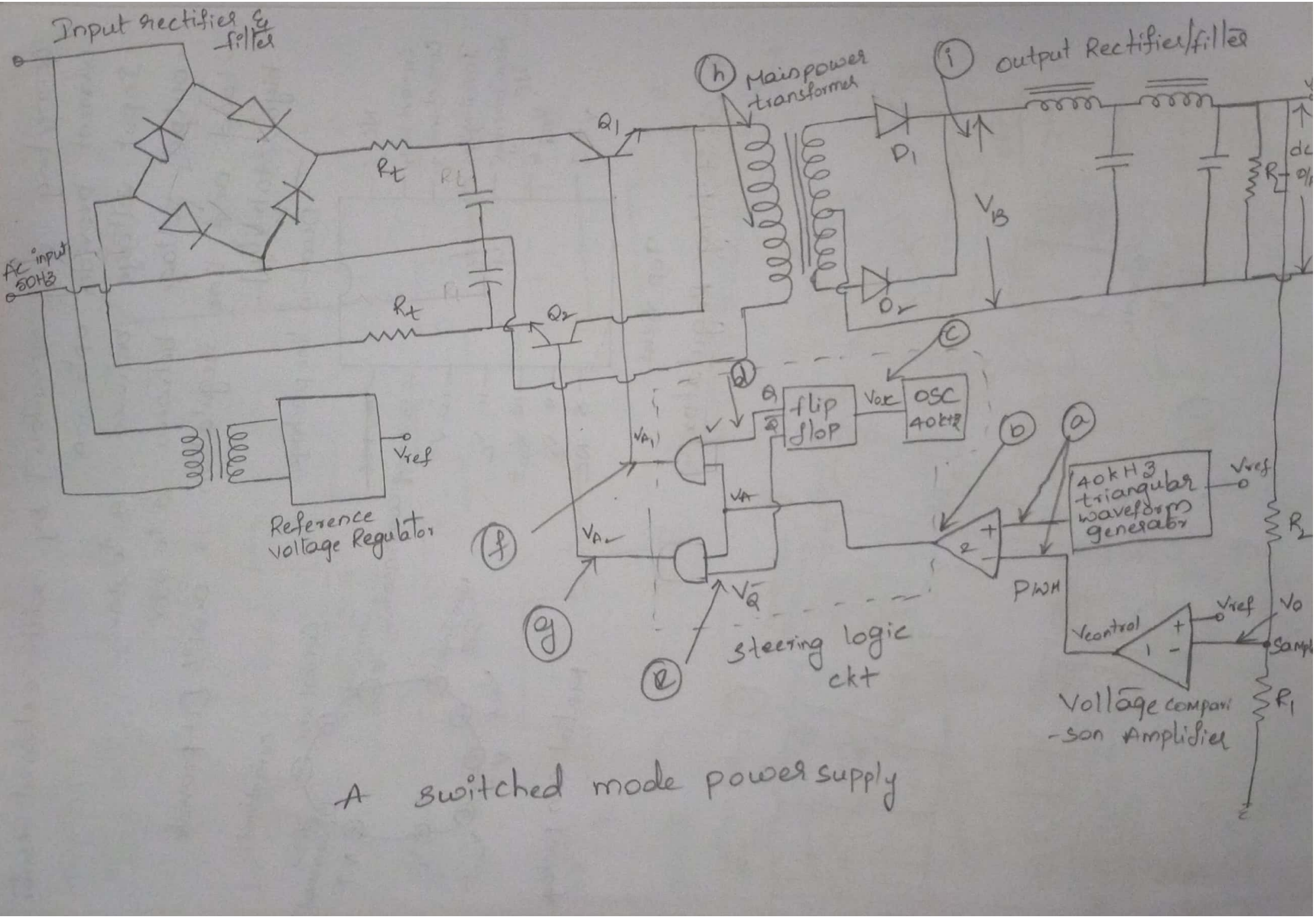


Metal can package

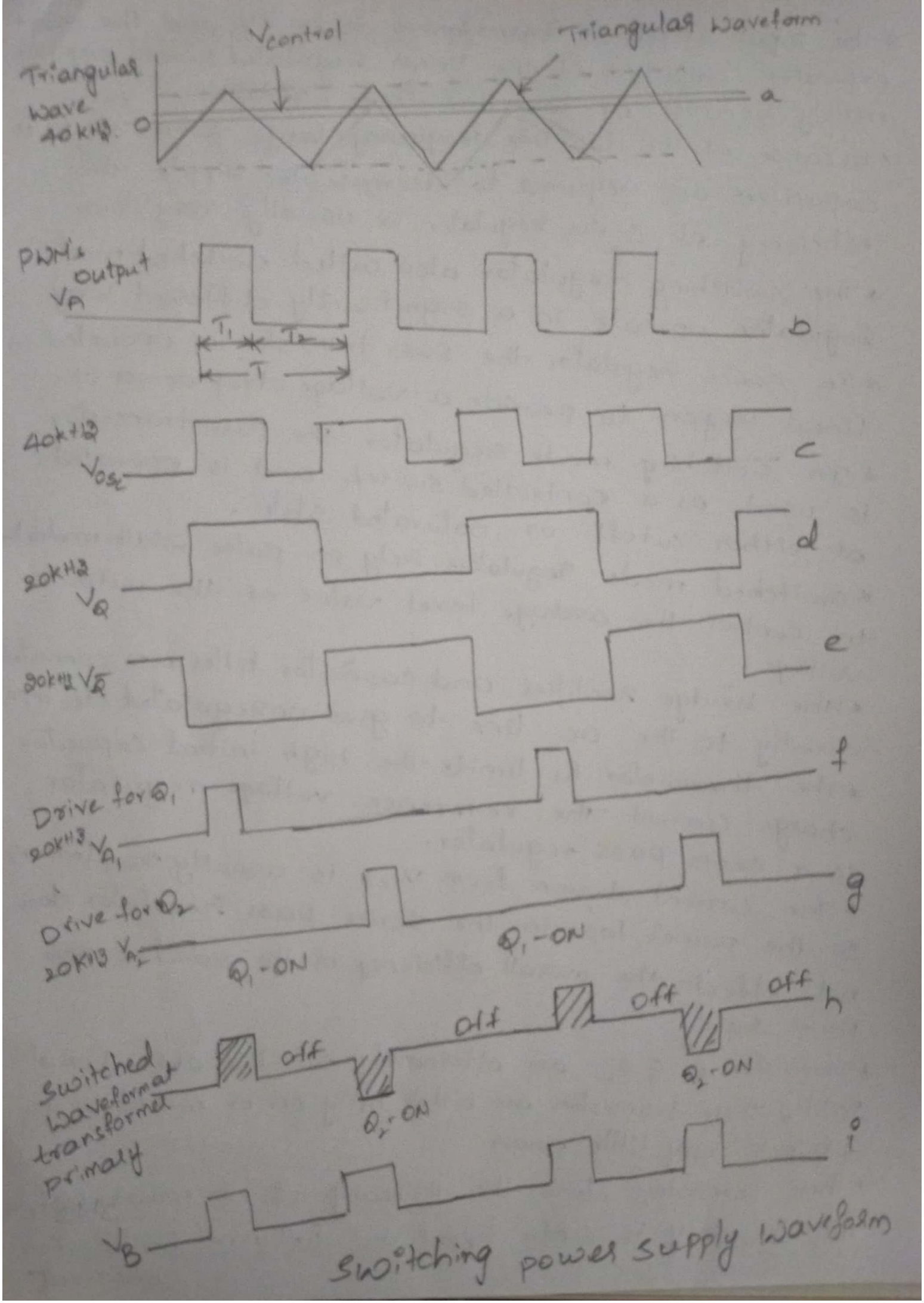
* Switching Regulator:-

(1) output rectified/ filter

Vo



A switched mode power supply



* The input stepdown transformer is bulky and the most expensive component of the linear regulated power supply mainly because of low line freq. (50Hz).
• Because of the low line frequency, large values of filter capacitors are required to decrease the ripple. The efficiency of series regulator is usually very low.
* The switching regulator also called switched mode regulator operate in a significantly different way.
* In series regulator the pass transistor is operated in linear region to provide a voltage drop across it.
* In switching mode regulator the pass transistor is used as a controlled switch and is operated at either cutoff or saturated state.
* switched mode regulators rely on pulse width modulation to control the average level value of the output voltage.
* the bridge rectifier and capacitor filter are connected directly to the ac line to give unregulated dc input
* The thermistor R_t limits the high initial capacitor charge current. The reference voltage regulator is a series pass regulator.
* the current drawn from V_{ref} is usually V_{ref} (MICROMA) so the power loss in the series pass regulator does not effect the overall efficiency of the switched mode power supply.
* Transistor Q_1 & Q_2 are alternately switched off and on at 20kHz. These transistors are either fully 'on' or cutoff. so they dissipate very little power.
* These transistors drive the primary of the main transformer. The secondary is centre-tapped and full wave rectification

is achieved by diodes D_1 and D_2.

* This unidirectional square wave is next filtered through a two stage LC filter to produce output voltage V_o.

MODULE - V

CMOS LOGIC AND DIGITAL CIRCUITS

*Introduction :-

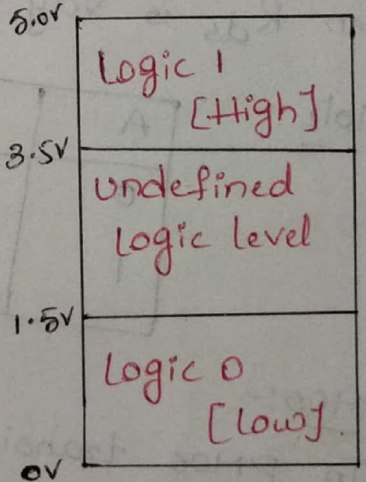
Now-a-days digital IC's are most commonly used in the modern digital systems. With the wide spread use of IC's it becomes necessary to know and understand the electrical characteristics of the most commonly IC logic families such as CMOS, bipolar, TTL and ECL. These logic families differ in the major components that they use in their circuitry. Bipolar use diode whereas TTL and ECL use bipolar transistors as their major circuit element. The MOS and CMOS use unipolar MOSFET transistors as their principle component. Because of the use of different principle component their electrical behaviour are different.

* CMOS Logic :-

The basic building blocks in CMOS logic circuits are MOS transistors. CMOS means Complementary Metal oxide Semiconductor.

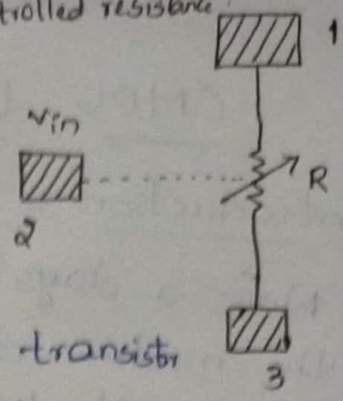
* CMOS Logic Level :-

The CMOS logic level for CMOS circuit may interpret any voltage in the range 0-1.5v as a logic 0 and in the range 3.5v-5.0v as a logic 1 as shown in figure. The voltage in between 1.5v to 3.5v are not expected to occur except during signal transistions and if they occur, the circuit may interpret them as either 0 to 1.



*MOS Transistor :-

MOS transistor as voltage controlled resistance

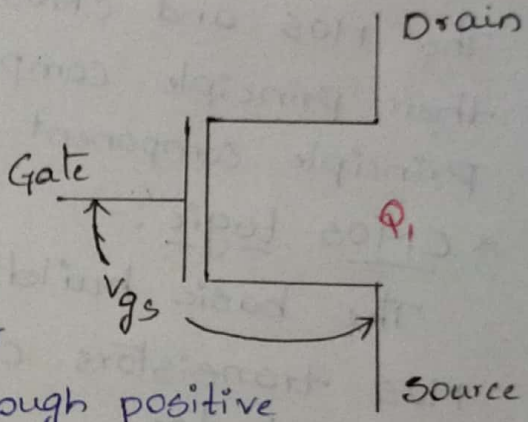


A MOS transistor is a three terminal device that acts like a voltage controlled resistance. An input voltage applied to one terminal controls the resistance between the remaining two terminals. In CMOS logic circuits, MOS transistor is operated so that its resistance is always either very high or very low.

There are two types of MOS transistors. They are

1. NMOS [n-channel]
2. PMOS [P-channel].

*NMOS :-

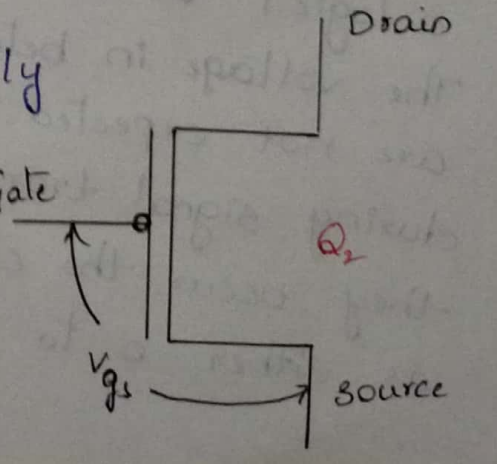


In NMOS transistor the voltage from gate to source is normally zero or positive. If $V_{gs} = 0$ then the resistance from drain to source R_{ds} is very high. It is of order of few Mega ohms. If V_{gs} is enough positive then R_{ds} is very low. It is between 0-10 ohms

Note :-

A	Q_1	output
0	off	0
1	ON	1

*PMOS :-



In PMOS transistor V_{gs} is normally zero or negative. If V_{gs} is zero, then the R_{ds} is very high and V_{gs} is enough negative.

Note :-

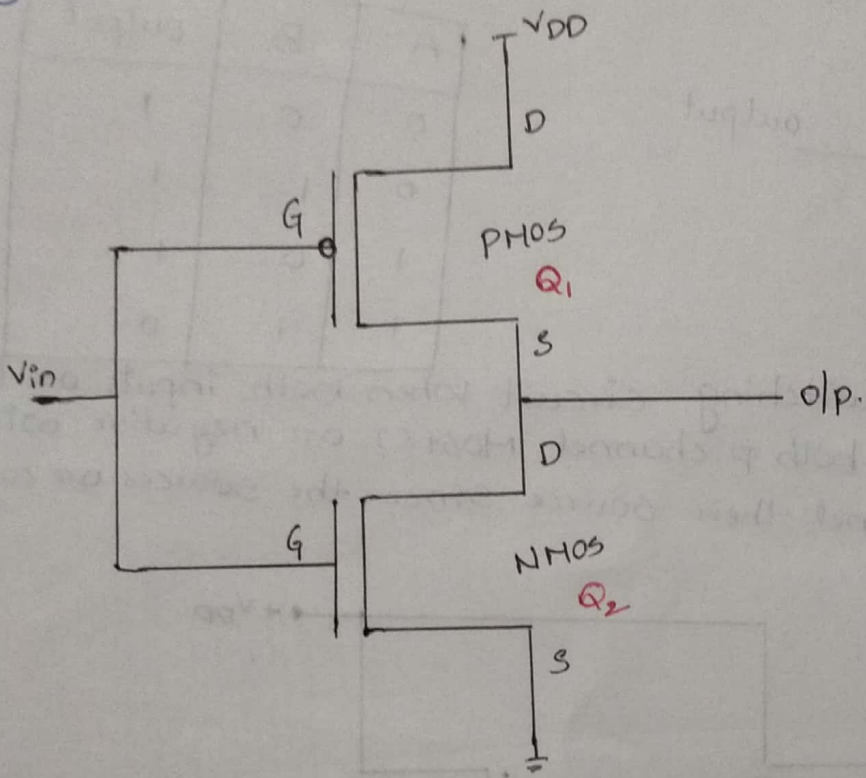
A	Q_2	output
0	ON	1
1	off	0

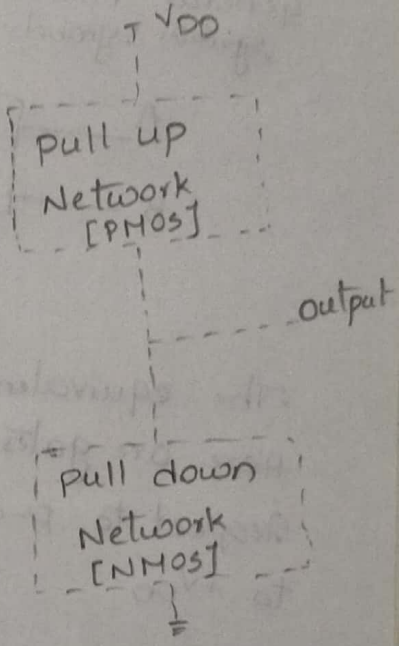
*~~CMOS NAND Gate~~ :-

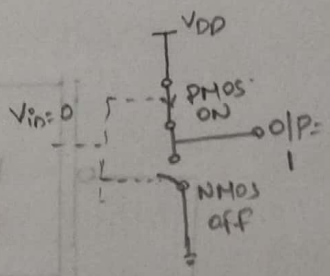
* Basic CMOS inverter :-

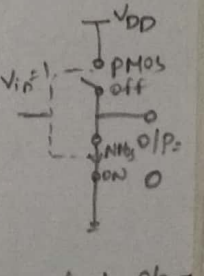
CMOS : PMOS + NMOS

Basic CMOS is also called as CMOS inverter. The CMOS is combination of PMOS and NMOS.



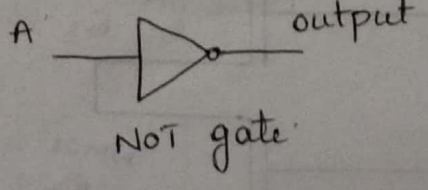






V_{in}	Q_1	Q_2	output
0	ON	off	1
1	off	ON	0

* The basic CMOS inverter acts as a NOT Gate.



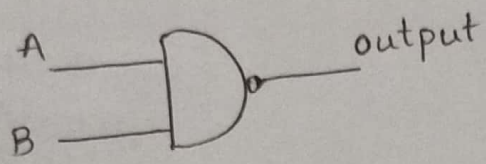
A	output
0	1
1	0

	NAND/AND [MULTIPLICATION]	NOR/OR [ADDITION]
PMOS	Parallel	Series
NMOS	Series	parallel.

* CMOS NAND Gate :-

CMOS NAND gate consists of two p-channel MOSFETs, Q_1 and Q_2 connected in parallel and two N-channel MOSFETs Q_3 and Q_4 connected in series for two input NAND gate.

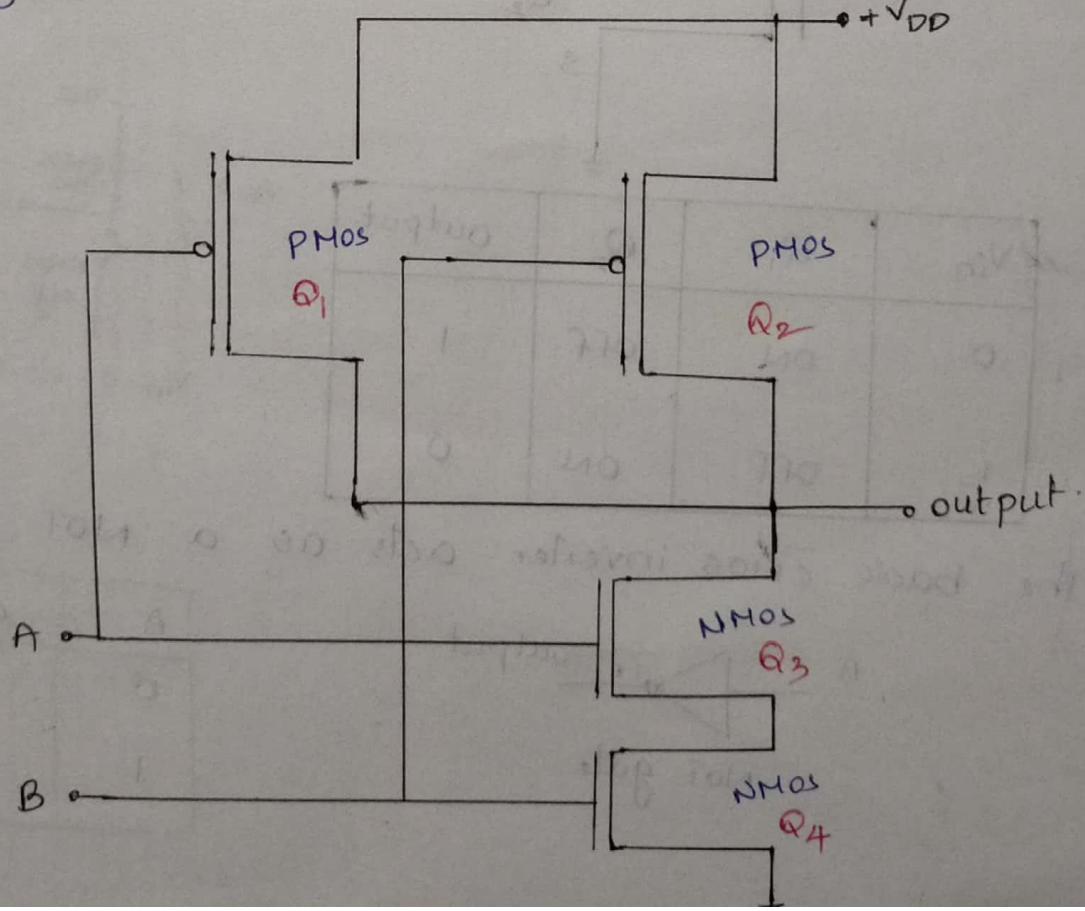
General NAND Gate :-
Symbol symbol.



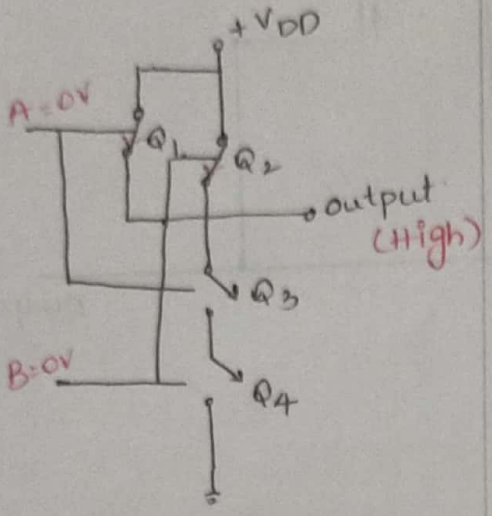
Truth Table :-

A	B	output
0	0	1
0	1	1
1	0	1
1	1	0

The equivalent switching circuit when both inputs are low. Here are gates of both p-channel MOSFET are negative with respect to p-channel their source. Since the sources are connected to $+V_{DD}$.



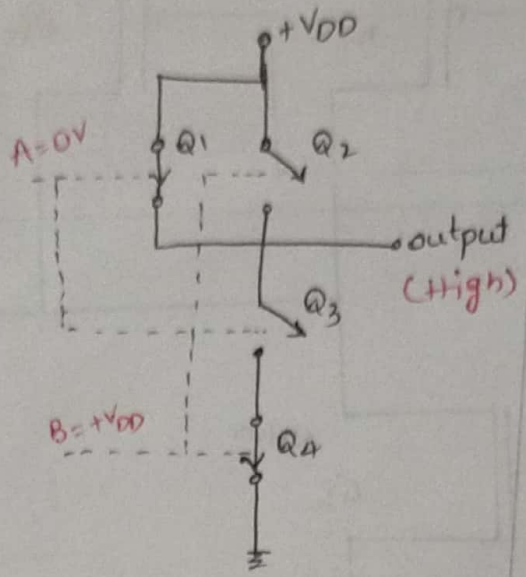
Thus Q_1 and Q_2 are both ON since the gate to the source voltage of Q_3 and Q_4 are both 0V. those MOSFET are off. the output is therefore connected to $+V_{DD}$ (High) through Q_1 and Q_2 and is disconnected from ground and similarly all other.



$A = B = 0V$

$V_{G_1} = V_{G_2} = -V_{DD}$

$V_{G_3} = V_{G_4} = 0V.$

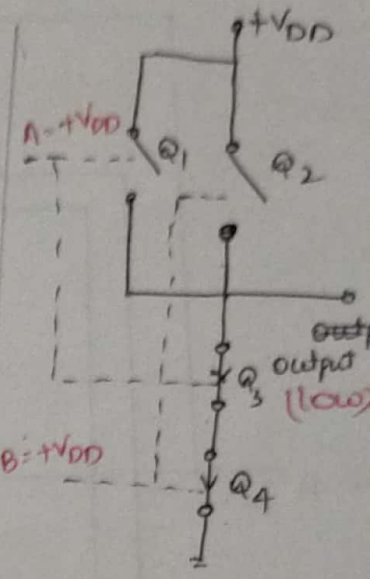


$A = 0V \quad B = +V_{DD}$

$V_{GS_1} = -V_{DD}$

$V_{GS_4} = +V_{DD}$

$V_{GS_2} = V_{GS_3} = 0V$



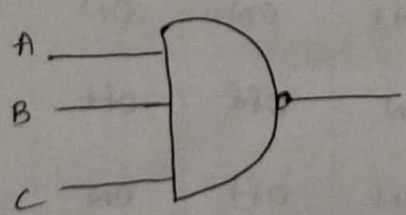
$A = B = +V_{DD}$

$V_{GS_1} = V_{GS_2} = 0V$

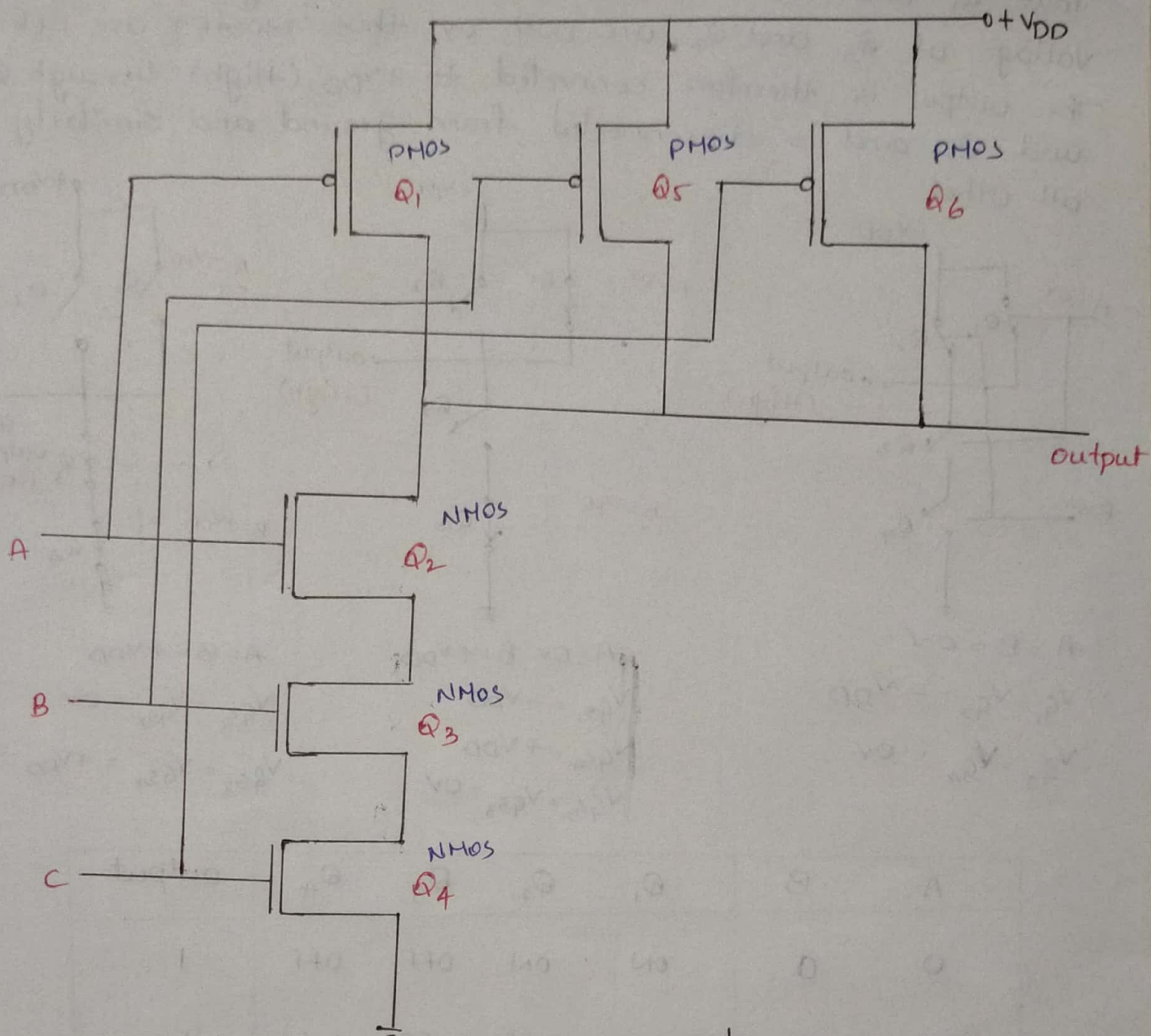
$V_{GS_3} = V_{GS_4} = +V_{DD}$

A	B	Q_1	Q_2	Q_3	Q_4	output
0	0	ON	ON	Off	Off	1
0	1	ON	Off	Off	ON	1
1	0	Off	ON	ON	Off	1
1	1	Off	Off	ON	ON	0

Truth table for CMOS 2- input NAND gate.



3-Input NAND gate Symbol.



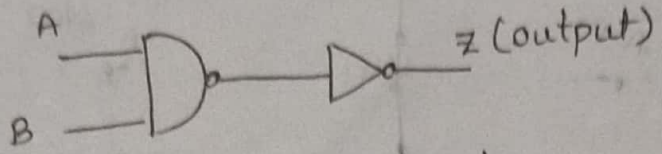
CMOS 3-Input NAND Gate

A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z [output]
0	0	0	ON	Off	Off	Off	ON	ON	1
0	0	1	ON	Off	Off	ON	ON	Off	1
0	1	0	ON	off	ON	Off	Off	ON	1
0	1	1	ON	off	ON	ON	off	off	1
1	0	0	Off	ON	Off	off	ON	ON	1
1	0	1	off	ON	ON	ON	Off	off	1
1	1	0	off	ON	ON	Off	off	ON	1
1	1	1	Off	ON	ON	ON	off	Off	0

* CMOS AND Gate:-

Truth Table:-

A	B	output
0	0	0
0	1	0
1	0	0
1	1	1



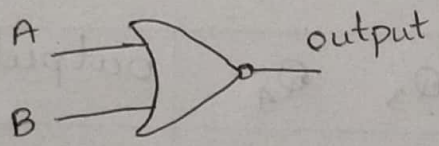
Symbol for AND gate.

The CMOS AND gate can be designed by using CMOS NAND gate and CMOS inverter.

* CMOS NOR gate:-

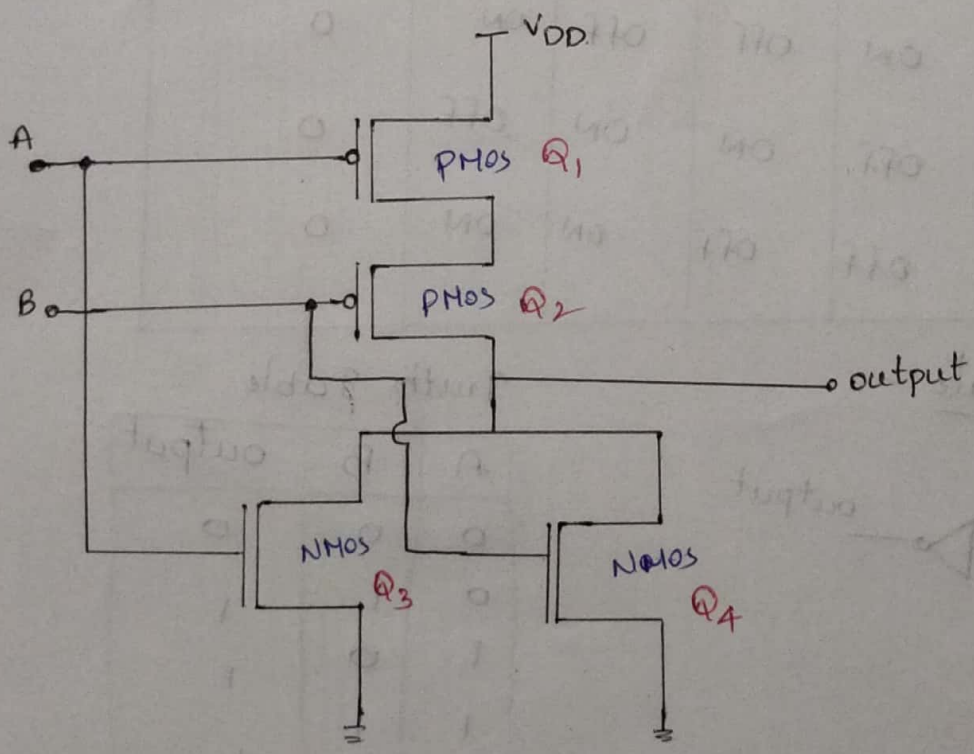
Here P-channel MOSFET is Q_1 and Q_2 are connected in series and N-channel MOSFETs Q_3 and Q_4 are connected in parallel.

Symbol of NOR gate:-

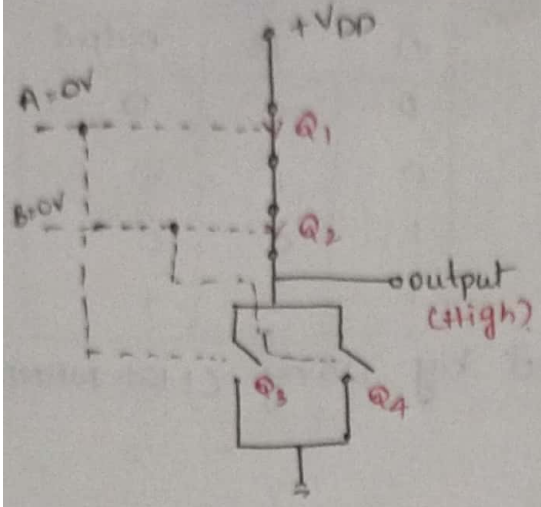


Truth Table of NOR gate:-

A	B	output
0	0	1
0	1	0
1	0	0
1	1	0



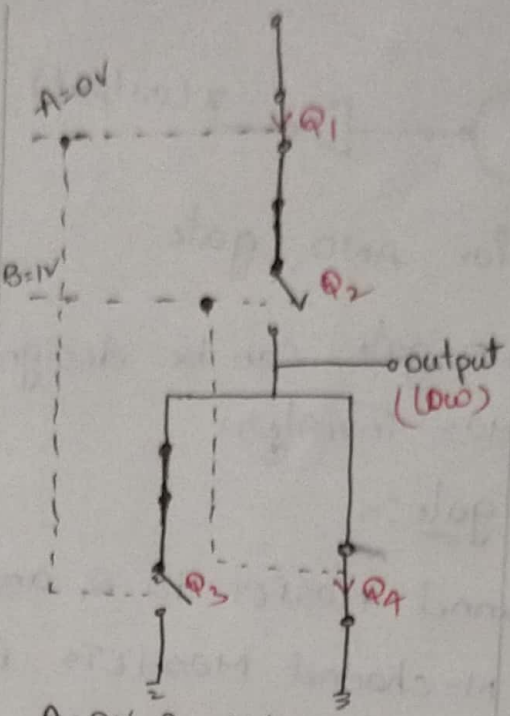
CMOS NOR Gate.



$A = B = 0V$

$V_{G_1} = V_{G_2} = -V_{DD}$

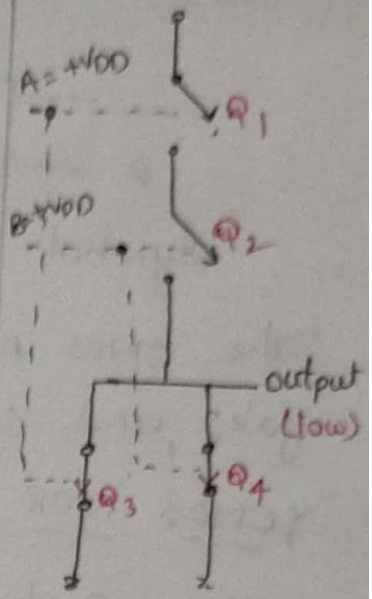
$V_{G_3} = V_{G_4} = 0V$



$A = 0V \quad B = +V_{DD}$

$V_{GS_1} = -V_{DD} \quad V_{GS_4} = V_{DD}$

$V_{GS_2} = V_{GS_3} = 0V$



$A = B = +V_{DD}$

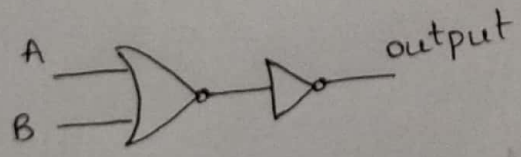
$V_{GS_1} = V_{GS_2} = 0$

$V_{GS_3} = V_{GS_4} = +V_{DD}$

* Truth Table :-

A	B	Q_1	Q_2	Q_3	Q_4	output
0	0	ON	ON	Off	Off	1
0	1	ON	Off	Off	ON	0
1	0	Off	ON	ON	Off	0
1	1	Off	Off	ON	ON	0

* CMOS OR Gate :-



Truth Table

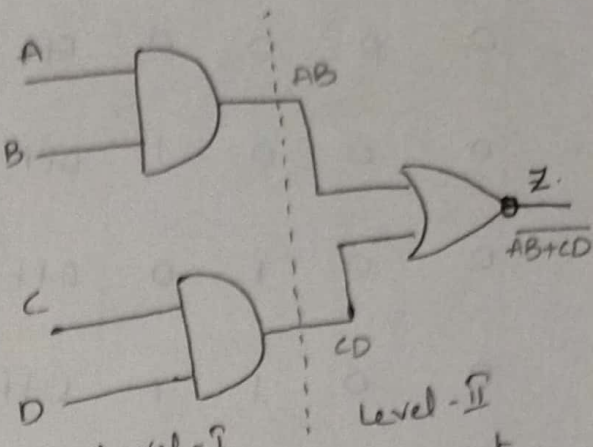
A	B	output
0	0	0
0	1	1
1	0	1
1	1	1

CMOS OR Gate is the combination of NOR gate or OR Gate.

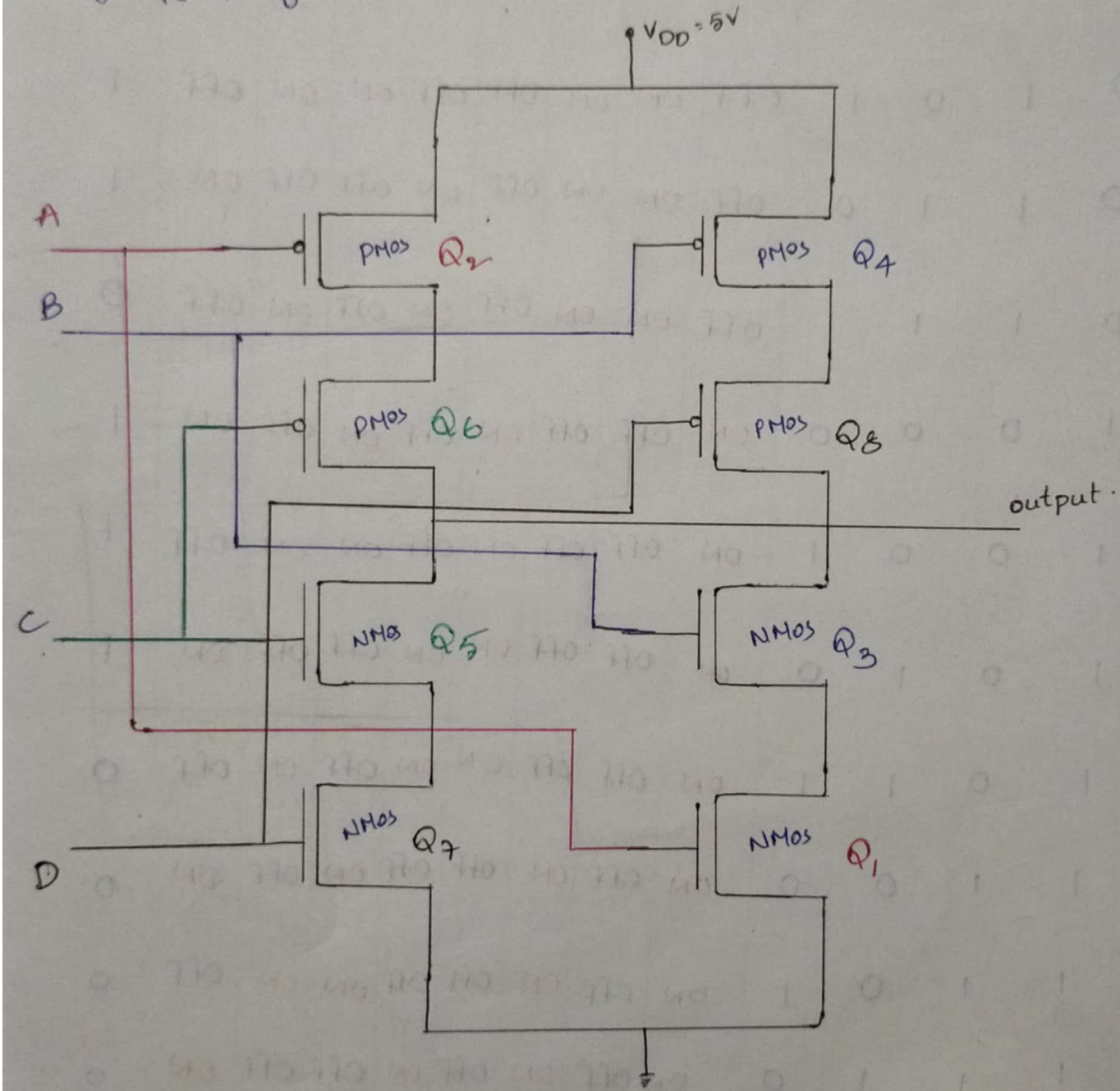
* CMOS AND-OR INVERT :-

The logic diagram of two wide, two input AND OR Invert [AOI] gate uses 2-input AND and NOR gates.

* There are two logic levels of gates. first level consists of two AND gates and second level consists of NOR gate.



AND-OR INVERT Gate



Two-input AOI gate.

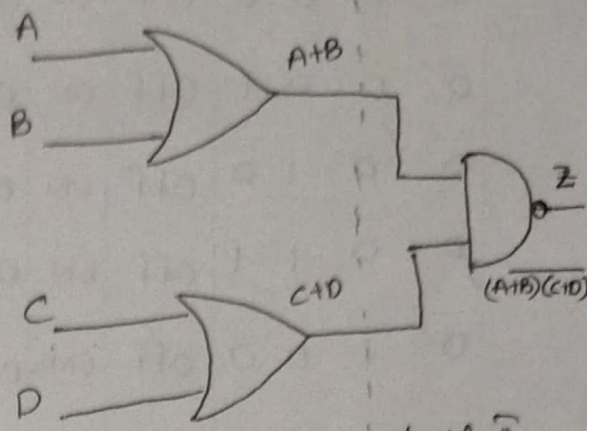
* Function Table - 2-Input AND-OR Invert gate.

A	B	C	D	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	output(z)
0	0	0	0	off	ON	off	ON	off	ON	off	ON	1
0	0	0	1	off	ON	off	ON	off	ON	ON	off	1
0	0	1	0	off	ON	off	ON	ON	off	off	ON	1
0	0	1	1	off	ON	off	ON	ON	off	ON	off	0
0	1	0	0	off	ON	ON	off	off	ON	off	ON	1
0	1	0	1	off	ON	ON	off	off	ON	ON	off	1
0	1	1	0	off	ON	ON	off	ON	off	off	ON	1
0	1	1	1	off	ON	ON	off	ON	off	ON	off	0
1	0	0	0	ON	off	off	ON	off	ON	off	ON	1
1	0	0	1	ON	off	off	ON	off	ON	ON	off	1
1	0	1	0	ON	off	off	ON	ON	off	off	ON	1
1	0	1	1	ON	off	off	ON	ON	off	ON	off	0
1	1	0	0	ON	off	ON	off	off	ON	off	ON	0
1	1	0	1	ON	off	ON	off	off	ON	ON	off	0
1	1	1	0	ON	off	ON	off	ON	off	off	ON	0
1	1	1	1	ON	off	ON	off	ON	off	ON	off	0

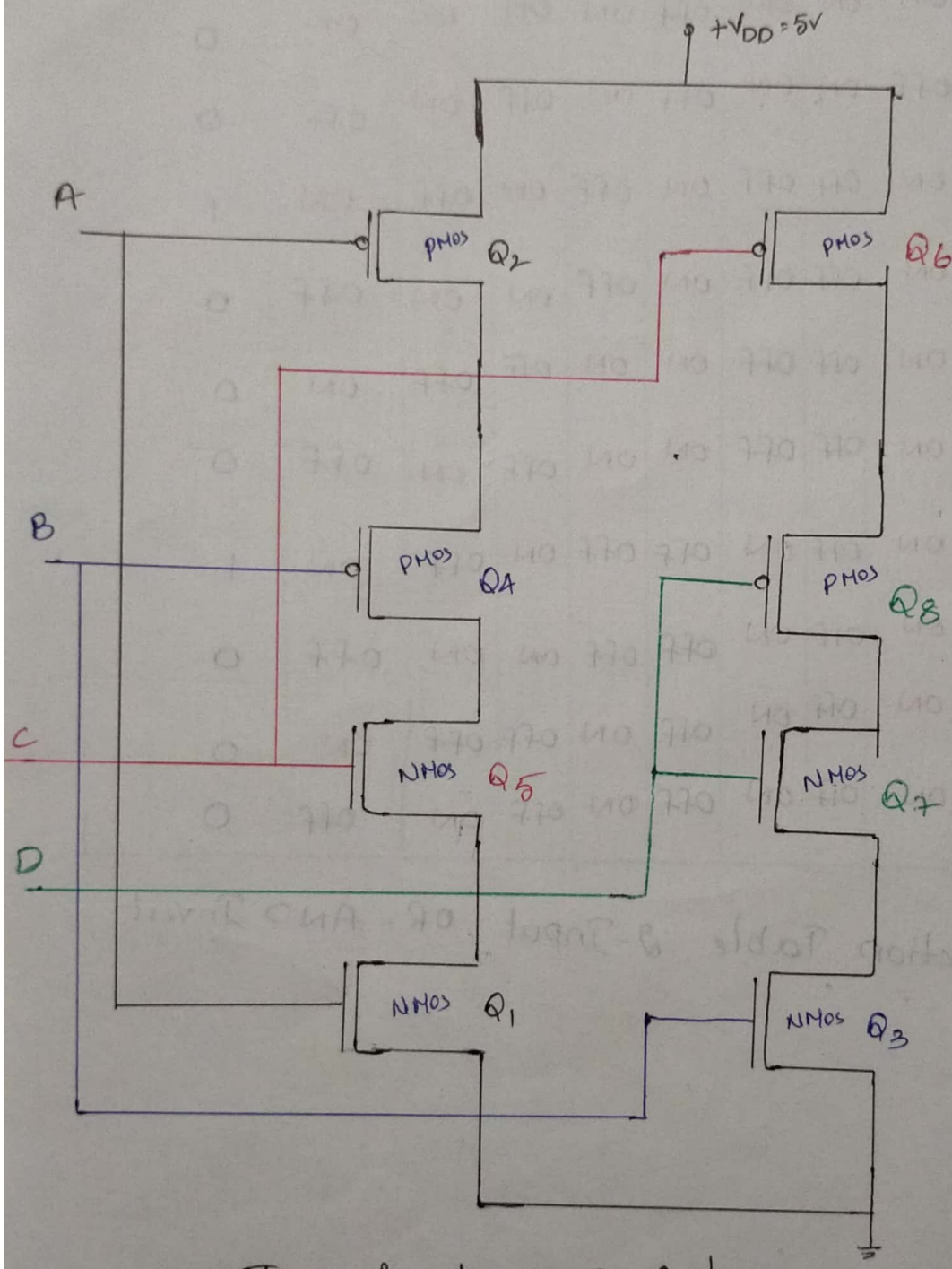
* CMOS OR AND INVERT Gates :-

The logic diagram of two-wide two input OR-AND INVERT [OAI] gate uses 2-input OR and NAND gates.

* There are two levels of gates first level consists of two OR gates and second level consists of NAND gate.



OR-AND INVERT Gate.



Two input OAI Gate.

A	B	C	D	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8	output
0	0	0	0	off	ON	off	ON	off	ON	off	ON	1
0	0	0	1	off	ON	off	ON	off	ON	ON	off	1
0	0	1	0	off	ON	off	ON	ON	off	off	ON	1
0	0	1	1	off	ON	off	ON	ON	off	ON	off	1
0	1	0	0	off	ON	ON	off	off	ON	off	ON	1
0	1	0	1	off	ON	ON	off	off	ON	ON	off	0
0	1	1	0	off	ON	ON	off	ON	off	off	ON	0
0	1	1	1	off	ON	ON	off	ON	off	ON	off	0
1	0	0	0	ON	off	off	ON	off	ON	off	ON	1
1	0	0	1	ON	off	off	ON	off	ON	ON	off	0
1	0	1	0	ON	off	off	ON	ON	off	off	ON	0
1	0	1	1	ON	off	off	ON	ON	off	ON	off	0
1	1	0	0	ON	off	ON	off	off	ON	off	ON	1
1	1	0	1	ON	off	ON	off	off	ON	ON	off	0
1	1	1	0	ON	off	ON	off	ON	off	off	ON	0
1	1	1	1	ON	off	ON	off	ON	off	ON	off	0

Function Table 2-Input OR-AND Invert gate.

* Implementation of any function using CMOS logic :-

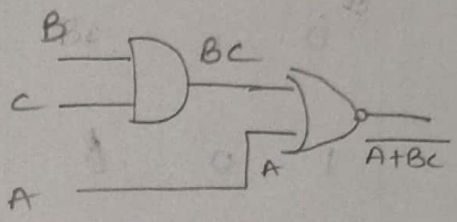
$f = \overline{A+(B\cdot C)}$

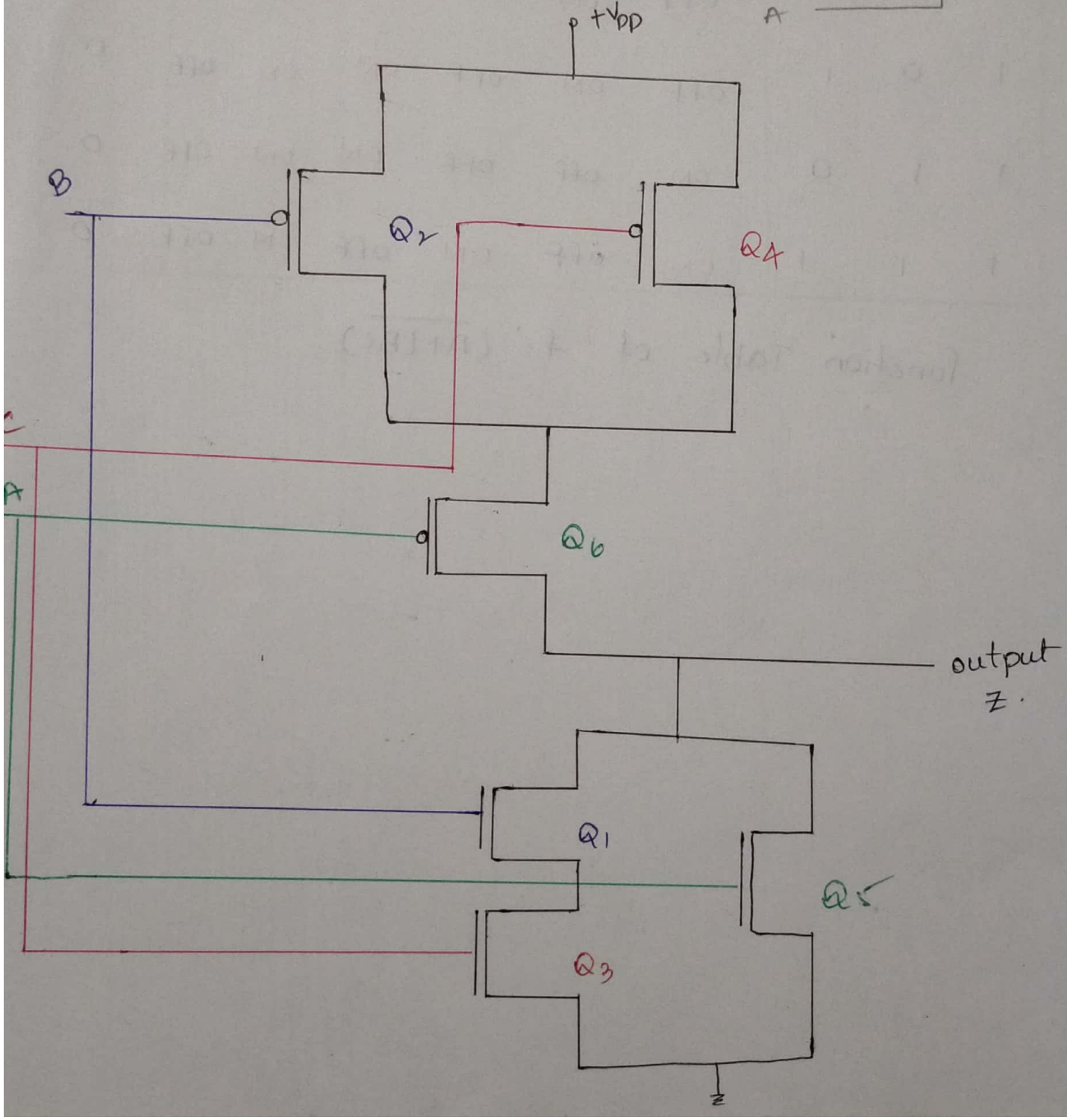
Given $f = \overline{[A+(B\cdot C)]}$

Note :- AOI $[\overline{AB+CD}]$ [It is like SOP (Sum of products)]

OAI $[\overline{(A+B)(C+D)}]$ [It is like POS [product of sum]].

Given $f = \overline{A+(BC)}$ [~~It is in~~





A	B	C	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	output
0	0	0	off	ON	off	ON	off	ON	1
0	0	1	off	ON	ON	off	off	ON	1
0	1	0	ON	off	off	ON	off	ON	1
0	1	1	ON	off	ON	off	off	ON	0
1	0	0	off	ON	off	ON	ON	off	0
1	0	1	off	ON	off	ON	ON	off	0
1	1	0	ON	off	off	ON	ON	off	0
1	1	1	ON	off	ON	off	ON	off	0

- function Table of $f = \overline{(A + (BC)}$

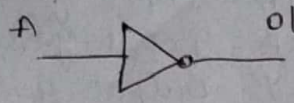
* Combinational circuits using TTL 74xx ICs :-

• Study of Logic gates using 74xx ICs :-

- Basic gates are AND, OR, NOT.
- Universal gates are NAND, NOR.

The basic gates and universal gates are studied by using IC 74xx.

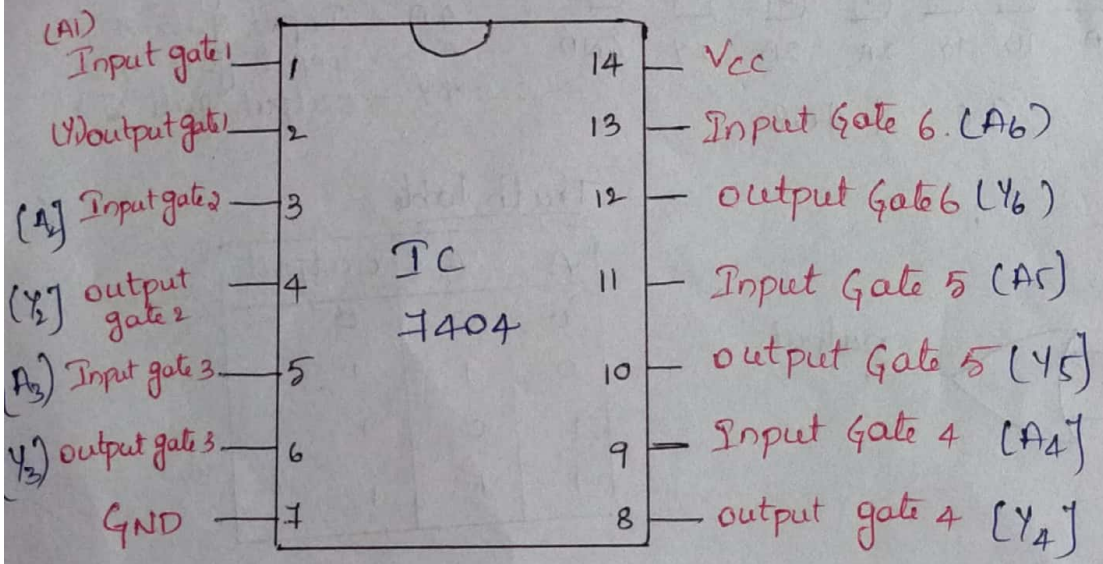
• NOT gate :-



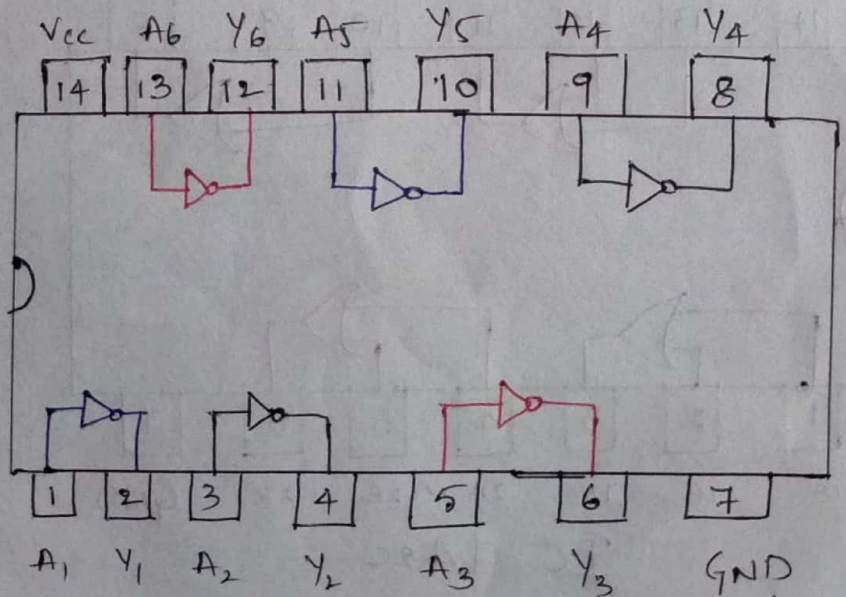
Truth Table :-

A	O|P
0	1
1	0

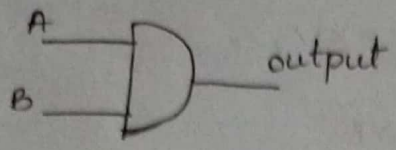
• NOT gate by using IC 7404.



Pin Configuration of IC 7404.



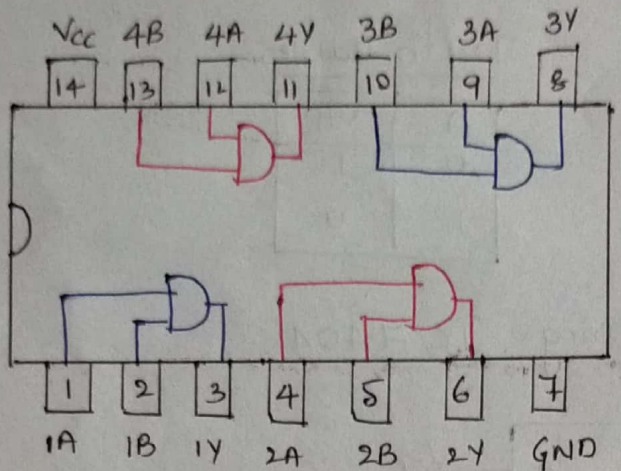
* AND gate:



Truth Table

A	B	output
0	0	0
0	1	0
1	0	0
1	1	1

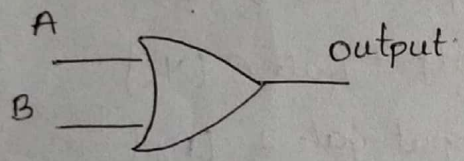
AND gate by using IC 7408.



IC 7408

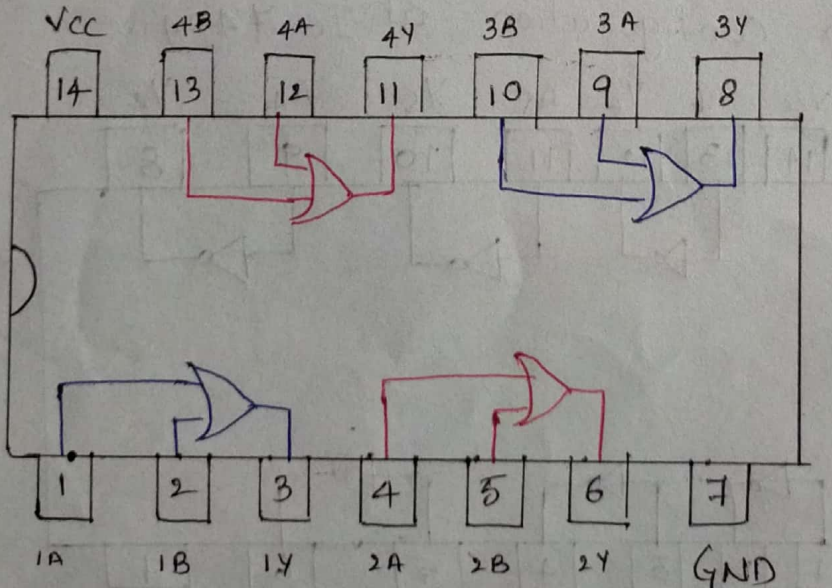
1A - Input gate 1
1B - Input gate 1
1Y - output gate 1
2A - Input gate 2
2B - Input gate 2
2Y - output gate 2
3A - Input gate 3
3B - Input gate 3
3Y - output gate 3
4A - Input gate 4
4B - Input gate 4
4Y - output gate 5.

* OR Gate:-



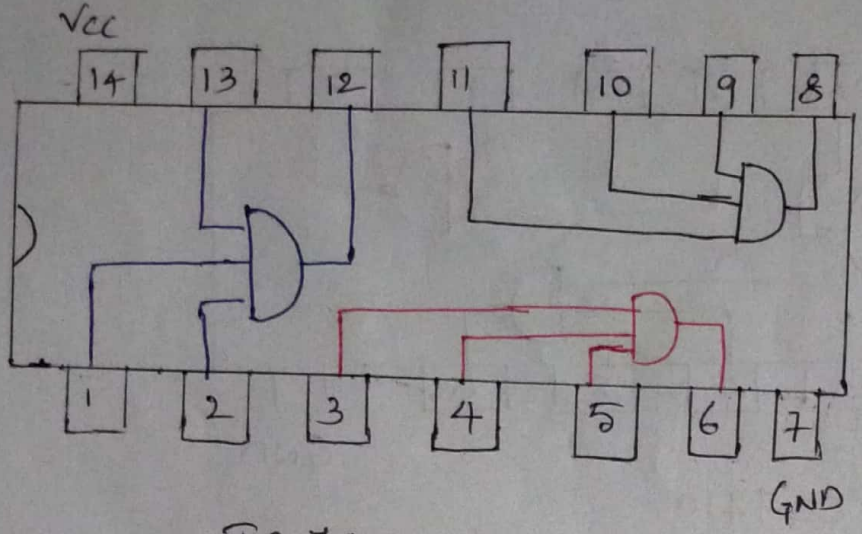
Truth Table:-

A	B	output
0	0	0
0	1	1
1	0	1
1	1	1



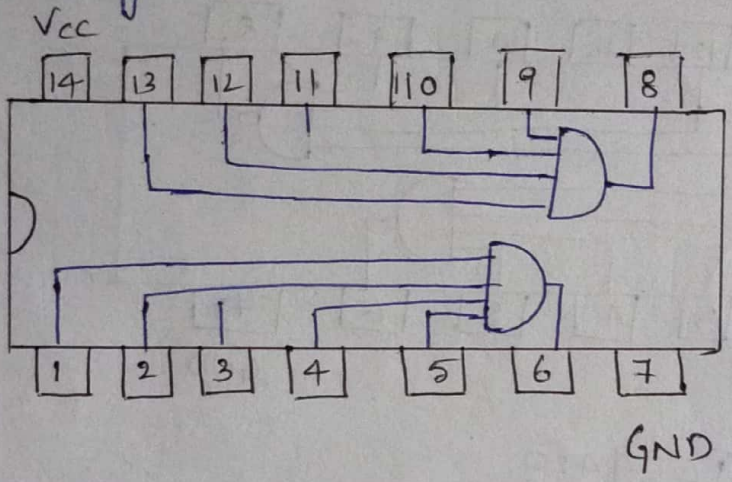
IC 7420.

3-Input AND gate:



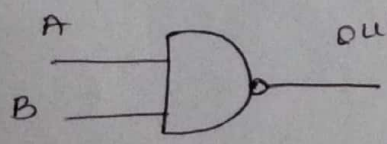
IC 7411

4-input AND gate.



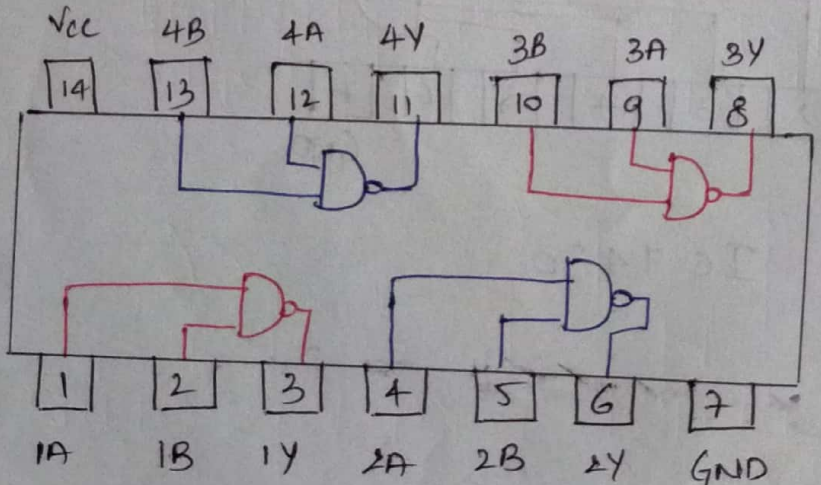
IC 7421

* NAND gate:-



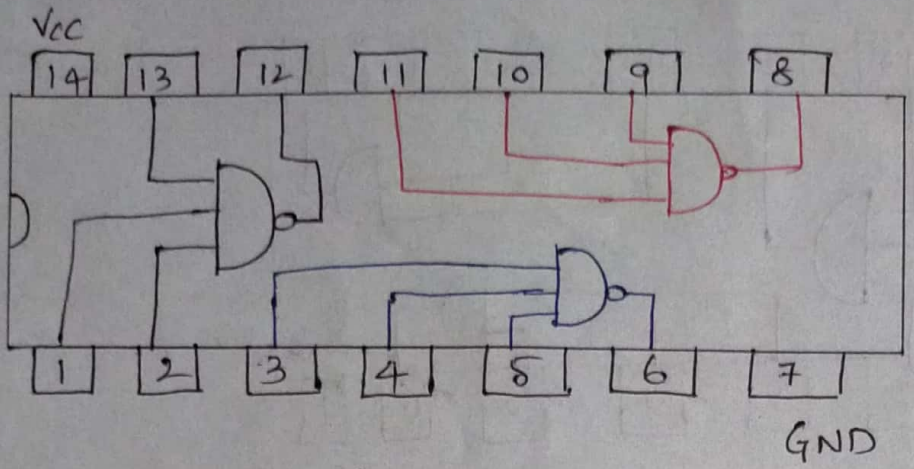
Truth Table.

A	B	output
0	0	1
0	1	1
1	0	1
1	1	0



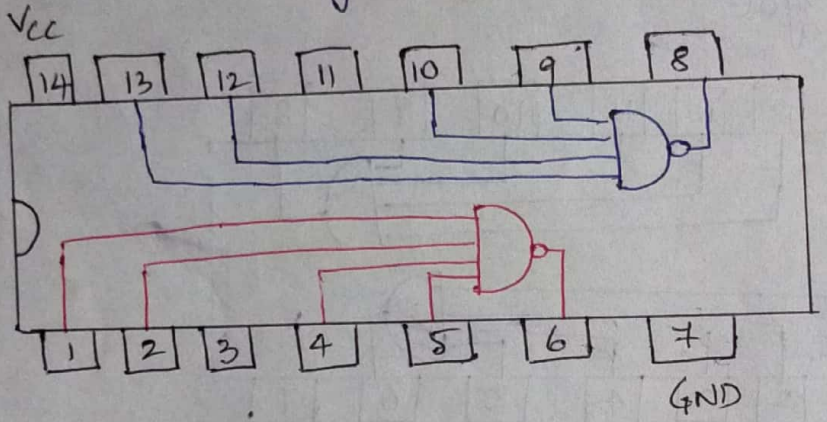
IC 7400

3-input NAND Gate:



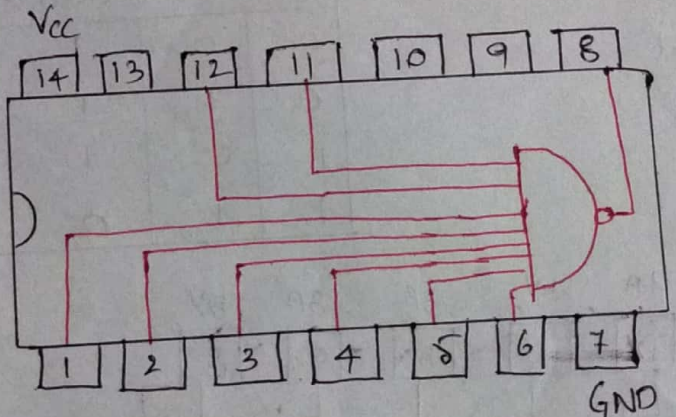
IC 7410

4-Input NAND gate



IC 7420

8-input NAND gate.

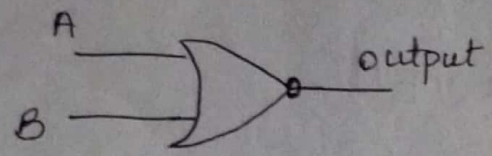


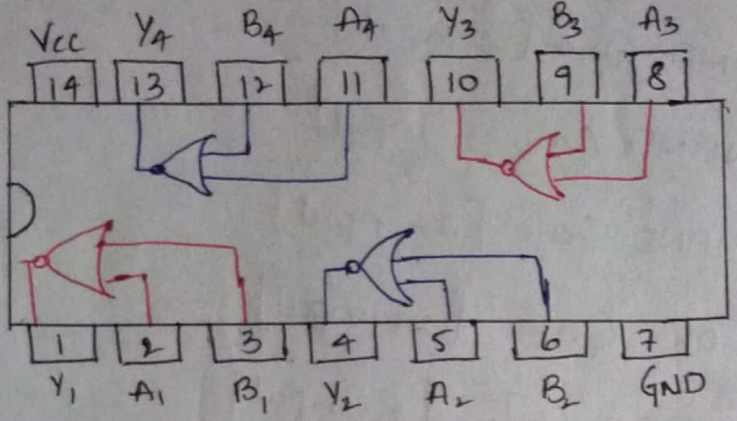
IC 7430.

* NOR Gate :-

Truth Table :-

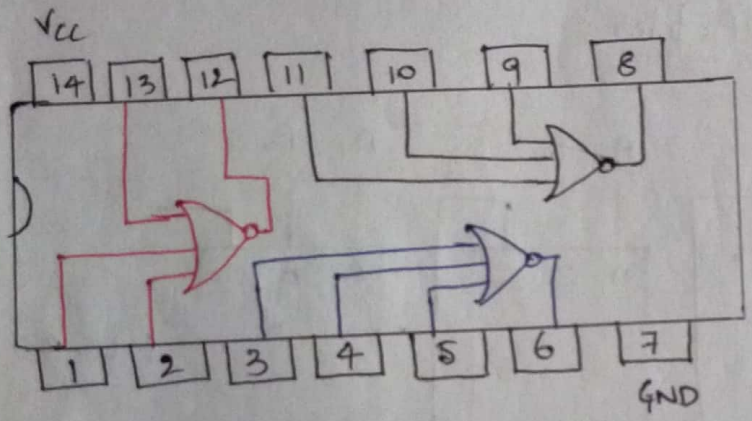
A	B	output
0	0	1
0	1	0
1	0	0
1	1	0





IC 7402.

8-input NOR Gate.

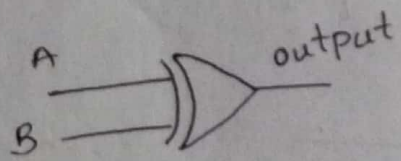


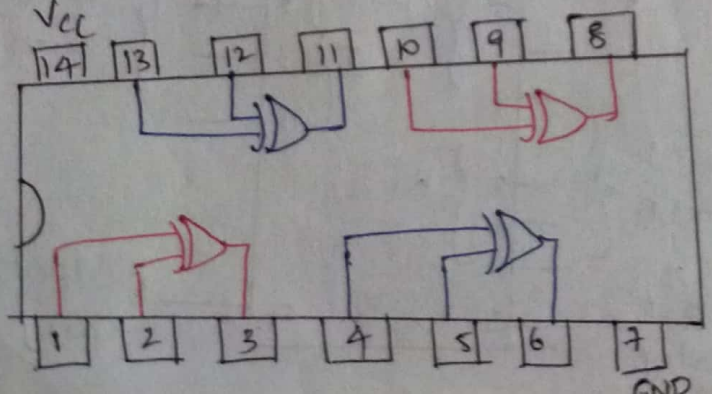
IC 7427.

* XOR Gate :-

Truth table :-

A	B	output
0	0	0
0	1	1
1	0	1
1	1	0

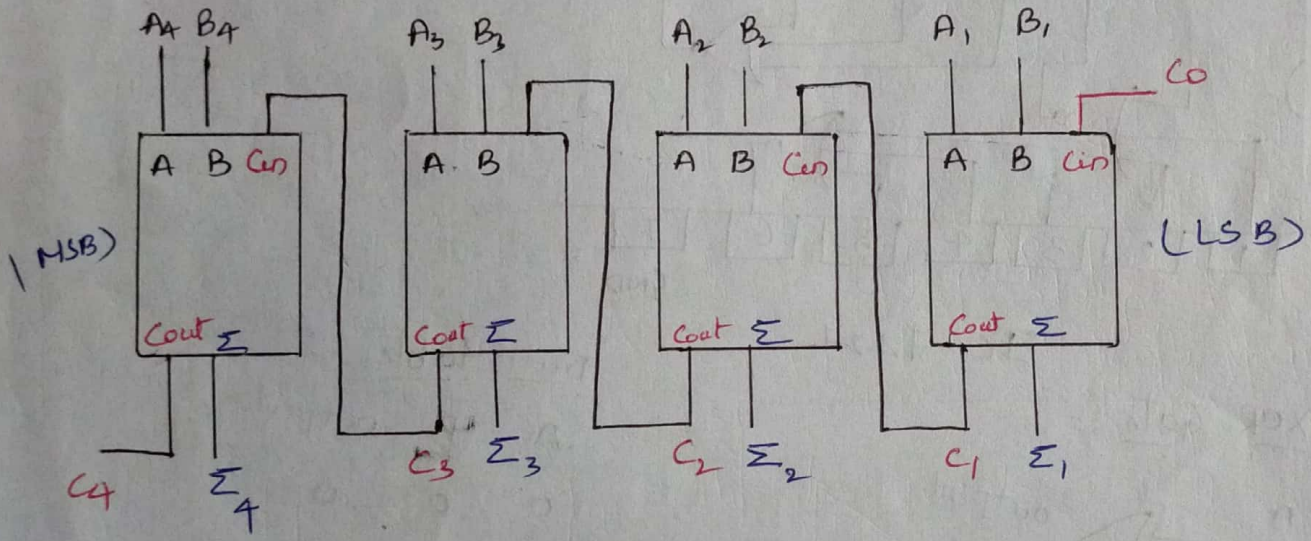




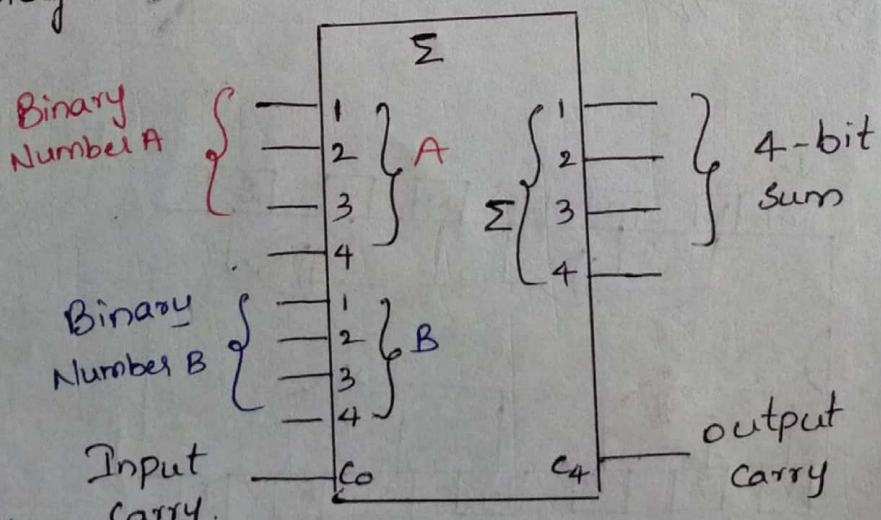
IC 7486.

IC Number	Specification
IC 7400	NAND Gate [2-input]
IC 7402	NOR Gate [2-input]
IC 7404	NOT Gate
IC 7408	AND Gate [2-input]
IC 7410	NAND Gate [3-input]
IC 7420	NAND Gate [4-input]
IC 7432	OR Gate [2-input]
IC 7486	X OR Gate [2-input]

* Four-Bit Parallel Adder :-

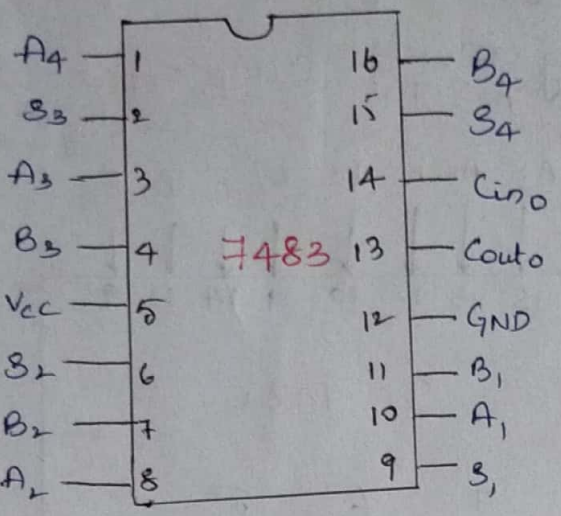


Block Diagram:



(b) logic symbol.

* A basic 4-bit parallel adder is implemented with four full-adder stages. The carry output of each adder is connected to to the carry input of the next higher-order adder. These are called internal carries.

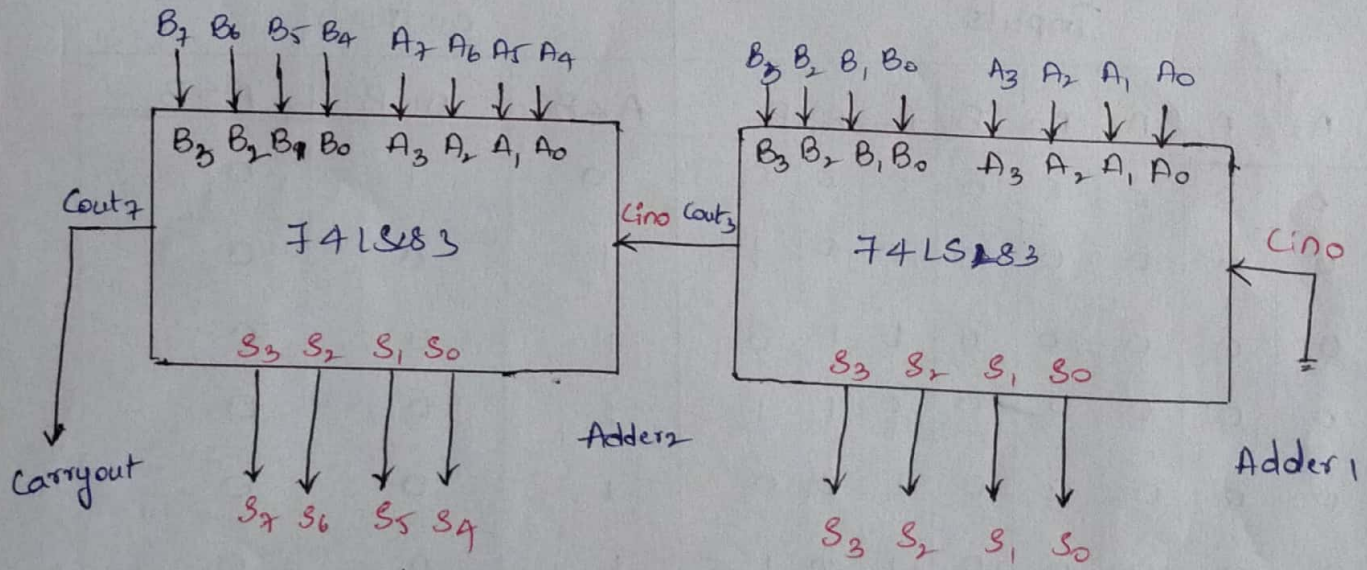


Pin diagram of IC 7483

C_{n-1}	A_n	B_n	sum(S_n)	C_n
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Truth Table for each stage of a 4-bit parallel adder.

* 8-bit parallel adder using two IC 7483



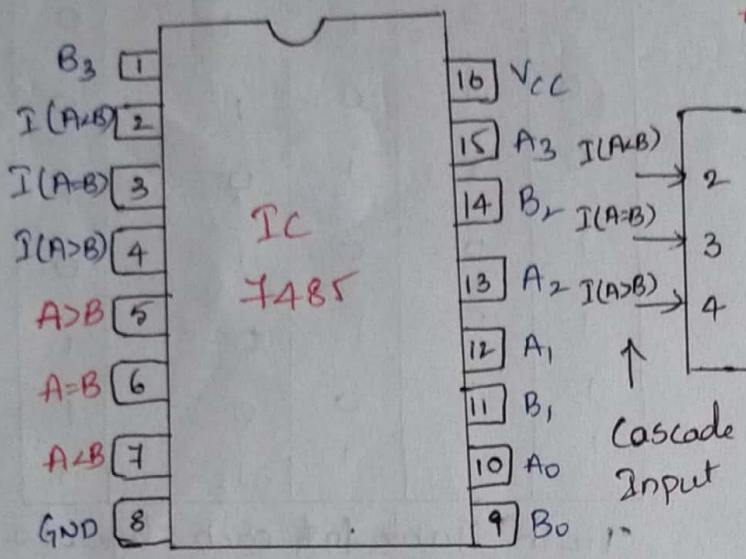
Cascading of two IC 7483s

The 4-bit parallel adder can be expanded to handle the addition of two 8-bit numbers by using two 4-bit adders. The carry input of the low order adder (C_0) is connected to ground because there is no carry into the least

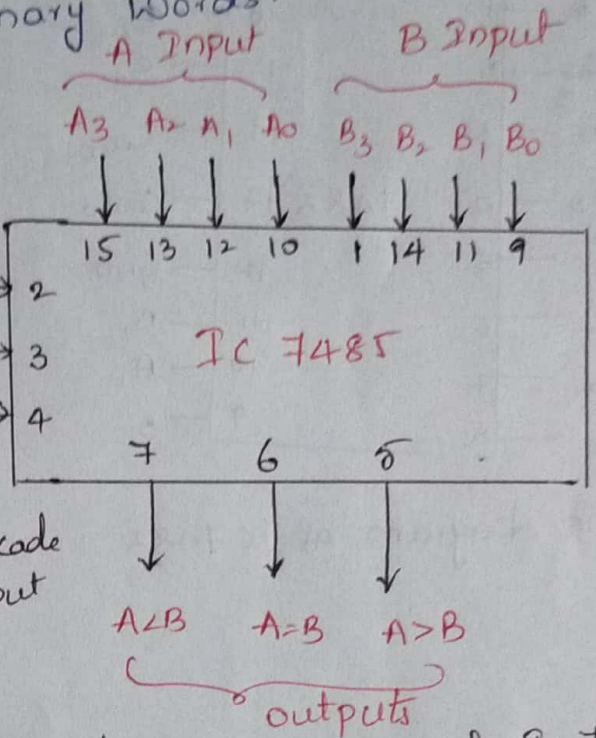
significant bit position, and the carry output of the low-order adder is connected to the carry input of the high-order adder. This process is known as cascading.

* 4-Bit Comparator :- [Ic 7485]

Ic 7485 is a 4-bit comparator. It can be used to compare two 4-bit binary words.



Pin diagram Ic 7485



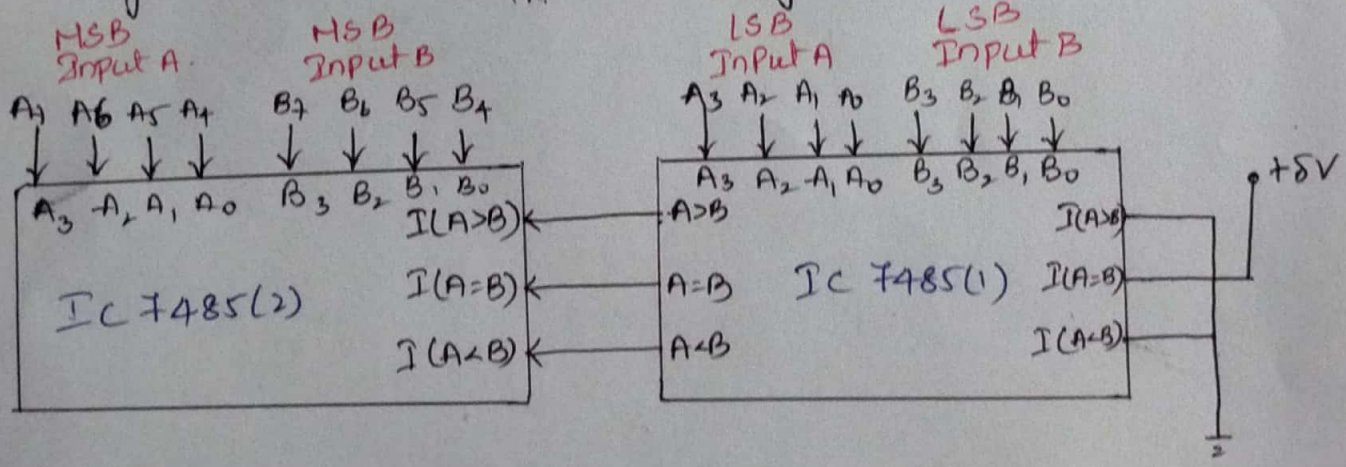
Logic Diagram of Ic 7485

Inputs								outputs		
A_3	A_2	A_1	A_0	B_3	B_2	B_1	B_0	A<B	A=B	A>B
0	0	0	0	0	0	0	0	0	1	0
0	0	0	0	0	0	0	1	1	0	0
0	0	0	0	0	0	1	0	1	0	0
0	0	0	0	0	0	1	1	1	0	0
0	0	0	0	0	1	0	0	1	0	0
0	0	0	0	0	1	0	1	1	0	0
0	0	0	0	0	1	1	0	1	0	0
0	0	0	0	0	1	1	1	1	0	0
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	1	0	0	1	1	0	0
0	0	0	0	1	0	1	0	1	0	0

Truth Table of 2-Bit Comparator.

Inputs				outputs		
A_1	A_0	B_1	B_0	A<B	A=B	A>B
0	0	0	0	0	1	0
0	0	0	1	1	0	0
0	0	1	0	1	0	0
0	0	1	1	1	0	0
0	1	0	0	0	0	1
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	1	0	0
1	0	0	0	0	0	1
1	0	0	1	0	0	1
1	0	1	0	0	1	0
1	0	1	1	1	0	0
1	1	0	0	0	0	1
1	1	0	1	0	0	1
1	1	1	0	0	0	1
1	1	1	1	0	1	0

* Design an 8-bit Comparator using two 7485 IC's.



*Truth Table of 4-Bit Comparator

Comparing Inputs							Cascading Inputs			Outputs		
A_3	B_3	A_2	B_2	A_1	B_1	A_0 B_0	A>B	A<B	A=B	A>B	A<B	A=B
$A_3 > B_3$		X		X		X	X	X	X	1	0	0
$A_3 < B_3$		X		X		X	X	X	X	0	1	0
$A_3 = B_3$		$A_2 > B_2$		X		X	X	X	X	1	0	0
$A_3 = B_3$		$A_2 < B_2$		X		X	X	X	X	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 > B_1$		X	X	X	X	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 < B_1$		X	X	X	X	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 > B_0$	X	X	X	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 < B_0$	X	X	X	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$	1	0	0	1	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$	0	1	0	0	1	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$	0	0	1	0	0	1
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$	X	X	1	0	0	1
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$	1	1	0	0	0	0
$A_3 = B_3$		$A_2 = B_2$		$A_1 = B_1$		$A_0 = B_0$	0	0	0	1	1	0

* Decoder :-

A decoder is a multiple input, multiple output logic ckt which converts coded inputs into coded outputs.

The input code generally has a fewer bits than the o/p code. i.e n inputs 2^n outputs.

It is one-to-one mapping circuit. The general structure of the decoder is :

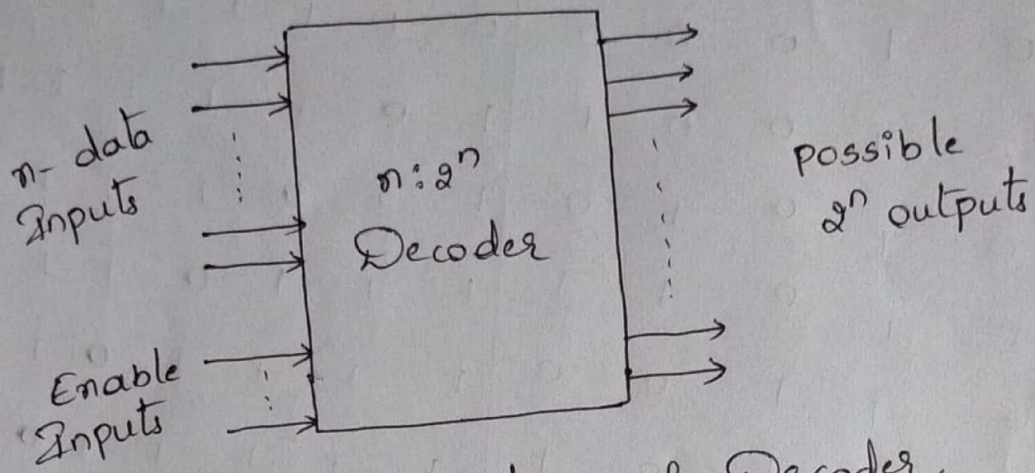
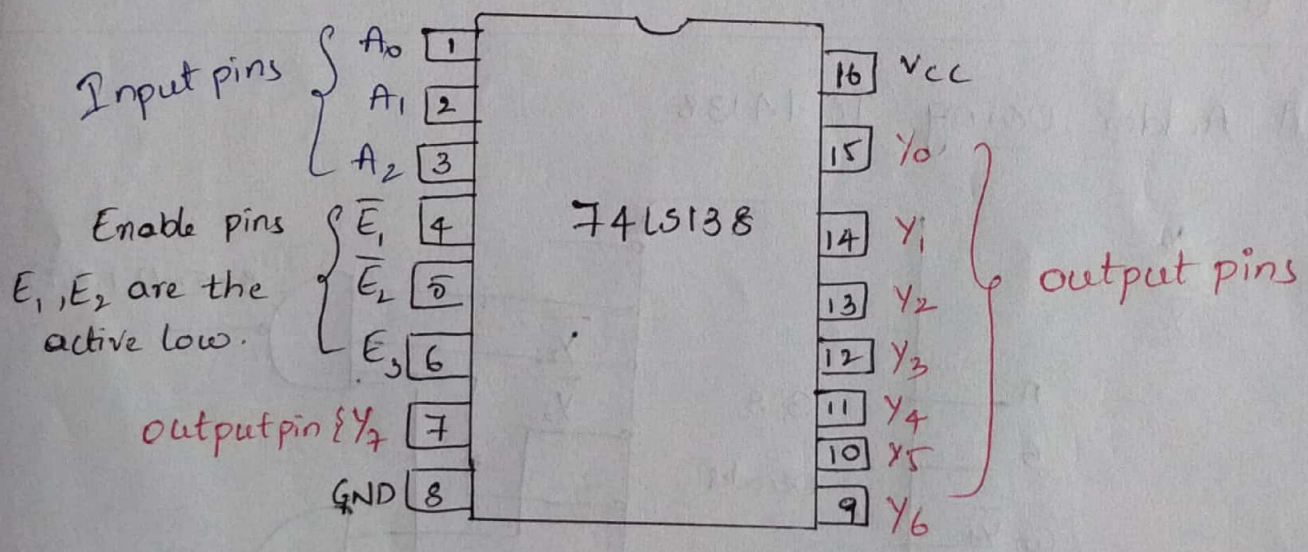


fig: General structure of Decoder.

* 3×8 Decoder using IC 74138

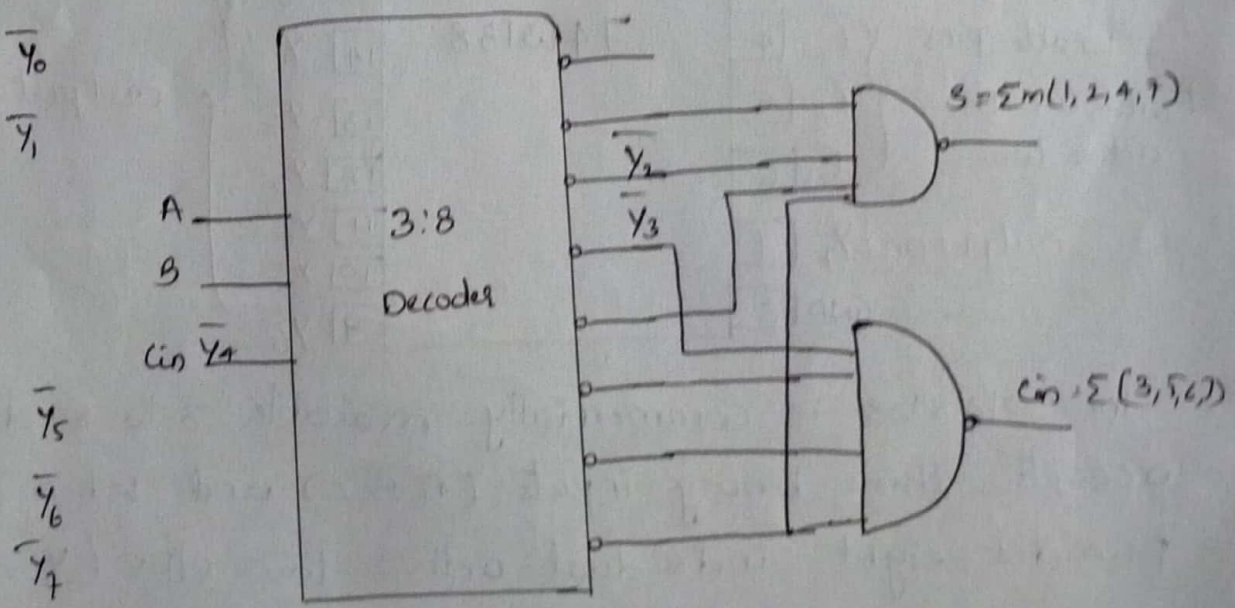


The 74x138 is commercially available 3-to-8 decoder. It accepts three binary inputs (A, B, C) and when enabled, provides eight individual active low o/p's ($Y_0 - Y_7$).

* Truth Table :-

INPUT						OUTPUTS							
E_1	E_2	E_3	A_0	A_1	A_2	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$
1	x	x	x	x	x	1	1	1	1	1	1	1	1
x	1	x	x	x	x	1	1	1	1	1	1	1	1
x	x	0	x	x	x	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

Full Adder using IC 74138



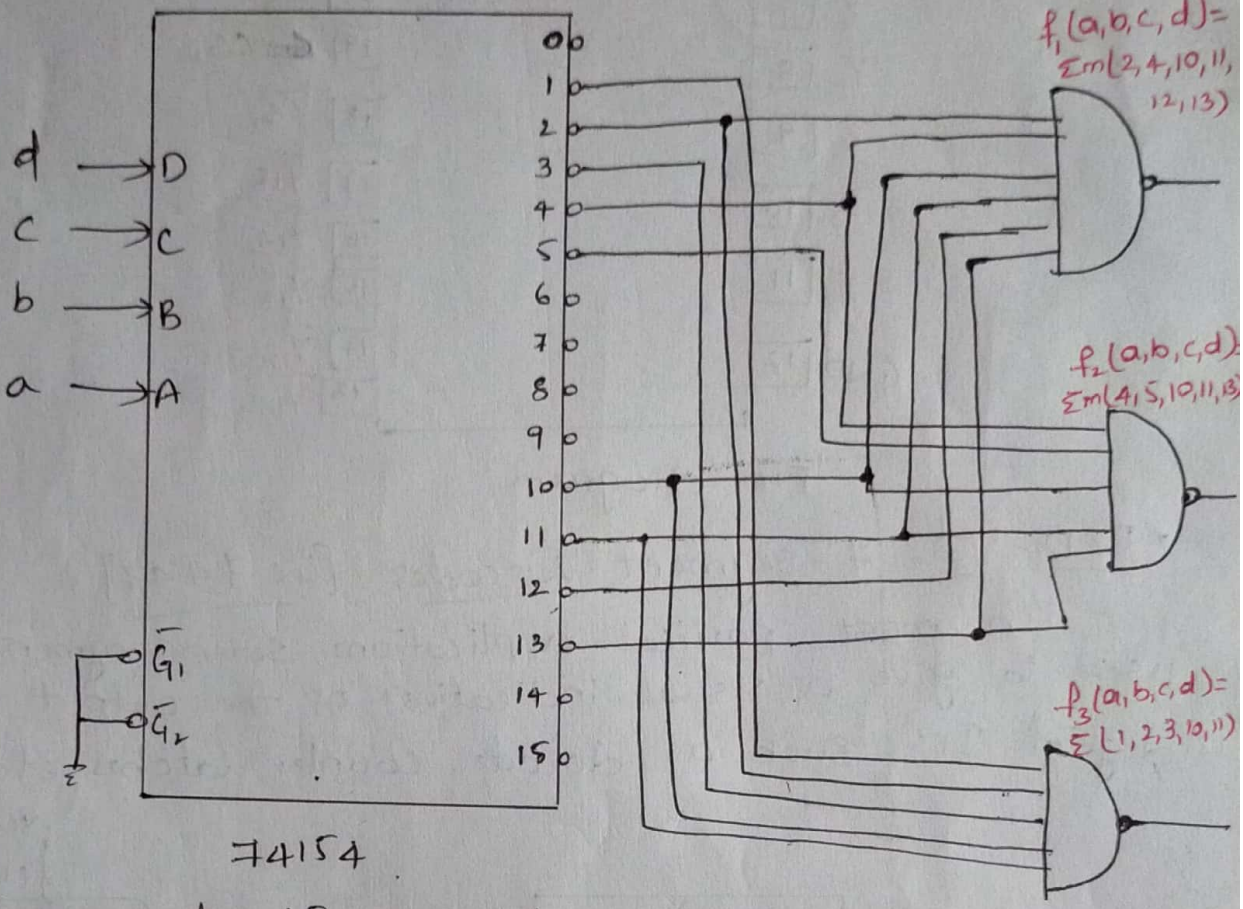
* Implementation of Multiple functions.

$f_1(a,b,c,d) = \Sigma m(2,4,10,11,12,13)$

$f_2(a,b,c,d) = \Sigma m(4,5,10,11,13)$

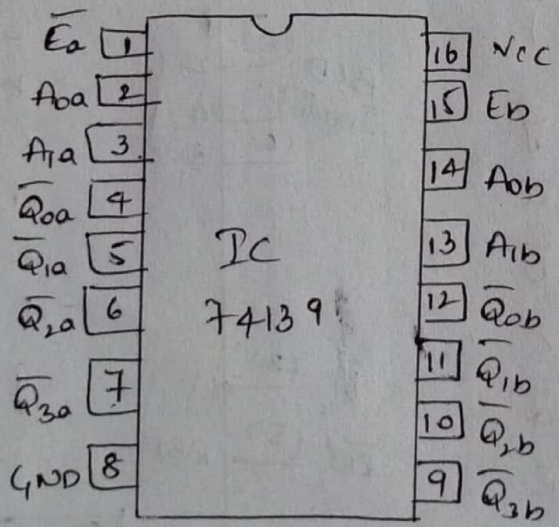
$f_3(a,b,c,d) = \Sigma m(1,2,3,10,11)$

The realization of set of functions with a 74154 decoder



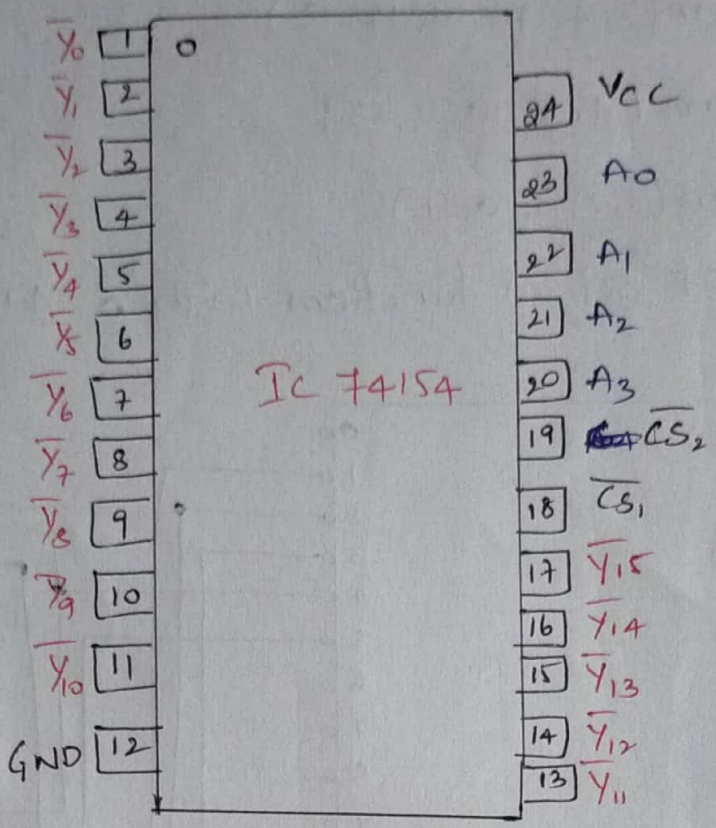
74154

* Dual 2×4 Decoder (IC 74139)



Inputs			outputs			
$\bar{G}$	Select					
	B	A	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

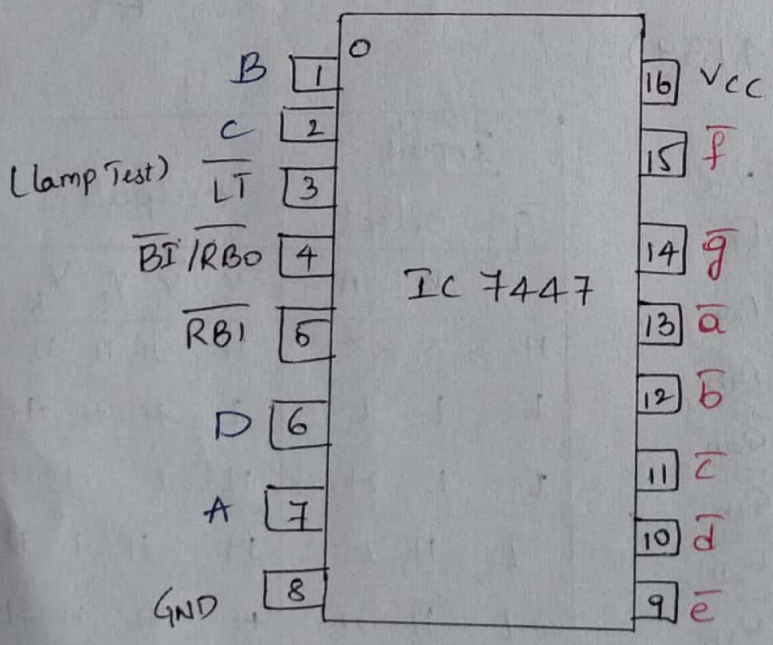
* IC 74154 4-to-16 Decoder :-



Pin diagram

* BCD-to-7-Segment Decoder [IC 7447]

In most partical applications, seven segment display are used to give a visual indication of the output states of digital ICs such as decade counter, latches etc.



(a) PIN Diagram.

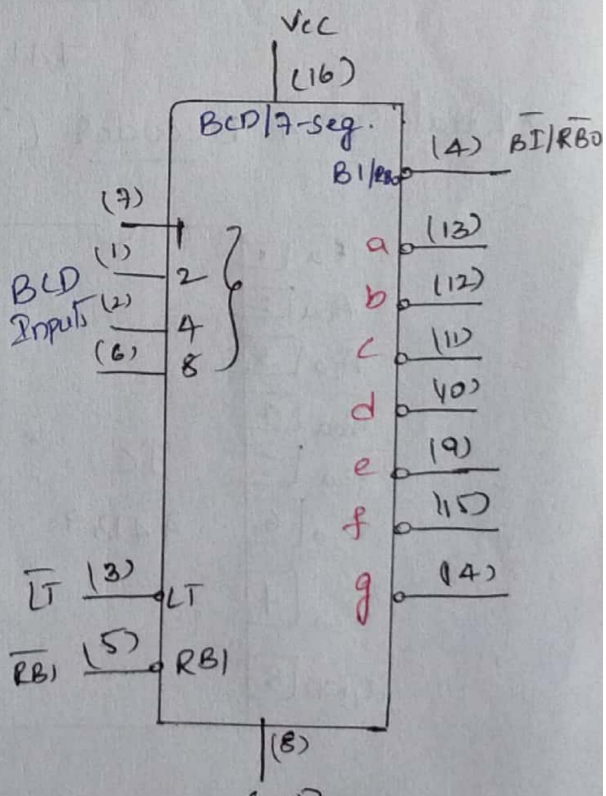
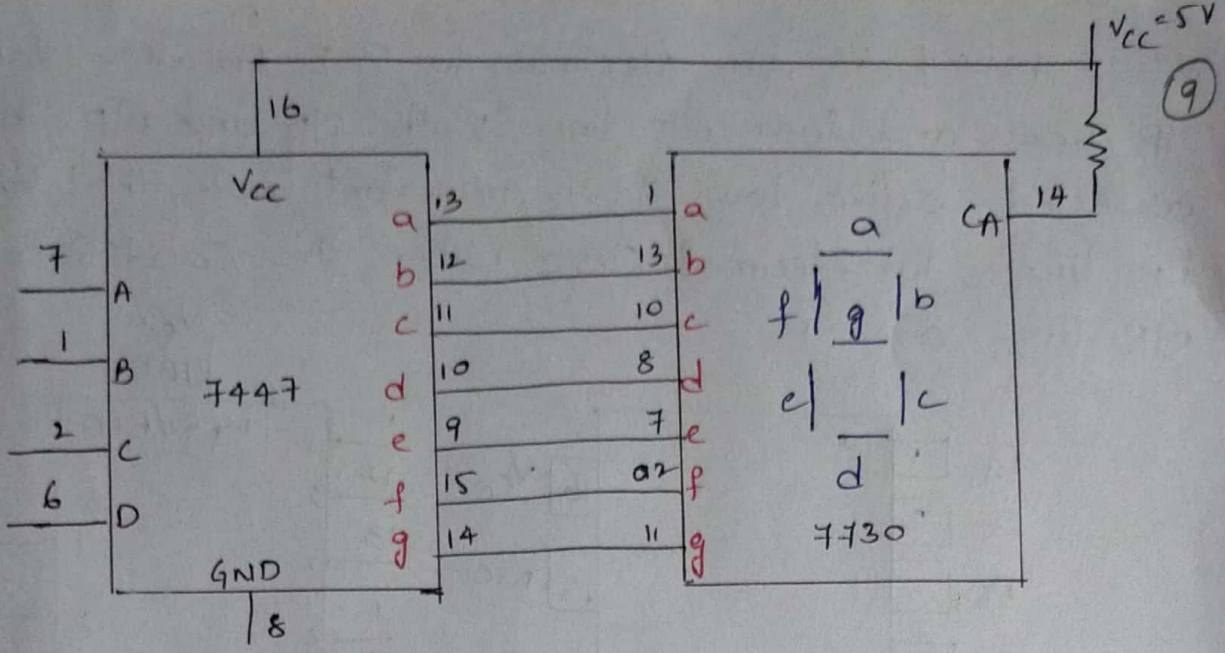


fig: logic Diagram



* Truth Table:-

BCD Inputs				output logic levels from 7447 to 7-segment							Decimal No. Display
D	C	B	A	a	b	c	d	e	f	g	
0	0	0	0	0	0	0	0	0	0	1	0
0	0	0	1	1	0	0	1	1	1	1	1
0	0	1	0	0	0	1	0	0	1	0	2
0	0	1	1	0	0	0	0	1	1	0	3
0	1	0	0	1	0	0	1	1	0	0	4
0	1	0	1	0	1	0	0	1	0	0	5
0	1	1	0	1	1	0	0	0	0	0	6
0	1	1	1	0	0	0	1	1	1	1	7
1	0	0	0	0	0	0	0	0	0	0	8
1	0	0	1	0	0	0	1	1	0	0	9

* Encoder:- An encoder is a digital ckt that performs the inverse operation of a decoder. An encoder has 2^n i/p lines and n o/p lines.

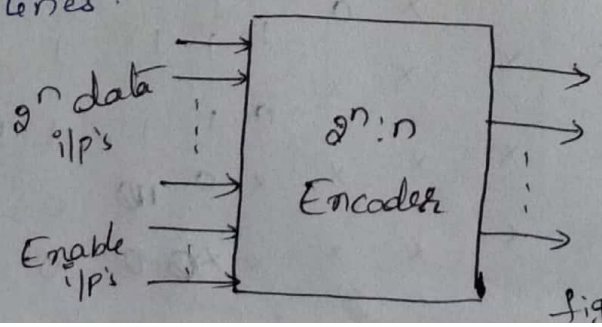
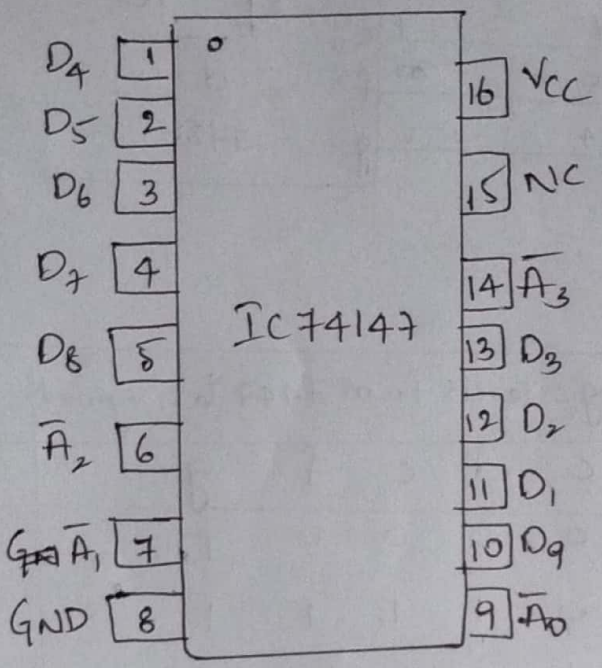
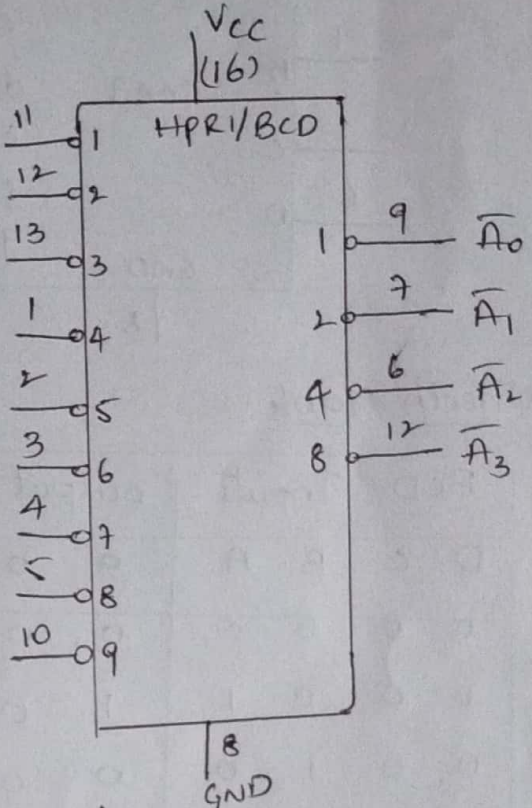


fig: General structure of Encoder.

*IC 74147 is for Decimal to BCD Encoder. It has nine i/p lines and four o/p lines Both i/p and o/p lines are asserted active low. It is important note that there is no i/p lines for decimal zero. when this condition occurs, all o/p lines are 1.



pin diagram



logic diagram

Decimal value	Inputs									outputs			
	1	2	3	4	5	6	7	8	9	D	C	B	A
0	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	0
2	x	0	1	1	1	1	1	1	1	1	1	0	1
3	x	x	0	1	1	1	1	1	1	1	1	0	0
4	x	x	x	0	1	1	1	1	1	1	0	1	1
5	x	x	x	x	0	1	1	1	1	1	0	1	0
6	x	x	x	x	x	0	1	1	1	1	0	0	1
7	x	x	x	x	x	x	0	1	1	1	0	0	0
8	x	x	x	x	x	x	x	0	1	0	1	1	1
9	x	x	x	x	x	x	x	x	0	0	1	1	0

*Multiplexers :-

Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single output line.

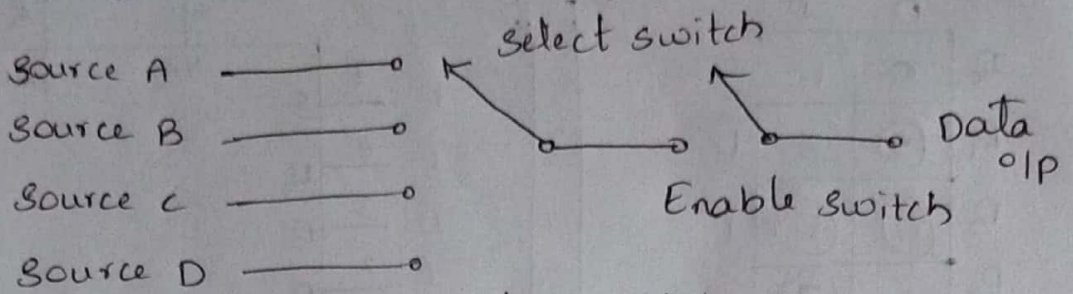
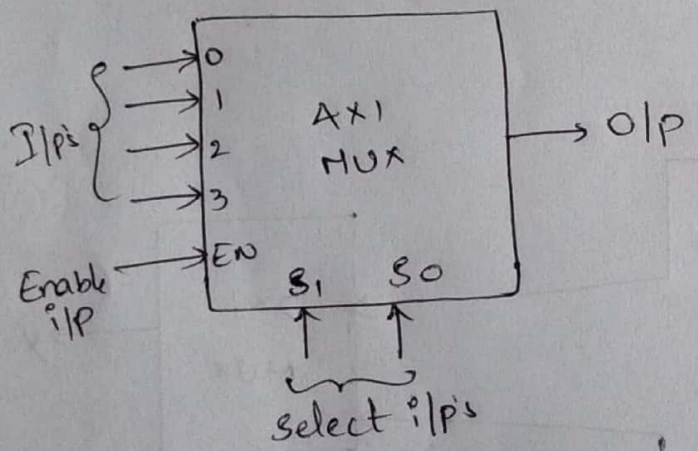


fig: Analog selector switch

The basic Multiplexer has several data i/p lines and single o/p line. The selection of a particular i/p line is controlled by a set of selection lines.

Normally there are 2^n i/p lines and n selection lines whose bit combinations determine which i/p is selected. Therefore multiplexer is "many to one".

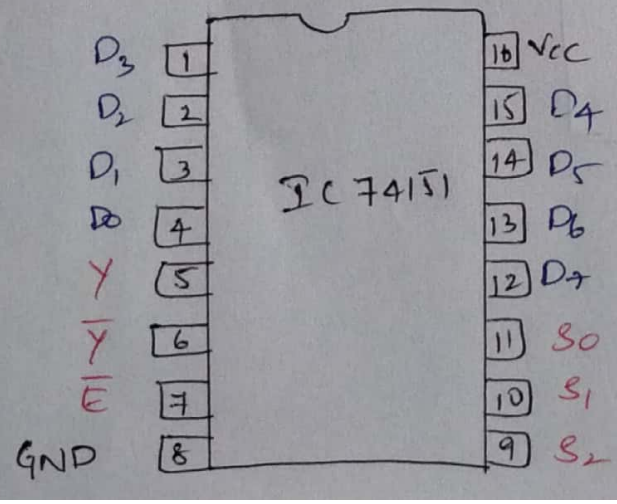


Logic symbol.

Truth Table :

S_1	S_0	Y
0	0	D_0
0	1	D_1
1	0	D_2
1	1	D_3

* 8x1 Multiplexer using IC 74151

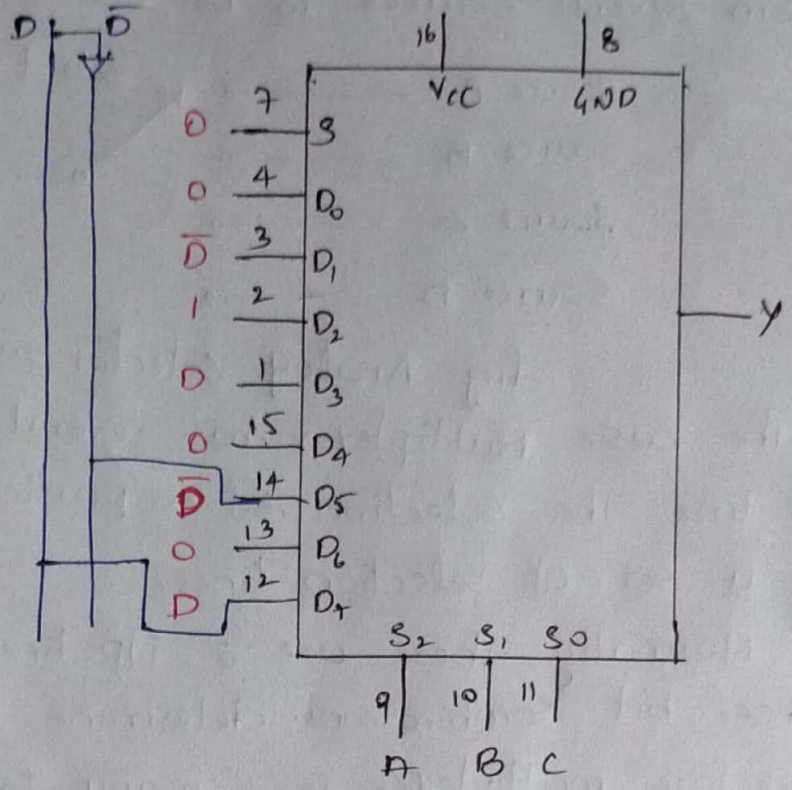


Enable	select i/p's			output
E	S_2	S_1	S_0	Y
0	x	x	x	0
1	0	0	0	D_0
1	0	0	1	D_1
1	0	1	0	D_2
1	0	1	1	D_3
1	1	0	0	D_4
1	1	0	1	D_5
1	1	1	0	D_6
1	1	1	1	D_7

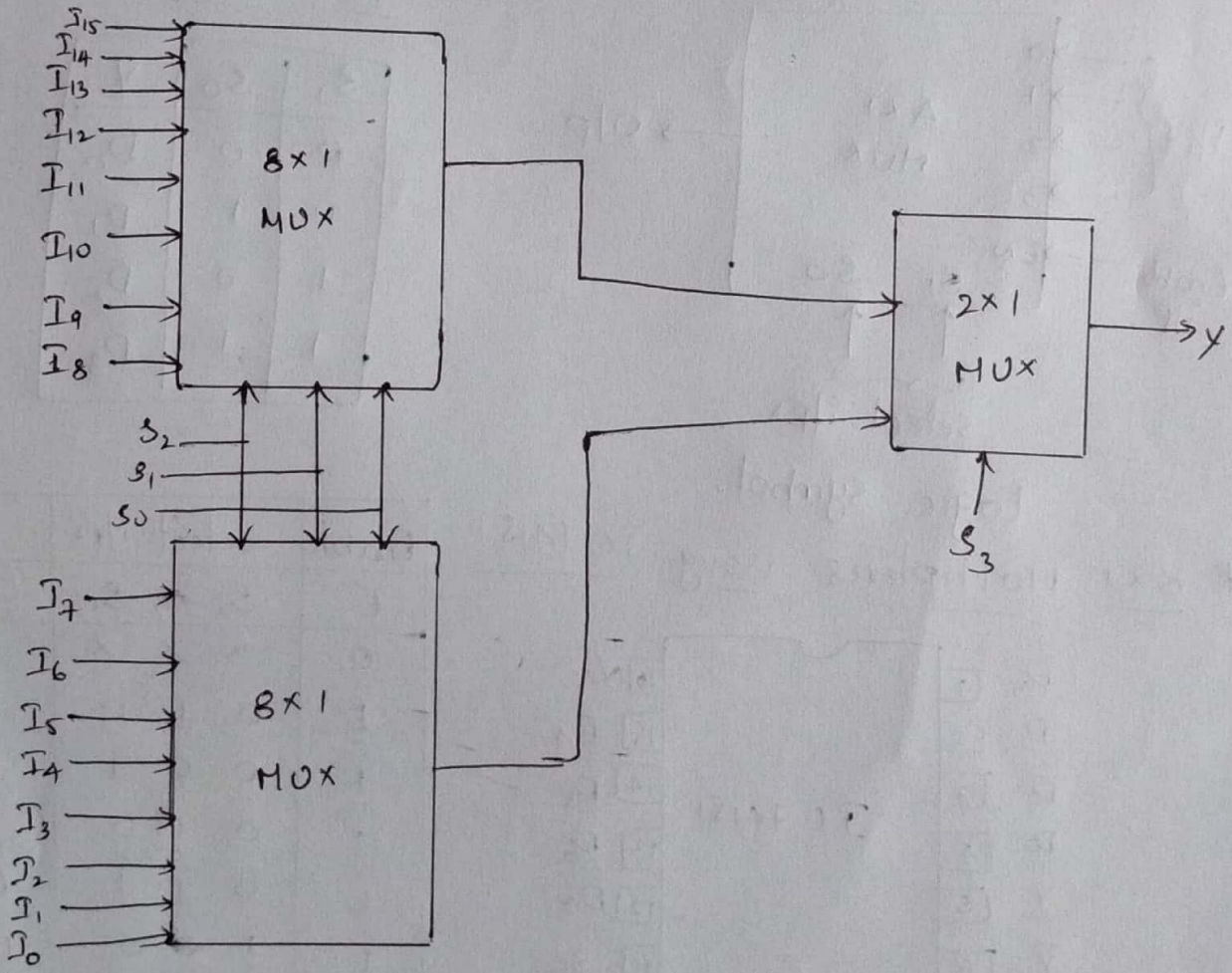
* Implementation :-

$f = \Sigma m(2, 4, 5, 7, 10, 14)$

	$\bar{D}$	D	
D_0	0	1	D
D_1	2	3	$\bar{D}$
D_2	4	5	1
D_3	6	7	D
D_4	8	9	0
D_5	10	11	$\bar{D}$
D_6	12	13	0
D_7	14	15	$\bar{D}$



* 16×1 MUX using two 8×1 MUX

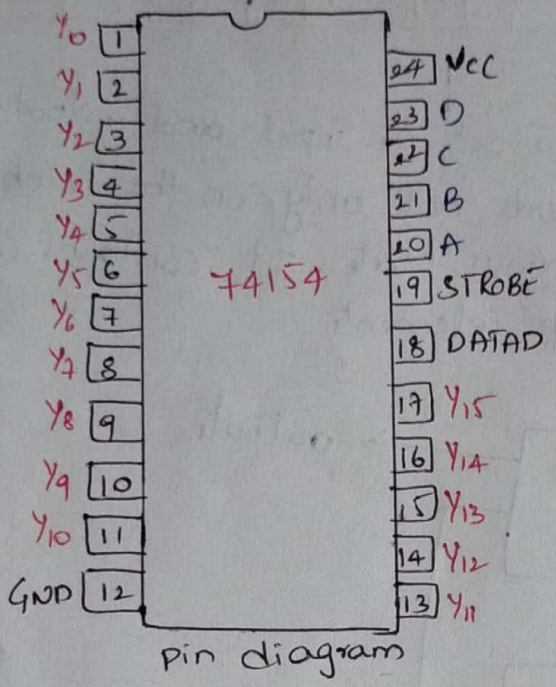


* Demultiplexer :-

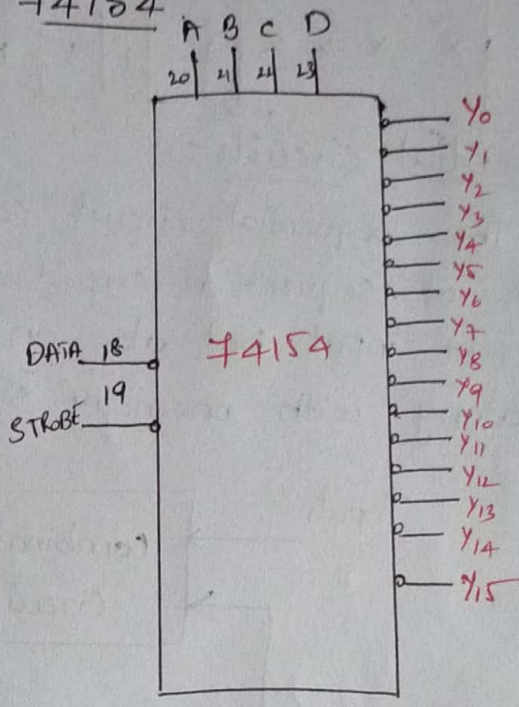
The Demultiplexer is a ckt that receives information on a single line and transmits this information on one of the 2^n possible o/p lines.

The selection of specific o/p line is controlled by the value of n selection lines.

* 1 to 16 Line Demultiplexer 74154 :



pin diagram



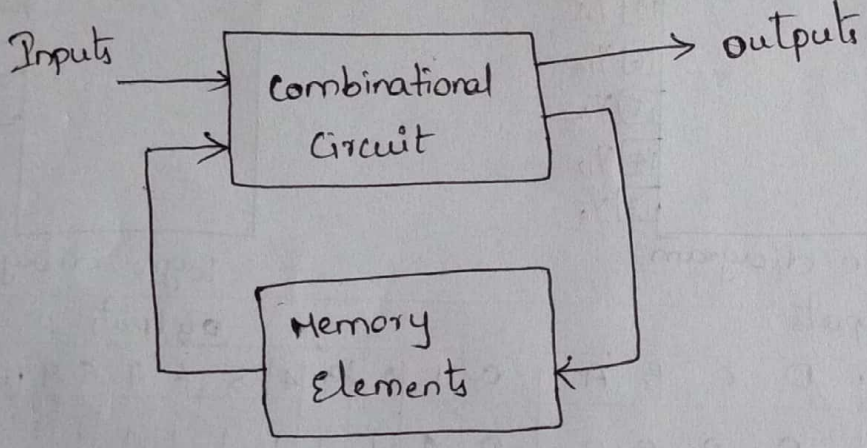
logic diagram

Inputs						outputs													
G_1	G_2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	0	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	0	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	0	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1
0	0	1	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1
0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0

G_1	G_2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
0	0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	x	x	x	x	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	x	x	x	x	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	x	x	x	x	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

* Sequential Circuits:-

The sequential circuit contains set of Input and output. The output of sequential circuit depends not only on the combination of present input but also on previous state. It contains combination ckts along with memory storage elements.



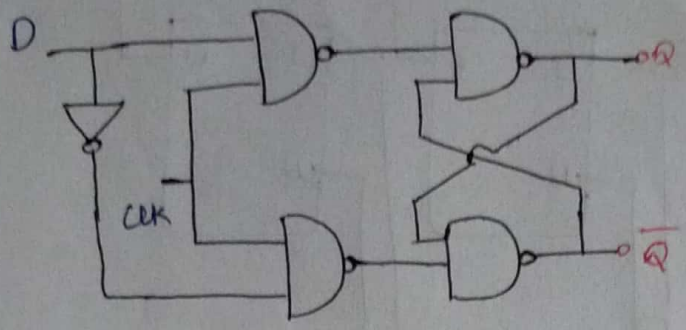
*flipflop:-

A flipflop is a basic memory element used to store only one bit of information.

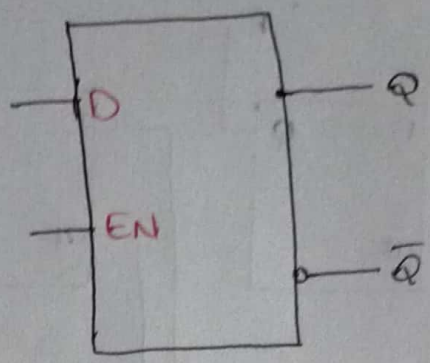
*latch:- A basic flipflop circuit without any clock pulse is called latch.

flipflop is a 1 bit memory cell which can be used for storing the digital data. To increase the storage capacity interms of number of bits, we have to use a group of flipflop. Such a group of flipflop is known as a Register.

* D-flipflop



logic diagram.



logic symbol.

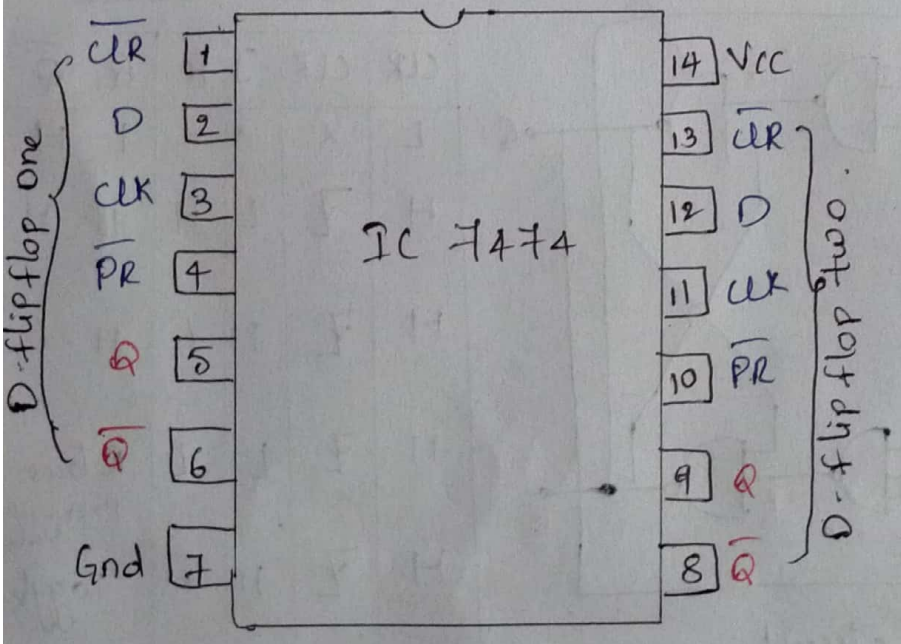
state table

Present state	Input	Next state
Q	D	Q(t+1)
0	0	0
0	1	1
1	0	0
1	1	1

$\bar{D}$=S D=R

S	R	Q
1	0	1
0	1	1
1	1	No chan
0	0	X

* D flipflop [IC 7474]

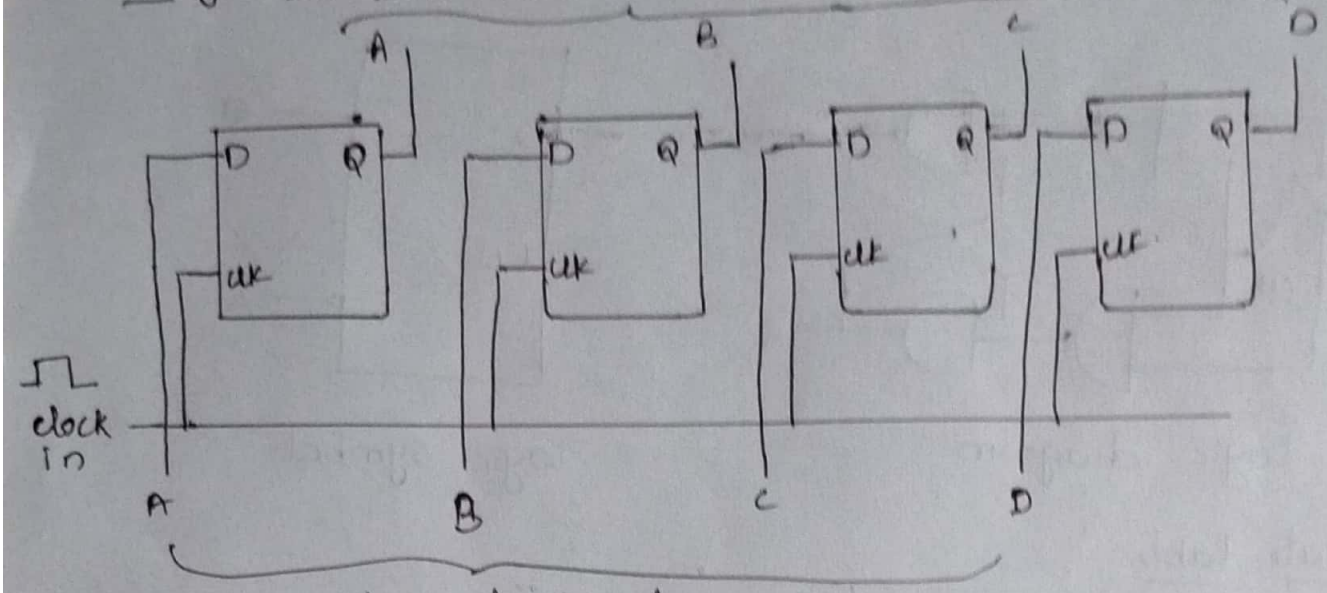


Truth Table.

Inputs				outputs	
PR	CLR	clk	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

CLR - clears the o/p to zero
PR - sets the o/p to one dual functionality

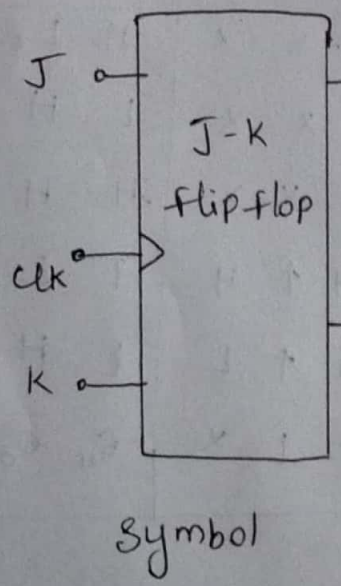
* Delay flip flop [4-Bit Data Input] 4-Bit Data output.



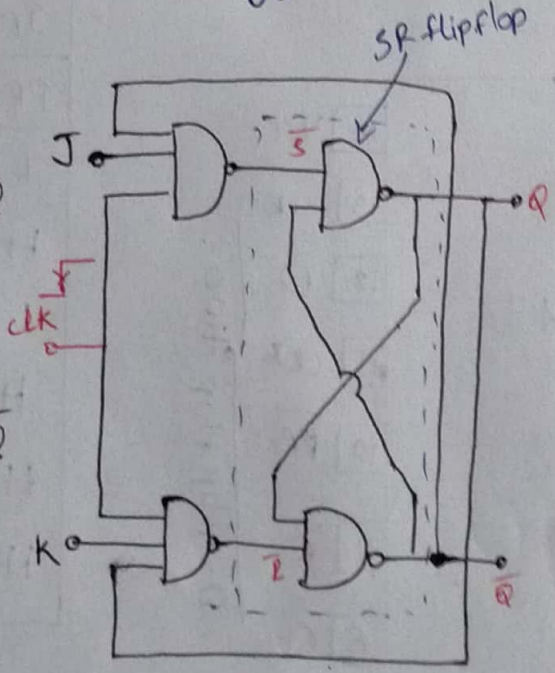
* IC 7473 [JK Master slave flip flop].

The master slave flip flop eliminates all the timing problems. The one flip flop acts as a Master ckt while the other acts as slave.

The TTL 74LS73 is a Dual JK flip flop IC, which conbins two individual JK type bistables within a single chip enabling single or master-slave toggle flip-flops to be made.



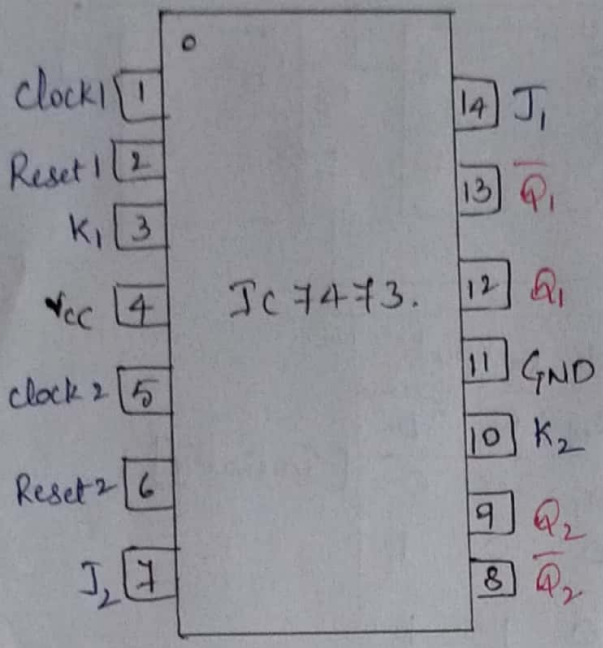
Symbol



circuit

Truth Table.

CLR	CLK	J	K	Q	$\bar{Q}$
L	X	X	X	L	H
H	↓	L	H	L	H
H	↓	H	L	H	L
H	↓	L	L	Retains Previous State	
H	↓	H	H	Toggle	



Pin diagram

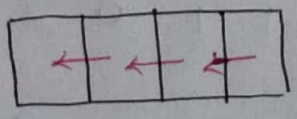
* Shift Register :-

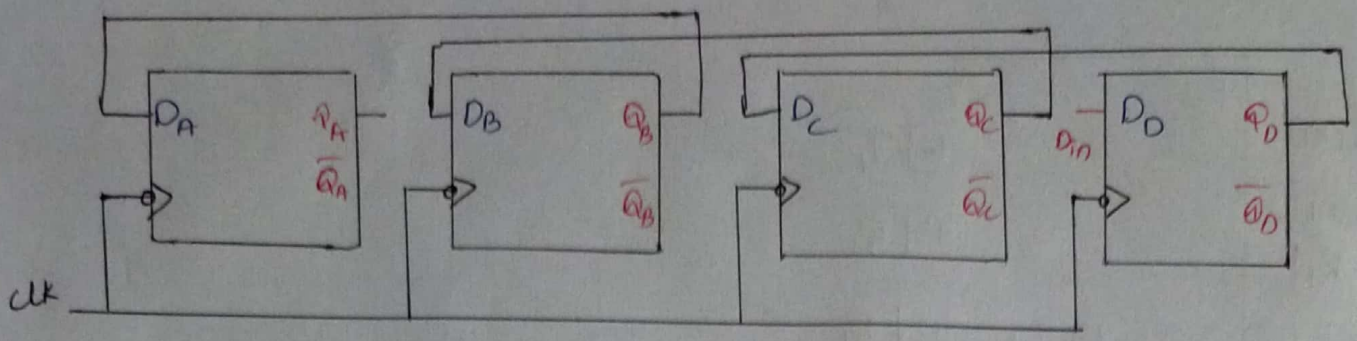
The movement of the bits or data

- classification based on the direction of data movement
  1. shift left Register
  2. shift right Register
- classification based on the mode of input and output
  1. SISO [Serial in Serial out shift Register]
  2. SIPO [Serial in parallel out shift Register]
  3. PISO [parallel in serial out shift Register]
  4. PIPO [parallel in parallel out shift Register]
  5. Universal shift Register.

* Shift left Register :-

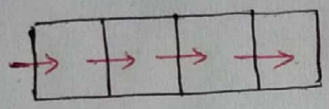
Generally D-flip flop is used for the operation of shift Register.

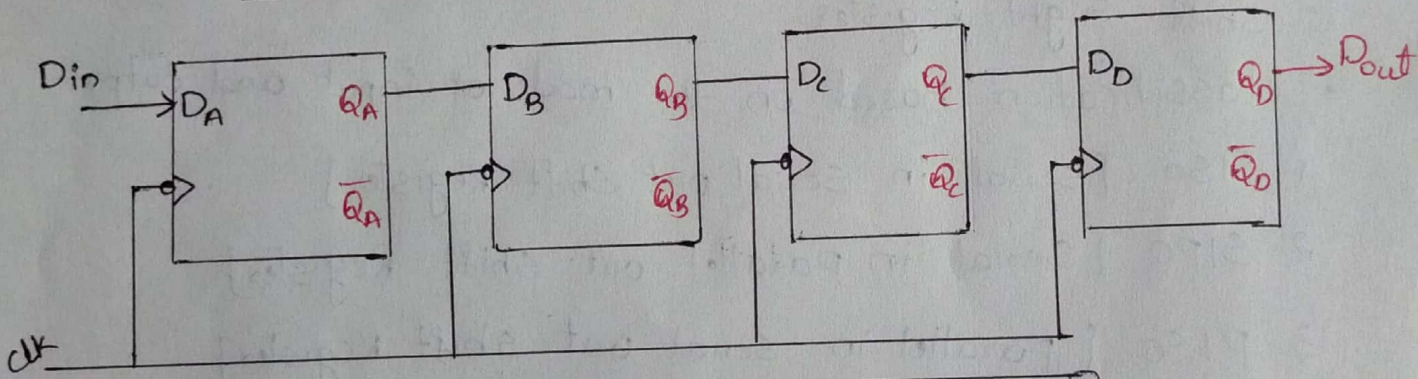




clock	Input	flipflop output				
		Q_A	Q_B	Q_C	Q_D	
		0	0	0	0	[Initially]
1	1	0	0	0	1	
2	1	0	0	1	1	
3	1	0	1	1	1	
4	1	1	1	1	1	

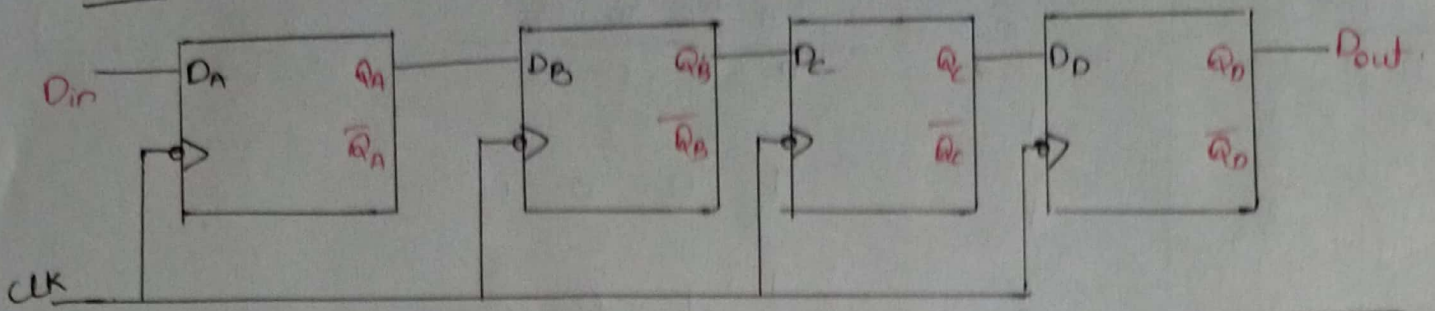
*Shift Right :-



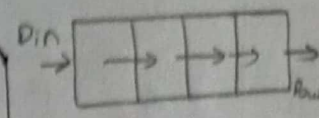


clock	Input	flipflop output				
		Q_A	Q_B	Q_C	Q_D	
		0	0	0	0	[Initial]
1	1	1	0	0	0	
2	1	1	1	0	0	
3	1	1	1	1	0	
4	1	1	1	1	1	

* SISO [Serial In Serial output shift Register]



Ex:- Din 1011

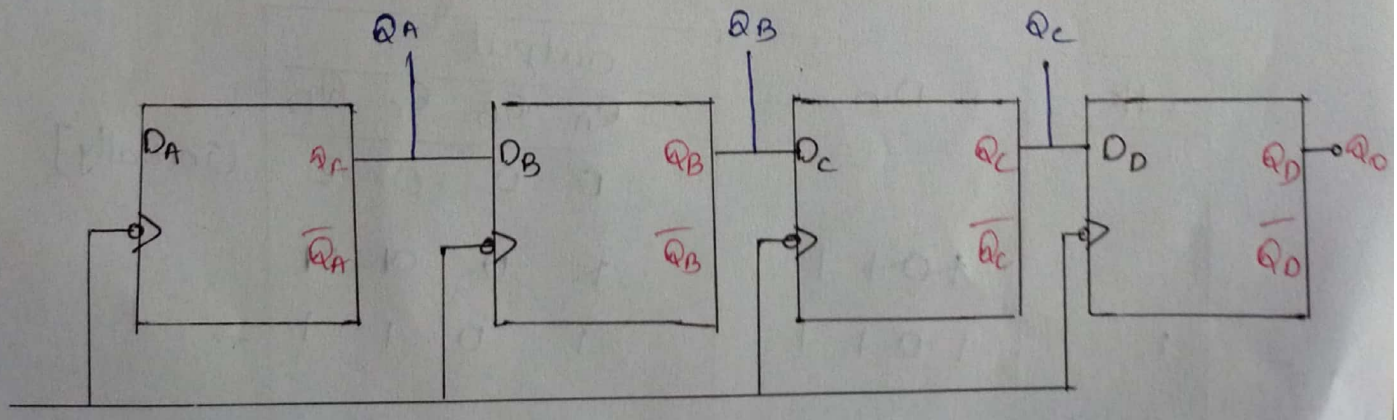


clock	Din	output Q_A	Q_B	Q_C	Q_D	
		0	0	0	0	
1	1	1	0	0	0	
2	0	0	1	0	0	
3	1	1	0	1	0	
4	1	1	1	0	1	
5		0	1	1	0	→ 1
6		0	0	1	1	→ 0
7		0	0	0	1	→ 1
8		0	0	0	0	→ 1

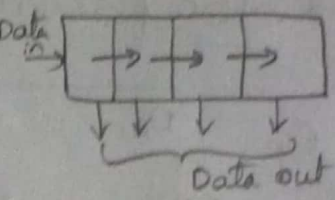
Serial out

* SIPO [Serial In parallel out Shift Register]

Parallel out means at a time output should be obtained.



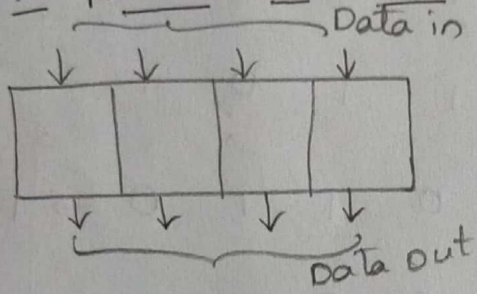
clk	Din	output Q_A Q_B Q_C Q_D
		0 0 0 0
1	1	1 0 0 0
2	1	1 1 0 0
3	0	0 1 1 0
4	1	1 0 1 1 → out.
5		0 0 0 0

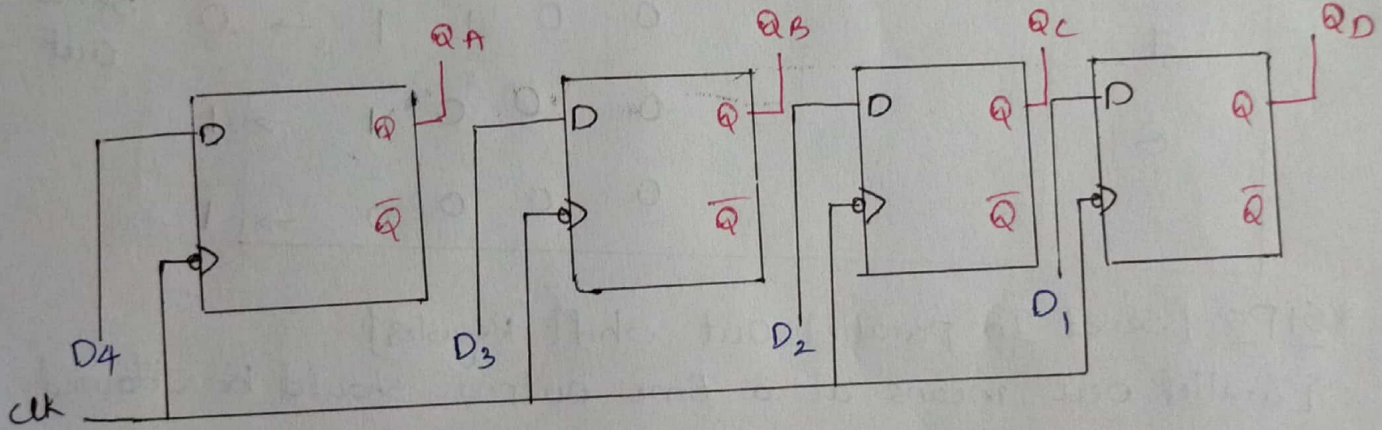


SISO - MSB bit is entered first

SIPO - LSB bit is entered first.

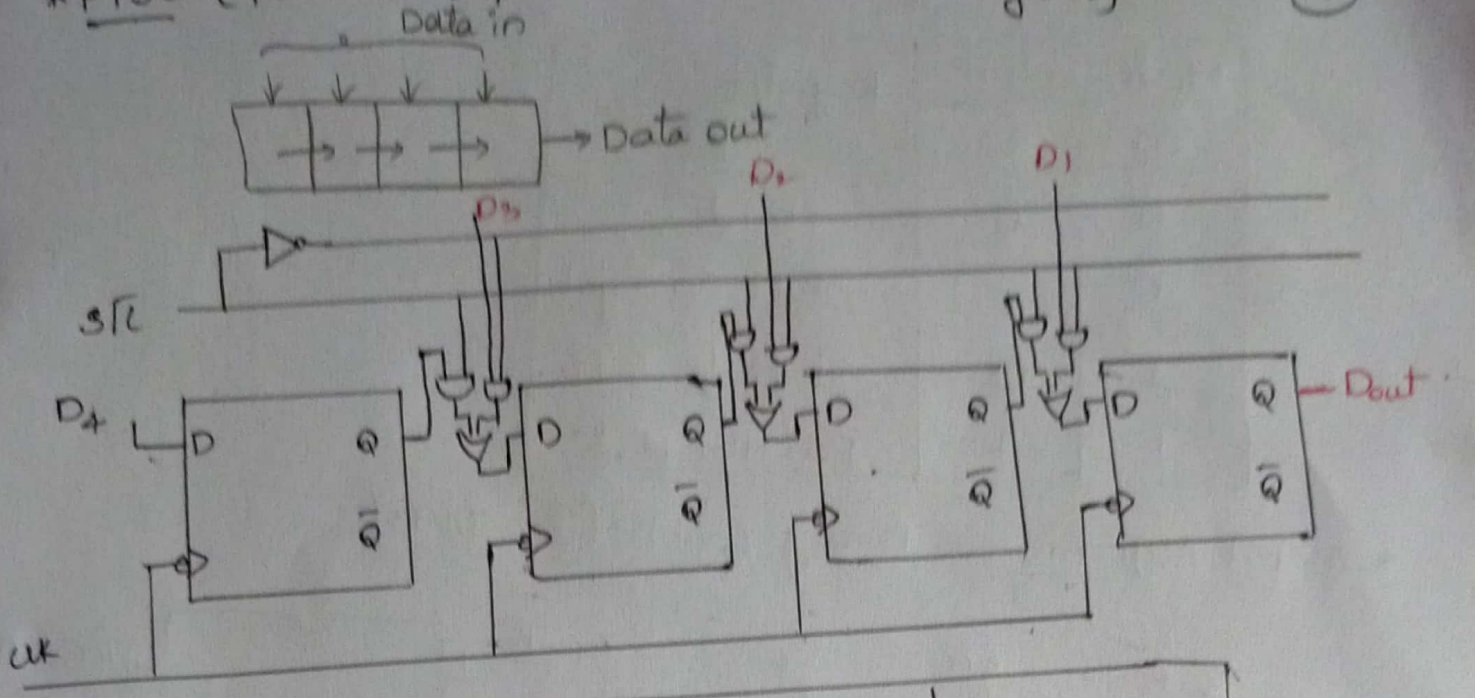
* Parallel In parallel out shift Register [PIPO]





clk	Din	output Q_A Q_B Q_C Q_D	
		0 0 0 0	(Initially)
	~~1 0 1 1~~	~~1 0 1 1~~	
1	1 0 1 1	1 0 1 1	→ out.
2		0 0 0 0	

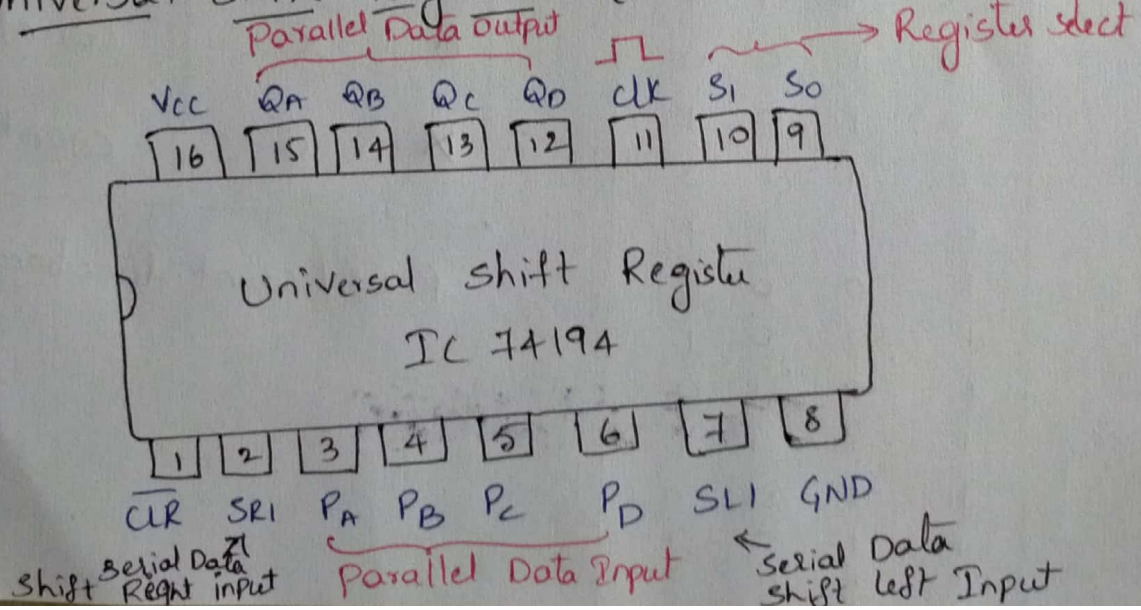
*PISO [Parallel Input Serial out shift Register]



clk	Input	output			
		Q_A	Q_B	Q_C	Q_D
		0	0	0	0
1	1101	1	1	0	1
2		0	1	1	0
3		0	0	1	1
4		0	0	0	1
5		0	0	0	0

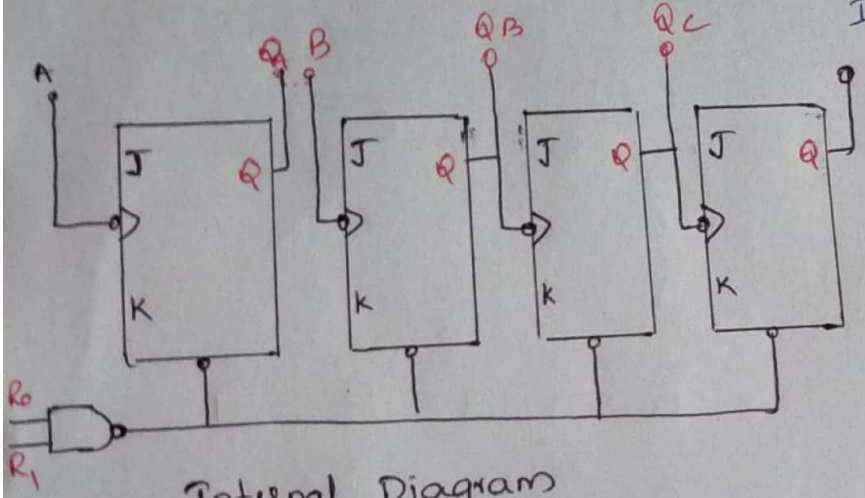
1 0 1 1 — out

* Universal shift Register :- [IC 74194]

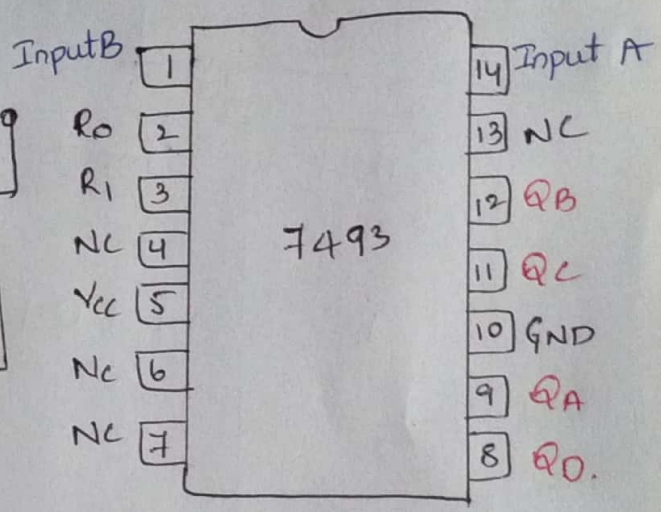


Mode control		Register Type
S_1	S_0	
0	0	Hold
0	1	shift to right
1	0	shift to left
1	1	Parallel Mode.

* 4-bit Asynchronous Binary Counter [IC 7493]



Internal Diagram



Pin diagram.

Count	output			
	Q_A	Q_B	Q_C	Q_D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

Reset Inputs		output			
R_0	R_1	Q_A	Q_B	Q_C	Q_D
1	1	0	0	0	0
0	x	count			
x	0	count			

Reset / count functional Table.