MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

Department of Electronics and Communication Engineering

TIME TABLE

Academic Year : 2015 - 2016
Class : B.Tech, ECE - IV YEAR II SEM - A

With Effective From : 23-11-15
Class Room no : 111

Period	I	II	III	12:15-1:00	IV	V	VI
Day/Time	9:15 - 10:15	10:15 - 11:15	11:15 - 12:15		1:00 - 2:00	2:00 - 3:00	3:00 - 4:00
Monday	CPLD & FPGA/ CAD FOR VLSI	Seminar		Lunch	RS	CPLD & FPGA/ CAD FOR VLSI	WCN/SC
Tuesday	WCN/SC	Seminar			CPLD & FPGA/ CAD FOR VLSI	RS	WCN/SC
Wednesday	RS	Industry Oriented Mini Project			RS	WCN/SC	CPLD & FPGA/ CAD FOR VLSI
Thursday	Major Project				Major Project		
Friday	Major Project				Major Project		
Saturday	Major Project				Major Project		

Sub Code	Theory/Practical	Hrs	Staff in-charge
204C1	Elective - III i)Wireless Communications & Networks ii)Satellite Communications	4	Dr.M J C Prasad Mr.P.Ashok Babu
204D2	Elective - IV Radar Systems	4	M.Kranthi Kumar
204E4.	Elective - V CPLD & FPGA CAD For VLSI	4	Mr. B Srinivas Dr.K.Sri Hari Rao
20427	Industry Oriented Mini Project	2	Mr. Yeligati Kiran, P.V.Subha
20428	Seminar	4	Dr. M J C Prasad, Mr.P.Ashok Babu, Mrs. Y Shirisha
20429	Major Project	18	Dr. S.Madhu Babu, , Mr. J.Sunil kumar, Mr. A.R.S.Balaji, Mr. T.Surendar Reddy, Mr. Gourishankar Sharma , Mr. D Praveen Kumar
	TOTAL	**36**	
Class Incharge			**Mr.G. Kumara Swamy**

TimeTable Incharge **HOD** **Principal**