Code No.: **54121**

MR 15

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)

Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.-500 100.

M.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, JULY-2017

SUBJECT: **: Design for Testability**

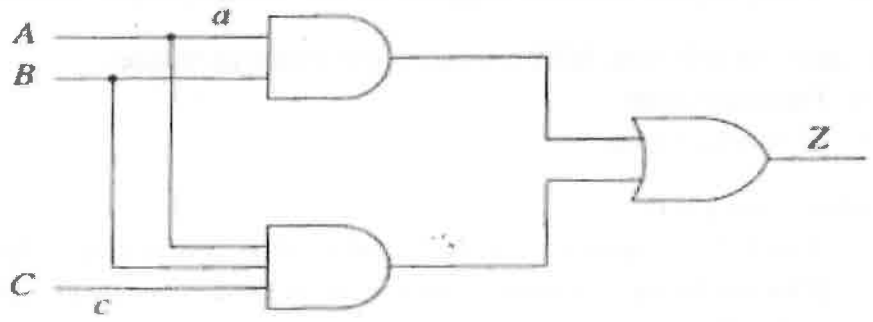
Branch/Specialization: ECE/VLSI SYSTEM DESIGN

Time: **3 Hours** Max Marks: **60**

PART-A

Answer the following Questions **5 X 4 Marks=20 Marks**

1. For the circuit of given figure
   a. Find the set of all tests that detect the fault a s-a-0.
   b. Find the set of all tests that detect the fault c s-a-1.



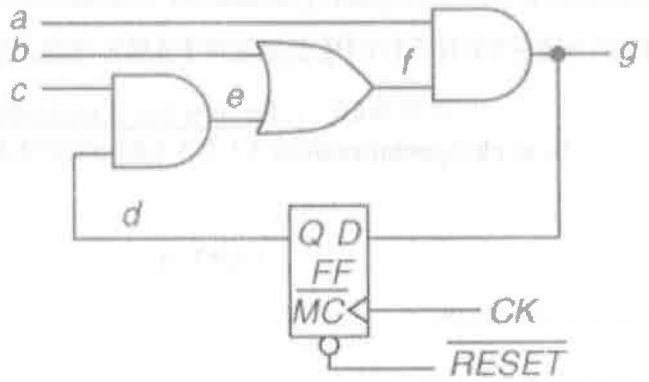
2. Explain the Transport Delays and Inertial Delays with an example.
3. Explain about Scan-Hold flip flop.
4. Explain about March test SRAM BIST.
5. Explain the following boundary scan test instructions
   a) Bypass b) Intest

PART-B

Answer any 5 questions **5 X 8 Marks=40 Marks**

1. Explain the following fault models. 8M
   a) Bridging fault b) Cross-point fault c) Path-delay fault d) Transition fault
2. a) Explain the dominance fault collapsing with an example. 4M
   b) How to test chips? What are the types of testing? 4M
3. a) Explain about the concurrent fault simulation with an example. 4M
   b) Briefly explain Roth's test-detect algorithm. 4M
4. a) Briefly explain about high level testability measures. 4M
   b) Explain about the partial scan design. 4M

5. Compute the combinational and sequential SCOAP testability measures (i.e., both controllability and observability) for the given circuit. 8M



6. a) With neat diagram, explain the process and implementation of the BIST. 4M
   b) Briefly explain about the weighted pseudo-random pattern generation. 4M

7. Explain the following BIST response compression techniques. 8M
   a) Transition count
   b) Signature analysis

8. Answer any **TWO**
   a) What is the difference between 'Boundary Scan Test' and 'Scan Test'? 4M
   b) What are the various control signals that are used in Test Access port controller? And explain them. 4M
   c) What is the procedure to do boundary scan testing for SRAM devices? 4M

Code No.: **54206** | **MR15**

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Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad.-500 100.

M.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, JULY-2017

SUBJECT: **CMOS MIXED SIGNAL CIRCUIT DESIGN**

Branch/Specialization: **ECE/ VLSI System Design**

Time: **3 Hours** Max Marks: **60**

PART-A

Answer the following Questions **5 X 4 Marks=20 Marks**

1. Write the importance of switched capacitor circuits in Analog and mixed signal design.
2. Explain about PLLs lock acquisition problem.
3. Discuss about stochastic approach in quantization noise.
4. Write about classifications of ADC.
5. Discuss about importance of Noise shaping modulators.

PART-B

Answer any 5 questions **5 X 8 Marks=40 Marks**

1. Explain the concept of fully differential filters and mention their benefits.
2. Explain the linear model of the type I PLL.
3. Explain about a) Binary scaled converts and b) charge redistribution switched capacitor circuits.
4. Explain about successive approximation converters.
5. Explain the approaches of digital decimation filters for over sampling A/D converters.
6. a. Explain about Low- Q Biquad filter.
   b. Explain whether a master slave D flip-flop can operate as a phase detector or a frequency detector. Assume the flip-flop provides differential outputs.
7. a. Explain about single-supply positive output converters.
   b. Explain about Time-interleaved A/D converters.
8. Answer any **TWO**
   a. write short notes on Delta-Sigma D/A converters.
   b. Explain the basic loop architecture of PLL.
   c. Explain the effect of jitters in analog circuits.

Code No.: **54124**

MR 15- 2016-17 Regular & 2015-16 Supply Admitted Students

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)
Maisammaguda, Dhulapally,(Post Via Kompally), Secunderabad-500 100.

M.TECH II SEMESTER REGULAR & SUPPLEMENTARY EXAMINATIONS, AUGUST - 2017

SUBJECT: **AD HOC WIRELESS NETWORKS**

Branch/Specialization: **ECE/Common to Embedded Systems (Reg) & VLSI System Design (Supply)**

Time: **3 Hours** Max. Marks: 60

PART-A

Answer All Questions **5 X 4M = 20 Marks**

1. List and explain the fundamentals of Wireless LANs.
2. Classify MAC protocols of ad hoc wireless network.
3. What do you mean by table-driven routing protocols? List examples.
4. What are the issues and Challenges in providing QoS in Ad Hoc Wireless Networks?
5. What are the various evolving Standards in sensor networks?

PART-B

Answer any 5 Questions **5 X 8M =40 Marks**

1. Differentiate HIPERLAN standards. (8M)

2. a) Explain the major issues that affect the design and performance of an ad hoc wireless network. (4M)
   b) Explain MACAW protocol. (4M)

3. (a) Explain hidden terminal problem. (4M)
   (b) Explain the AODV routing protocol. (4M)

4. a) Explain Ticket Based QoS Routing Protocol (4M)
   b) Classify QoS solutions for ad hoc wireless network. (4M)

5. a) Explain the Clustered sensor network architecture. (4M)
   b) Write briefly about data dissemination in sensor networks. (4M)

6. a. Explain about Collision Avoidance Time allocation protocol. (4M)
   b. Explain issues in designing MAC Protocols for adhoc networks. (4M)

7. a. What are the design goals of a transport layer protocol for ad hoc wireless networks. (4M)
   b. Explain one Transmission Power Management Schemes for Ad Hoc Wireless Network. (4M)

8. Answer any **TWO**
   a. Explain issues in TCP in Wireless Domain. (4M)
   b. What do you mean by flooding explain with an example. (4M)
   c. Write on Data Dissemination in wireless sensor networks. (4M)